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Fabrication-Tolerant GaAs/SiN Coupling Above the Loss Threshold for Quantum Photonic Applications

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ABSTRACT

Quantum photonic integrated circuits (QPICs) are a promising platform for scalable quantum technologies. A major outstanding challenge is the efficient interconnection of diverse quantum photonic components, where optical losses must remain below the ~10% threshold required for advanced quantum applications. In this paper, the optical coupling between GaAs single-photon sources and a low-loss SiN interposer is investigated, where reliable high-efficiency transitions have not yet been achieved. To address this, a fully numerical framework is introduced for the optimization of waveguide mode couplers that directly incorporates experimentally characterized fabrication variations critically impacting performance, including waveguide misalignment, width deviation, and sidewall roughness. Using this approach, low-loss GaAs/SiN transitions are designed and experimentally demonstrated with reproducible coupling efficiencies of –0.43 dB ± 0.14 dB. These results establish a viable path toward low-loss heterogeneous QPICs tailored to advanced quantum applications.

1 | Introduction

The development of quantum technologies is driven by their potential to achieve capabilities beyond those of classical systems in communication, computation, simulation, and sensing [1]. A promising route toward these applications relies on controlling light–matter interactions, enabling the generation and manipulation of single photons [2, 3]. A key area of research in this domain is that of quantum photonic integrated circuits (QPICs) [4, 5], which aim to break the scalability limitations of conventional quantum photonic systems based on bulk optics [6]. The stringent performance requirements of advanced quantum applications [7–9] demand the use of the highest-quality QPIC components—such as single-photon sources, modulators, and detectors—that are based on distinct materials and fabrication platforms. The interconnection of these components must achieve ultra-high efficiency, with optical losses below ~10%. This inevitably requires heterogeneous integration on top of a common low-loss interposer platform. Such integration can be realized with techniques like micro-transfer printing (μTP) [10–13], which enables dense physical integration using commercial tools that provide scalable assembly with an alignment precision of 500 nm (3σ).

Within QPICs, the integration of single-photon sources (SPSs) plays an essential role. InAs quantum dots (QDs) embedded in

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GaAs waveguides have been established as excellent on-demand SPSs, combining near-unity emission purity and indistinguishability [14, 15]. From a loss perspective, this is enabled by high QD–waveguide coupling efficiencies (β > 98.4%) [16]. Consequently, for their co-integration with other components in heterogeneous QPIC architectures, the dominant contribution to photon loss arises from the transition between the GaAs emitter platform and the interposer.

While different strategies can be used to implement this coupling, mode couplers based on adiabatically tapered waveguides have shown the most potential for high coupling efficiency and tolerance to fabrication variations [17]. They consist of two parallel waveguides and gradually transform the guided mode by tapering the waveguide widths, enabling evanescent transfer of light from one waveguide to another without exciting unwanted modes [18]. This has led to near-lossless transitions for other essential devices that allow photon routing [19], manipulation [20, 21], and detection [21]. The GaAs–interposer transition needed for SPSs has, however, remained lacking in performance for two main reasons. First, the GaAs SPS platform suffers high waveguide propagation losses on the order of a few tens of decibels per millimeter [22]. This is related to electroabsorption and scattering from fabrication-induced sidewall roughness, where the latter is highly dependent on the waveguide cross-section [23] and thus the dominant loss mechanism relevant for coupler design. Second, fabrication variations—such as µTP-induced misalignment and other geometric deviations arising from processing—pose a significant challenge for achieving reliable > 90% optical coupling [24–27]. The coupler design challenge thus remains to determine a waveguide tapering profile that is simultaneously compact, highly efficient, and maintains high efficiency under fabrication-induced imperfections—i.e., exhibits high fabrication tolerance. One possible approach is to employ semi-analytical taper design methods, which generate short tapering profiles based on adiabaticity criteria [28–30]. However, these approaches do not enable the direct incorporation of fabrication variations and sidewall roughness into the design process. Therefore, fully numerical approaches are a promising alternative for achieving improved coupling performance under realistic conditions [31].

In this work, we design and experimentally validate two novel mode couplers for GaAs SPSs that are micro-transfer printed on a SiN interposer platform. We employ a numerical design approach that includes a complete systematic fabrication-variation corner analysis based on experimentally characterized imperfections—primarily µTP-induced misalignment and GaAs waveguide width deviation, as well as bonding-layer thickness deviation and minor refractive index uncertainties. Due to the adiabatic operating principle of the couplers, accounting for this broad set of variations inherently promotes robustness also against other small variations not explicitly considered, such as operating wavelength. Furthermore, for the first time to our knowledge, we optimize the waveguide tapering profile for maximal coupling efficiency while directly incorporating a width-dependent scattering loss model. We verify our approach through experiment as well as rigorous 3D finite-difference time-domain (FDTD) simulations. With this, we demonstrate low-loss fabrication-tolerant GaAs/SiN coupling with a reliable insertion loss as low as −0.43 dB ± 0.14 dB. The measured performance not only surpasses the loss threshold for quantum photonic applications of 90%, but also shows good agreement with simulations. Furthermore, our fabrication-aware numerical optimization approach can be directly translated to other platforms, facilitating the design of robust low-loss couplers for diverse heterogeneously integrated QPIC devices.

2 | Adiabatic Mode Coupler Design

2.1 | Device Structure

The structure of the optical mode couplers based on adiabatic waveguide tapers is shown in Figure 1. It consists of a micro-transfer printed GaAs strip waveguide with an embedded QD and an underlying SiN strip waveguide, separated by a thin divinylsiloxane-bis-benzocyclobutene (DVS-BCB) bonding layer. Only the GaAs waveguide (WG) is tapered, making the SiN structure translation-invariant in the longitudinal direction, so µTP-induced misalignment can only occur in the other, transverse direction. The QD emits single photons in the fundamental TE mode (TE_{00}) of the GaAs WG around a ~930 nm wavelength (λ)—the exact wavelength varies between QDs in a 30 nm range. As the photons travel along the GaAs taper, they are gradually transferred to the SiN WG (illustrated in Figure 1a). For our numerical optimization process, the GaAs taper is divided into $N = 24$ linear segments, each defined by its length L_i and two WG widths W_i and W_{i+1}, indicated both in Figure 1a and in a top view of the taper in Figure 1b. Each segment increments the taper width by 10 nm starting from the tip width (W_1) and ending at the final WG width (W_{25}). To minimize the mode mismatch losses at the taper tip, W_1 must be below ~100 nm according to our analyses—a width of 100 nm can already induce losses up to a few percent in some cases. Therefore, W_1 is selected to be 60 nm, which is the minimum feature size allowed by our electron beam lithography (EBL) processing. On the other hand, W_{25} is 300 nm, selected for high QD–WG coupling [32]. The remaining segment lengths L_i define a taper profile and are the subject of coupler design and optimization.

The transverse cross section of the device is shown in Figure 1c, with a GaAs and SiN layer thickness of 170 and 300 nm, respectively. The bonding layer thickness ($D_{DVS-BCB}$) is around 20 nm (see "Methods" for fabrication details). The width of the SiN WG is 2 µm to accommodate some misalignment (ΔY) during µTP. We also consider systematic variations of GaAs structure width (ΔW)—both the straight WG and the taper—and DVS-BCB thickness ($\Delta D_{DVS-BCB}$). Lastly, we also investigate propagation losses caused by GaAs sidewall roughness as mentioned in the introduction. Figure 1d shows the geometry and lateral FDTD discretization grid of a GaAs taper tip with applied sidewall roughness. This is characterized by a roughness root-mean-square (RMS) value (σ), conveying its transverse magnitude, and correlation length (L_c), conveying its longitudinal properties. We employ estimated values of $\sigma = 2$ nm and $L_c = 50$ nm, determined from SEM images of fabricated GaAs WGs similar to [23].

2.2 | Taper Optimization Approach

For taper optimization, simulations were performed for a wavelength of 930 nm with the Ansys-Lumerical eigenmode expansion

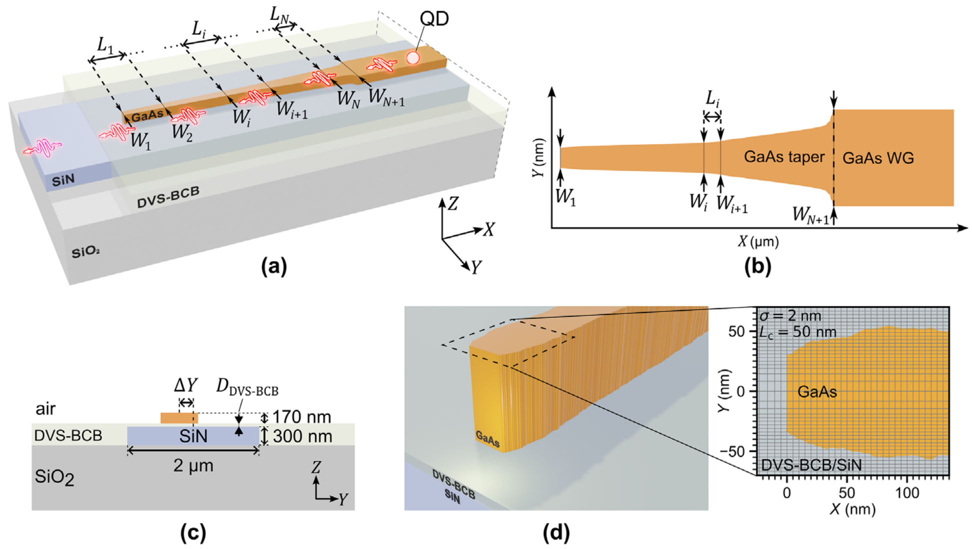

FIGURE 1 | Optical GaAs/SiN mode coupler and its design parameters. (a) 3D schematic of the structure with an illustration of a quantum dot (QD) and emitted photons. (b) Top view of the GaAs taper. (c) General structure cross section. (d) Geometry of a GaAs taper tip with applied sidewall roughness. The inset shows the top view of the tip overlayed by the FDTD simulation discretization grid.

(EME) simulator, enabling efficient segment length variation, whereas performance verification was done with the FDTD simulator. We refer to the "Methods" section for more details on the employed procedures.

We designed two tapers considering several systematic variations that include ΔY, ΔW, $\Delta D_{\text{DVS-BCB}}$, Δn_{GaAs}, and Δn_{SiN}, with the latter being variations of GaAs and SiN material refractive indices. The wavelength was not varied as broadband operation is expected from the already broad set of considered variations. In each case, several EME simulations were executed for different cases of systematic variations, including all fabrication corners (combinations of extreme values of variation parameters). Optimal taper segment lengths (L_i) were determined using a global optimization algorithm (dual annealing implementation in SciPy [33]) according to an objective function to be minimized. This function presents the key difference between the two designs.

For the optimization of the first taper (hereafter the baseline taper), we used the following objective function:

$$f_1\,(T_1,\ldots,T_M,L)=\sum_{j=1}^{M} w_j\left(\frac{1-T_j}{C_T}\right)^2+\left(\frac{L}{C_L}\right)^2 \qquad (1)$$

where the values of T_j $(T_1,\ldots,T_M)$ correspond to the transmission of the full coupler obtained from M EME simulations including a wide range of considered systematic variations, and L is the total taper length. The parameters w_j, C_T, and C_L are normalized weights and normalization constants. This function consists of two parts in order to penalize both simulated coupling losses and taper length. The normalization constants give control over their relative importance and the weights are chosen to prioritize the nominal variation case over fabrication corners. Each term is squared to steer the optimization algorithm away from excessively large values of L or $1-T_j$.

In the optimization of the second taper (hereafter the next-generation taper), we used a different optimization function to determine the taper segment lengths:

$$f_2\,(T_1,\ldots,T_M,L_1,\ldots,L_N) = \left[\sum_{j=1}^{M} w_j\left(1-T_j\cdot 10^{-\frac{1}{10}\sum_{i=1}^{N}\alpha_{j,i}L_i}\right)^p\right]^{\frac{1}{p}} \qquad (2)$$

where the explicit term penalizing the taper length in the second part of Equation 1 is replaced by directly incorporated propagation losses $\alpha_{j,i}$ (in decibels per unit length). The indices j and i define the variation case and taper segment, respectively, and the constant p is used to steer the optimization algorithm similar to Equation 1. Using this function, the taper length is naturally constrained through propagation losses and the function value corresponds to an actual physical quantity (optical loss). In this case, the considered fabrication corners are focused on a smaller, more realistic range of systematic variations.

2.3 | Propagation Loss Model

The modelled propagation losses $\alpha_{j,i}$ originate from GaAs WG sidewall roughness and depend on the WG width. Their magnitude was determined with 3D FDTD simulations similar to [23], where this was done for waveguides on the standalone GaAs SPS platform. The simulated propagation loss for the hybrid GaAs/SiN case is shown in Figure 2 (solid black line) as a function of GaAs WG width (W_{GaAs}). At the nominal width (W_{GaAs} = 300 nm), the propagation loss is 5.1 dB/mm and grows with increasing W_{GaAs}. Toward narrower widths, the losses initially decrease slightly before rapidly growing fivefold at 185 nm. After this peak, the losses rapidly decrease and fall below 0.1 dB/mm for W_{GaAs} below 100 nm. In relation to adiabatic tapers, these losses

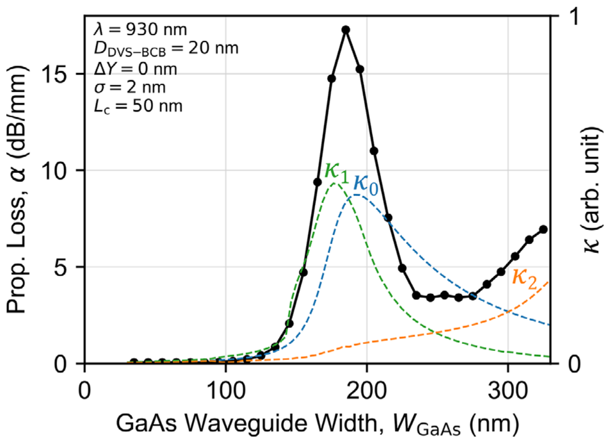

FIGURE 2 | Modelled propagation loss caused by sidewall roughness of GaAs waveguides printed on top of SiN waveguides (solid black line) and combined intermodal coupling terms (dashed colored lines).

are critically important since the high loss peak is located in the middle of the coupling region in Figure 1.

To study the origin of the peak and the growing trend toward large W_{GaAs}, we investigated intermodal coupling terms linked to the sidewall perturbation. Because the hybrid GaAs/SiN structure supports a large number of modes, we grouped contributions from different modes coupling to the TE_{00} mode into three combined terms—$\varkappa_0$, $\varkappa_1$ and $\varkappa_2$ (dashed colored lines in Figure 2). The first is the TE_{00} self-coupling coefficient, and the second two are sums of coefficients of cross-coupling between TE_{00} and higher-order modes. $\varkappa_0$ and $\varkappa_1$ are clearly related to the peak at W_{GaAs} = 185 nm and $\varkappa_2$ is related to the increasing trend toward large W_{GaAs}. Therefore, we attribute the peak to both self-interaction of TE_{00} and its interaction with higher-order modes, and the increasing trend only to the latter. We refer to ref. [23] for a deeper discussion of these coefficients.

3 | Results

3.1 | Optimized Tapers

The taper profiles obtained from numerical optimization are shown in Figure 3a. We also compare with the current state-of-the-art 3-segment taper from [25] (hereafter the reference taper), which is based on an established design method [28] that is less focused on fabrication variation corners and does not include propagation losses. The taper profiles are drawn in different base colors with tick marks at segment boundaries. For the new taper designs, modelled propagation losses are additionally indicated along the profiles by a heatmap (red). In all cases, the GaAs is tapered faster near the ends of the structure and slower in between, where light transitions from GaAs to SiN and is most susceptible to coupling with other modes [34]. The baseline taper (blue) is similar to the reference taper (brown) with a few small differences and faster tapering at the wide end, making it slightly shorter (39.5 µm) in comparison (45 µm). On the other hand, while the length of the next-generation taper (green) is similar (41.7 µm), it stands out with a different overall shape. The profile starts out at a shallow angle and progresses to a steeper angle about midway. This significantly compresses the region where propagation losses are highest in comparison with the other designs.

The modelled coupling loss of the different mode coupler designs is indicated in Figure 3b for expected and extreme values of the most critical systematic variations—ΔY and ΔW. Extensive analyses revealed that $\Delta D_{DVS-BCB}$, Δn_{GaAs}, and Δn_{SiN} have a smaller impact in comparison and are thus omitted for clarity. The coupling losses are given as losses extracted from simulations—in this case FDTD for verification—considering systematic variations (solid color) combined with scattering losses calculated from the propagation loss model (shaded area) shown in Figure 2. The simulated loss of the reference and the baseline taper is similar in all cases, with the latter showing slightly improved performance and lower variability. Their scattering losses appear almost identical. For the next-generation taper, the simulated loss is similarly low for smaller, expected variations but increases with less probable extreme variations. This is a result of the selected weights and systematic variation ranges used in the optimization procedure. As explained before, the next-generation taper is focused on realistic operating conditions and sidewall roughness while the baseline taper considers more extreme fabrication corners. This way, the resulting scattering loss contributions for the next-generation taper are two to four times smaller in all cases at the cost of increased loss in extreme corner cases. Consequently, the total coupling loss of the next-generation taper is substantially lower compared to the baseline taper for realistic systematic variations and is therefore expected to show the highest performance in experiments.

3.2 | Fabricated Structures

To validate the improved taper designs, we fabricated samples with GaAs WGs micro-transfer printed on top of SiN WGs using the procedures explained in refs. [25] and [35]. For more fabrication details, we refer to the "Methods" section. The fabricated GaAs WGs included tapers on both ends to couple light from SiN to GaAs and from GaAs back to SiN. The SiN WGs were terminated by focusing grating couplers to enable optical transmission measurements.

An optical microscope image of a complete GaAs/SiN circuit is shown in Figure 4a with scanning electron microscope (SEM) images of individual regions shown in Figure 4b–d. Figure 4b shows a SiN focusing grating coupler and part of the µTP site, where the SiN WG is tapered from a nominal with of 880 nm to 2 µm (used for µTP). Figure 4c shows the middle section of the tapered GaAs WG—this is a 5 µm straight section joining the two tapers. A part of the right taper is shown in Figure 4d.

We inspected the fabricated devices with SEM to analyze their structural integrity and systematic variations. A few circuits were damaged during µTP and were thus excluded from further analysis (see "Methods"). We determined the misalignment statistics of the µTP procedure based on 50 successfully printed GaAs WGs, as shown in Figure 4e. The median ΔY is −70 nm, which indicates a small offset in accuracy due to the µTP alignment procedure. The standard deviation of the data is 230 nm, which is in line with the specifications of the µTP tool. Additionally, we examined ΔW of 14 WGs and determined a −14 nm median and

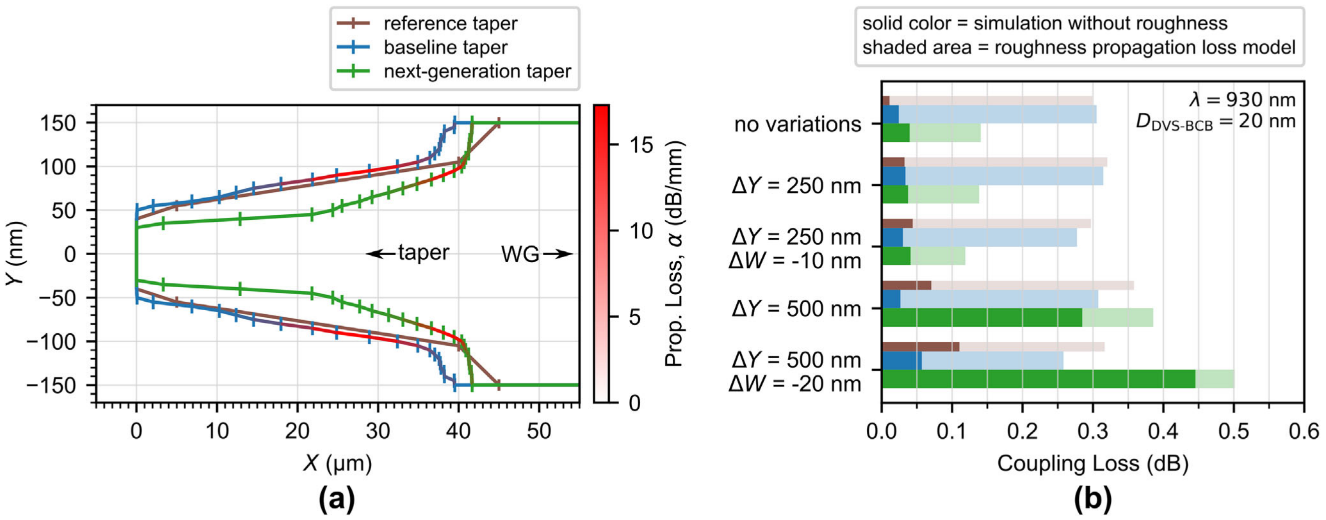

FIGURE 3 | Optimization results for the designed tapers. (a) Taper profiles with marked segment boundaries including a heatmap of modelled propagation losses. Reference 3-segment taper from ref. [25] is shown for comparison. (b) Modelled coupling loss for key systematic variations.

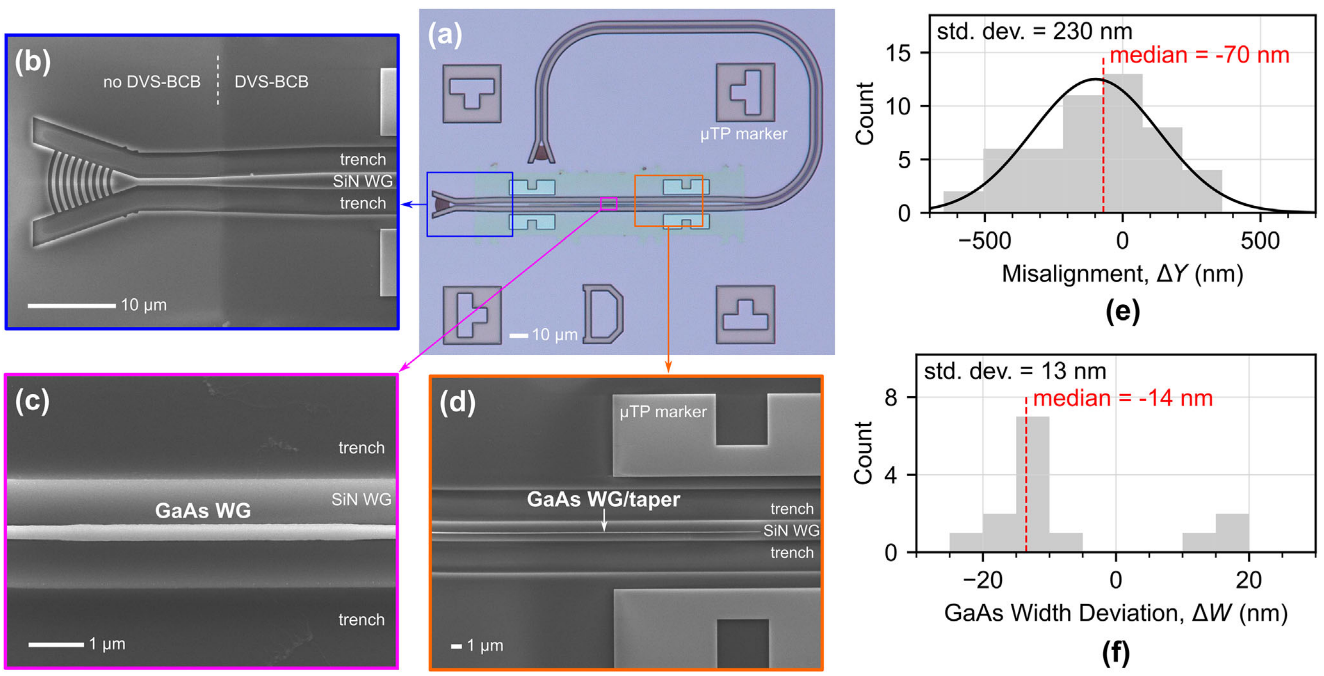

FIGURE 4 | Fabricated GaAs/SiN circuit. (a) Optical microscope image of a complete circuit. SEM images of individual regions are shown in (b–d). (b) SiN focusing grating coupler and edge of DVS-BCB layer. (c) Middle section of the GaAs WG. (d) Part of the right GaAs taper. (e) Measured GaAs WG misalignment statistics. (f) Measured GaAs width deviation statistics.

a 13 nm standard deviation, as shown in Figure 4f. We attribute this to pre-processing on the source GaAs chip prior to micro-transfer printing. Both the characterized ΔY and ΔW confirm our optimization procedure is based on reasonable assumptions regarding fabrication variations.

3.3 | Coupling Efficiency Measurements

GaAs/SiN coupling efficiencies were determined through optical transmission measurements performed in a cryostat at 4 K (QD operating temperature [2]). We measured the transmission of the fabricated circuits through an objective using a supercontinuum laser and a spectrometer. Five representative measured GaAs/SiN circuit transmission spectra are shown in Figure 5 for each taper design, including the highest and lowest obtained transmissions (excluding damaged circuits). For comparison, the mean transmission spectrum of calibration circuits with the same SiN layout but without printed GaAs WGs is shown (black). The measured transmission spectra generally follow the characteristic bell shape of grating coupler transmission that governs the mean calibration spectrum. The

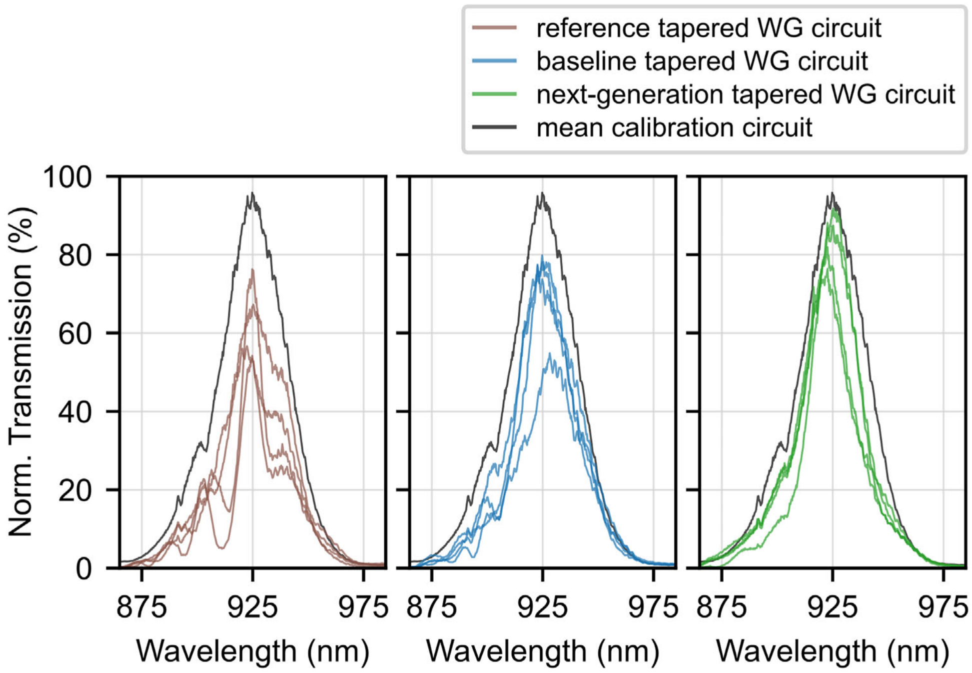

FIGURE 5 | Representative measured transmission spectra of GaAs/SiN circuits.

decreased transmission of GaAs/SiN circuits compared to calibration circuits is due to the transmission through the printed GaAs WG. In the case of the reference taper design (brown), transmission is lowest and exhibits pronounced interference fringes. These are reduced for the baseline taper (blue) and the smallest in the case of the next-generation taper (green), which also exhibits the highest transmission. We attribute the fringes to beating between the fundamental mode (even supermode) and higher-order modes (predominantly the odd supermode), which can be partly excited in the tapering regions—particularly in case of misalignment and other systematic deviations [34].

To determine the coupling efficiency of the mode couplers, η, we extracted the peak transmission of each circuit within a 920–930 nm wavelength range around the grating coupler peak transmission, as this yields the most reliable estimate of η by minimizing the influence of chip coupling variations and interference fringes. We determined the insertion loss (in decibels) of each printed GaAs WG by normalizing this value to the extracted peak transmission of adjacent calibration circuits. We corrected for the scattering loss in the 5 µm middle section of the printed GaAs WGs (0.055 dB) based on measured propagation losses of 11 dB/mm ± 0.3 dB/mm (discussed in Section 4). These were extracted from GaAs waveguides of different lengths printed on the SiN chip. The resulting η per taper is shown by the boxplot in Figure 6.

The baseline taper exhibits a higher η with reduced variability compared to the reference taper. The next-generation taper achieves an even higher η but shows slightly more variability compared to the baseline taper, which we attribute to the design trade-off between tolerance to systematic variations and propagation losses. To show the most probable coupling efficiencies, we report η as the median ± spread, chosen conservatively as the larger distance from the median to the lower or upper quartile. Therefore, η is −1.05 dB ± 0.20 dB, −0.58 dB ± 0.13 dB, and −0.43 dB ± 0.14 dB for the reference, baseline, and next-generation taper designs respectively. The reference taper performance here remains consistent with prior work [25, 36], validating our fabrication and measurement approach. It further indicates successful optimization of GaAs tapers with improved coupling efficiency and tolerance to both systematic variations and propagation losses.

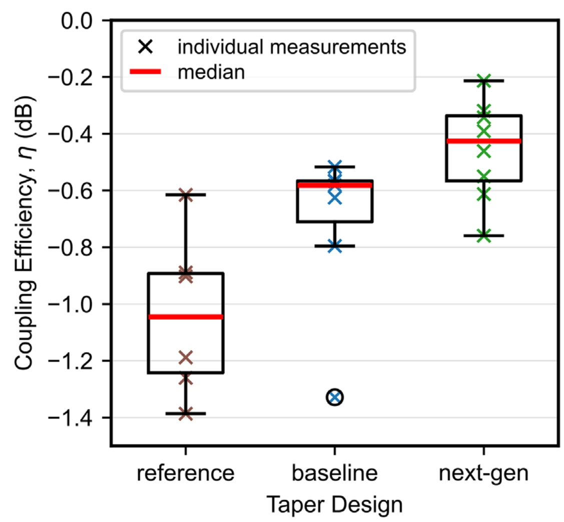

FIGURE 6 | Measured coupling efficiency of fabricated GaAs/SiN mode couplers.

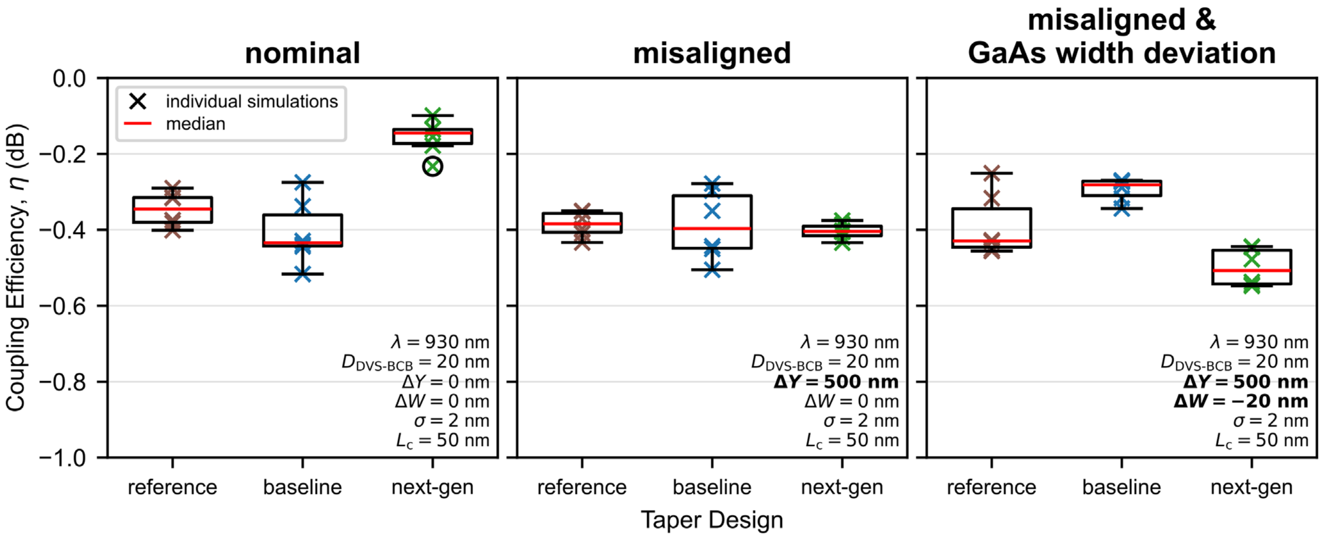

FIGURE 7 | Coupling efficiency of GaAs/SiN couplers extracted from realistic FDTD simulations including GaAs sidewall roughness and extreme systematic variations.

4 | Discussion

4.1 | Verification of Results

To additionally verify our taper optimization approach and confirm our treatment of width-dependent scattering losses, we performed FDTD simulations of the mode couplers with applied sidewall roughness (as seen in Figure 1). While these simulations can be performed for validation purposes, they are too computationally expensive to directly include in the optimization procedure. Extracted η is shown in Figure 7 for extreme cases of systematic variations from Figure 3. These correspond roughly to the measured largest ΔY (560 nm) and ΔW (−25 nm). Individual simulations involve different sidewall roughness profiles following the same roughness statistics (σ and L_c) as for taper optimization.

The extracted η for the reference and baseline tapers is similar, with a slight increase for the latter in the third variation case. In contrast, the next-generation taper exhibits substantially higher η in the first variation case due to lower scattering losses, but η decreases in the less probable second and third cases under extreme systematic variations. These trends are precisely in line with the results presented in Figure 3. The baseline design is more tolerant to extreme fabrication corners, whereas the next-generation design is more tolerant to propagation losses and smaller, more realistic fabrication variations.

Coupling efficiencies are slightly higher in simulations compared to the measurements discussed before. We suspect the main origin of this discrepancy stems from the difference between modelled (5 dB/mm at W_{GaAs} = 300 nm) and measured propagation loss (11 dB/mm at W_{GaAs} = 300 nm). This is likely due to a higher roughness RMS value (σ) than initially estimated—SEM analysis of sidewalls of the printed GaAs WGs indicated a value of ∼3 nm (3.2 nm ± 0.6 nm based on 16 sidewall samples) rather than 2 nm. This is also in line with earlier, detailed analyses of sidewall roughness and related scattering losses in the monolithic GaAs platform [23].

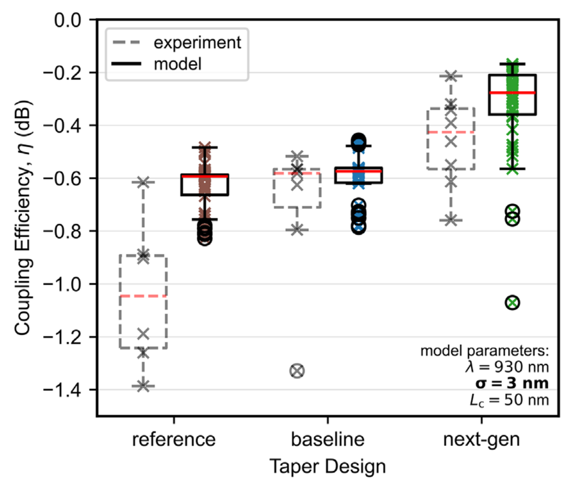

FIGURE 8 | Modelled coupling efficiencies of GaAs/SiN couplers for σ = 3 nm with measured coupling efficiencies shown for reference.

To further investigate this discrepancy and directly compare the taper optimization model with experimental results, Figure 8 shows the modelled η obtained from EME simulations combined with the propagation-loss model for σ = 3 nm, using experimentally measured values of fabrication variations. Experimental coupling efficiencies from Figure 6 are included for reference. The simulated results comprise 50 cases for each taper with misalignment and GaAs width deviation randomly sampled from the experimental data shown in Figure 4, and DVS-BCB thickness drawn from a uniform distribution in a 10–40 nm range (in line with fabrication data in the "Methods" section).

An excellent match between the measured and modelled η range is observed for the baseline and next-gen tapers. We suspect that the interference fringes in the measured transmission spectra are the primary cause of the mismatch in the reference taper case. Furthermore, we suspect that the remaining discrepancies of the medians and distributions can be attributed primarily to a limited experimental sample size, as well as possible additional

TABLE 1 | Comparison of reported GaAs/SiN coupler efficiencies.

η (sim.) [%]	η (meas.) [%]	λ [nm]	Coupling type	Integration technique	Fabrication tolerance	Reference
88–96	84–95	930	adiabatic	µTP	yes	this work
>95	82	930	adiabatic	µTP	yes	[25]
~98	63	970	resonant	µTP	no	[37]
99	43	940	resonant	µTP	no	[38]
<69	—	916	adiabatic	wafer bonding	no	[39]
—	65	930	adiabatic	die bonding	no	[24]

η variations caused by the stochastic nature of scattering losses (e.g., as seen in Figure 7). Additionally, for future work, further characterization of the DVS-BCB thickness variation could be of interest because a detailed assessment requires statistics from many device cross sections.

4.2 | Coupler Efficiencies in Literature

To place the performance of the next-generation taper in broader context, Table 1 shows a comparison with evanescent GaAs/SiN mode couplers reported in literature—including both adiabatic and resonant couplers (e.g., directional couplers), as well as µTP-based and other heterogeneous integration approaches. Since we target state-of-the-art ~930 nm QDs, and comparison across wavelength ranges is complicated by differing propagation losses, the best-performing couplers operating near this wavelength range are included.

While simulations often predict η approaching unity, a large gap between theoretical performance and experimental results has persisted. This is largely attributed to fabrication imperfections, which have limited experimentally demonstrated η to ~65% [24, 37–39]. Addressing the issue of fabrication tolerance by accounting for some variations, excluding sidewall roughness, has increased η to ~82% and partially reduced this gap [25]. By adopting a novel design methodology that systematically incorporates key fabrication variations and, critically, scattering losses, we further extend this boundary reliably beyond the 90% barrier and significantly narrow the gap between simulation and experiment. This improvement is enabled by the explicit inclusion of the relevant fabrication imperfections in a rigorous numerical taper design process together with detailed characterization of fabricated devices.

5 | Conclusion

In this work, we addressed the critical challenge of realizing low-loss, fabrication-tolerant mode couplers for heterogeneous QPICs. In particular, we investigated the optical transition between GaAs waveguides—essential for single-photon sources—and a low-loss SiN interposer. We introduced a fully numerical optimization framework for adiabatic mode couplers that directly incorporates all fabrication-variation corners. A key feature of our approach is the rigorous FDTD evaluation of sidewall-scattering losses in the hybrid GaAs/SiN structure, which revealed a strong dependence on GaAs waveguide width. These scattering losses, together with fabrication corners, were integrated directly into the optimization objective function, clearly distinguishing our approach from earlier work. This enables a streamlined design methodology for highly reliable and efficient couplers, capturing fabrication imperfections with unprecedented accuracy.

We experimentally validated the newly designed mode couplers and characterized the µTP-induced misalignment and GaAs waveguide width deviation statistics in fabricated devices, confirming the fabrication variations considered in the taper design. The optimized GaAs/SiN couplers yielded an insertion loss of −0.43 dB ± 0.14 dB, representing a substantial improvement over the reference design (−1.05 dB ± 0.2 dB). Crucially, these results bring the coupling efficiency reliably within the < 10% optical loss threshold demanded by advanced quantum applications—a benchmark that has been challenging to meet under realistic fabrication conditions.

Computationally expensive FDTD simulations of the full couplers with applied sidewall roughness validate our model, which shows close agreement with experimental results. This represents an important predictive accuracy improvement over previous approaches and confirms that the remaining coupling losses are now dominated by sidewall scattering. While future work might fine-tune the taper optimization weights slightly according to the measured distributions of fabrication variations, further improvement in efficiency will likely require either advancing GaAs fabrication processes to reduce roughness or transitioning to longer operational wavelengths—e.g., using O-band QDs [23, 40]. The latter would also enable wider taper tips and coupling to silicon, which is not transparent at 930 nm but has a much smaller refractive-index mismatch with GaAs, potentially relaxing fabrication tolerance constraints. More broadly, the fabrication-aware design strategy presented here can be directly translated to other material systems, representing a pivotal step toward reliable, next generation heterogeneous QPICs.

6 | Methods

6.1 | Taper Optimization

In our EME and FDTD simulations, we extracted the transmission of the TE_{00} mode from the SiN WG into the GaAs WG at a 930 nm wavelength. Transmission in the reverse direction is expected to be the same [41] (confirmed by simulations). The employed material refractive indices were approximately 1.45, 1.54, 2.00, and 3.48 for SiO_2, BCB, SiN, and GaAs [42], respectively. The first three values are standard refractive indices of these materials, and the last is the refractive index of GaAs at a temperature of 4 K. During taper optimization, where only segment lengths are varied, we performed efficient EME simulations based on pre-computed scattering matrices.

The systematic variations considered in taper design included ΔY (0–500 nm), ΔW (±30 nm), $D_{\text{DVS-BCB}}$ (0–60 nm), Δn_{GaAs} (±0.05), and Δn_{SiN} (±0.05). For the optimization of the baseline taper based on the objective function in Equation 1, we employed $M = 35$ variation cases, including the nominal case (no variations), two cases with misalignment ($\Delta Y > 0$) since this is the key variation caused by μTP, and all $2^5 = 32$ fabrication corners. Based on initial tests, we selected $C_T = 0.05$, $C_L = 50$ μm, and pre-normalization weights of 1, 1/4, and 1/32 for the nominal case, misalignment cases, and the fabrication corners, respectively. The optimization of the next-generation taper was based on the refined objective function in Equation 2, which evaluates a weighted generalized mean of optical losses across the considered variations. Here, we focused on more realistic variations considered in $M = 10$ cases, including the nominal case, one misalignment case, and $2^3 = 8$ fabrication corners. We excluded refractive index variations since we found that their impact is not significant. We employed the same pre-normalization weights as before, except using 1/8 instead of 1/32 for the fabrication corners, and we used a generalized mean exponent $p = 4$, increasing the impact of outliers (compared to exponent 2 in Equation 1) to ensure robust taper performance.

6.2 | Sample Fabrication

GaAs structures were defined with EBL and inductively coupled plasma etching on the μTP source chip as reported in [23, 35]. Tethers suspending the structures after wet etching of the underlying AlGaAs release layer were made of photoresist. In parallel, the SiN target was realized with EBL and reactive ion etching. All SiN and GaAs structures were completely contained within EBL write fields to avoid stitching issues. A 50 nm ± 20 nm DVS-BCB bonding layer was spin-coated on the SiN chip, with thickness confirmed through thin-film interferometry. Tapered GaAs waveguides were printed on designated sites guided by alignment markers and pattern recognition. The waveguides were printed into the DVS-BCB layer with the same pressure in all cases, resulting in a reduced DVS-BCB thickness under the transferred devices. Cross-section analyses of earlier samples indicate a thickness around 20 nm, with minimum and maximum observed thickness approaching 10 and 40 nm, respectively. Finally, the tethers were removed by a combination of chemical cleaning and reactive-ion etching, and the DVS-BCB layer was hard cured. Further details of the μTP procedure can be found in ref. [25].

For each GaAs taper design, 9–12 GaAs/SiN circuits were fabricated on 2 samples. The employed μTP procedure was still being optimized for these very long and narrow GaAs WGs while processing the first sample, resulting in a few devices being damaged. Due to extra care in the rinsing process, all 13 devices printed on the second sample remained intact. Therefore, 6–8 circuits were used for the optical characterization of each taper design. For measurement calibration, SiN circuits without printed GaAs WGs were defined throughout the chip and several meandered GaAs WGs with different lengths were additionally printed. These included 9 circuits with WG lengths between 0.17–1.86 mm, terminated by GaAs grating couplers.

6.3 | Optical Transmission Measurements

The optical transmission measurement setup consisted of a cryostat with an objective, free-space optics, and a supercontinuum laser and spectrometer interfaced through optical fibers. Using this setup, the free-space beams must be precisely aligned to grating couplers on the sample in the cryostat. Although the grating coupler layout was identical in all circuits, fabrication variations necessitated performing fine realignment for each circuit to achieve optimal coupling. Since there were several alignment parameters used (primarily the orientation of four mirrors and XYZ position of the sample), measurement conditions could drift slightly throughout the sample characterization process. Therefore, to ensure consistent measurement calibration, we alternated between measuring GaAs/SiN circuits under test and SiN calibration circuits. Initial measurements of 10 calibration circuits showed a ∼0.1 dB standard deviation at the grating coupler peak and a signal-to-noise ratio above 30 dB.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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