

Optical Degradation of 845 nm VCSELs With Different Oxide Apertures for Silicon Photonics

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Abstract—In this work, we analyzed the optical degradation of 845 nm VCSELs designed for silicon photonics (SiPh) applications as a function of the oxide aperture. First, we investigated the optical degradation in relation to the stress current. The experimental results showed that devices with a larger oxide aperture exhibit better reliability. From the analysis of the degradation kinetics, we found that the current at which the highly accelerated degradation process occurs depends inversely on the aperture radius. This result was explained by showing that devices with a larger aperture have lower thermal impedance, and therefore operate at lower internal temperatures at similar bias points. This interpretation is supported by isothermal constant current stress tests, which show that when the same internal temperature is maintained during ageing, for all VCSEL geometries under study the onset of degradation occurs at the same time. The equivalent activation energy of the degradation process was found to fall between 0.43 and 0.68 eV. Our analysis demonstrated that using a larger aperture can improve device reliability.

Index Terms—Degradation, silicon photonics, VCSEL, thermal impedance.

I. INTRODUCTION

IN RECENT years, data centers and computing applications have been experiencing bottlenecks in data transmission and

energy efficiency [1], [2]. Due to the limitations of electrical signals transmitted through copper wires, electrical transmission has largely been replaced by optical communication for long-haul transmission. However, this shift has not yet been implemented for short-range communications (i.e., board- and chip-level data communications) due to the cost and size of optical transceivers. Silicon photonics (SiPh) aims to bridge this gap by providing highly scalable and low-cost optical devices [3].

To achieve this goal, SiPh leverages the standard CMOS process to fabricate all the required photonic components, except for laser diodes. Due to its indirect bandgap, silicon is not suitable as an optical source [4]. Instead, III-V materials such as GaAs and InP are employed to develop IR sources. Nonetheless, the material mismatch between the substrate (silicon) and the active materials results in poor material quality [5], [6], [7] that lead to suboptimal optical performance and short-lifetime lasers. In the last two decades, various alternatives to the direct growth of III-V layers onto silicon have been proposed. The most common approaches include flip-chip integration [8], bonding [9], and, more recently, micro-transfer printing [10], which has recently gained significant momentum. Micro-transfer printing involves picking up a pre-processed device coupon from a source wafer, which is then printed onto the host photonic integrated circuit (PIC) wafer using a stamp [11]. Consequently, III-V devices do not exhibit extended defects due to materials mismatch.

The most common laser diodes integrated in PICs are edge-emitting devices such as Fabry-Pérot (FP), Distributed Bragg Reflector (DBR), and Distributed Feedback (DFB). These lasers all have extended planar cavities and exhibit relatively high threshold currents, ranging from 10 to 100 mA. In short-reach communications, such as in data centers, there are strict requirements in terms of energy consumption [12]. The most promising optical sources for high-speed, low-power communication are the vertical-cavity surface-emitting lasers (VCSELs). Compared to other types of lasers, VCSELs offer high-throughput wafer-level testing, easy interfacing with optical fibers, and, most importantly, sub-mA threshold currents and high slope efficiencies, making them excellent candidates as light sources for PICs [13]. In the past few years, several studies have addressed the degradation modes of infrared VCSELs [14], [15], [16]. However, there is a lack of studies on photonic integrated

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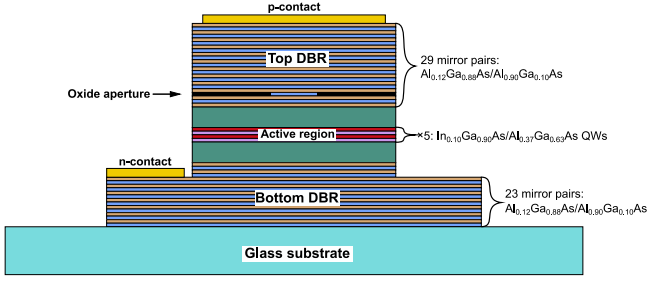


Fig. 1. Cross-sectional schematic of the VCSEL structure used in this work.

lasers, which could suffer from higher thermal impedance due to integration on silicon-on-insulator (SOI) or other thermally insulating platforms. To fill this gap, in this paper we investigated the optical reliability of 845 nm VCSELs suitable for integration into SiN platforms for silicon photonics [17], [18] with a new set of experiments testing devices with different oxide aperture. The oxide aperture diameter is a key design parameter in VCSELs, as it directly affects the threshold current, series resistance, and optical mode profile. In general, larger oxide apertures reduce the resistance and thermal impedance, leading to lower internal temperatures during operation for a given current, but potentially bring the device into potential multi longitudinal modes operation [19]. However, the aperture size also influences device reliability: a lower thermal impedance slows down temperature-activated degradation processes, such as impurity diffusion, which ultimately limits the device lifetime. Therefore, for VCSELs the choice of oxide aperture involves a trade-off between optical performance and long-term reliability.

Firstly, we studied optical degradation using current step stress and constant current stress experiments on devices with three different apertures (4, 5, and 6 μm). Then, we evaluated the thermal impedance of the three geometries through pulsed measurements. Finally, we repeated the constant current experiments for the 4 μm aperture lasers at different ambient temperatures to determine the activation energy of the main degradation process.

Based on the experimental results of our study, we demonstrate that i) in devices with larger aperture, the onset of high-accelerated degradation occurs at higher currents; ii) this feature is directly related to the lower thermal impedance, which decreases with increasing diameter; iii) the onset of critical threshold current increase is thermally-activated, with an activation energy of 0.43 to 0.68 eV.

II. DEVICES UNDER TEST

The devices analyzed within this work are vertical-cavity surface-emitting laser diodes emitting at 845 nm. The structure (Fig. 1), starting from the top, includes a Ti/Pt/Au disk-shaped p-contact that serves both as electrode and as a top reflector. The top DBR is p-doped with carbon and consists of 29 mirror pairs of $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}/\text{Al}_{0.90}\text{Ga}_{0.10}\text{As}$. At the bottom of the p-DBR, within the layer closest to the separate confinement heterostructure (SCH) region, a 30-nm $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ layer is included. This layer enables the formation of a 4–6 μm oxide aperture through selective wet oxidation. The presence of this aperture laterally confines the current, and consequently the

optical mode to the center of the circular VCSEL structure. The active area of the laser is located below the aperture and consists of a $1 - \lambda$ thick SCH and a multi-quantum-well (MQW) structure containing five 4 nm thick $\text{In}_{0.10}\text{Ga}_{0.90}\text{As}/\text{Al}_{0.37}\text{Ga}_{0.63}\text{As}$ QWs. The bottom DBR is n-doped and is composed of 23 mirror pairs of $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}/\text{Al}_{0.90}\text{Ga}_{0.10}\text{As}$. A Ni/Ge/Au n-contact is positioned a few DBR mirror pairs below the active volume. At the bottom of the n-DBR, a 527 nm $\text{Al}_{0.12}\text{Ga}_{0.88}\text{As}$ buffer layer is purposely included to tune the cavity length between the bottom DBR and the substrate, which is supposed to include a diffraction grating in the final application [13]. Underneath this layer, a 4 nm GaAs layer serves as an etch stop layer with respect to an $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ sacrificial layer, which is required for the micro-transfer-printing process. Further information regarding the device epitaxy, growth, and fabrication can be found in [21]. The devices are meant to be transferred onto a SiN platform, thus allowing the fabrication of vertical-cavity silicon-integrated lasers (VCSILs) [21]. The samples analyzed in this work were transferred onto a glass substrate to characterize the optical emission from the bottom side.

The glass substrate not only enables bottom-side characterization, which is useful from a research and a diagnostic perspective, but also has a refractive index similar to that of SiO_2 , leading to minimal perturbation of the optical mode compared to the target application on SiN platform.

III. METHODOLOGY

To measure the optical degradation of the devices, we tested representative VCSELs with 4, 5, and 6 μm oxide apertures. The samples were aged and characterized at a fixed temperature using a source meter. The temperature control was maintained by a TEC-controlled baseplate.

First, to evaluate degradation as a function of the stress current, the devices were submitted to a current step stress experiment.

In this aging test, the stress current was increased by 50 μA every hour, starting from 50 μA . After each stage of the step-stress, an optical characterization (L-I) was performed.

To evaluate the degradation kinetics over time, the devices were then subjected to a constant-current stress experiment. The aging test was interrupted at various stages to evaluate the effect of device degradation by performing L-I characterization. In this work, we analyze the results of various current stress tests carried out up to 7 mA.

Regarding the measurement of the thermal impedance, we employed a pulsed setup to map the device internal temperature following Xi's forward voltage method [20]. To this aim, we applied square waveforms featuring 2 μs pulse width and a repetition period of 1 ms, resulting in a 0.2% duty cycle to minimize device self-heating. The results of these analyses are reported in the following section.

IV. OPTICAL DEGRADATION

A. Current Step-Stress Results

During the current step-stress test, we recorded the L-I characteristics every hour before increasing the stress current by

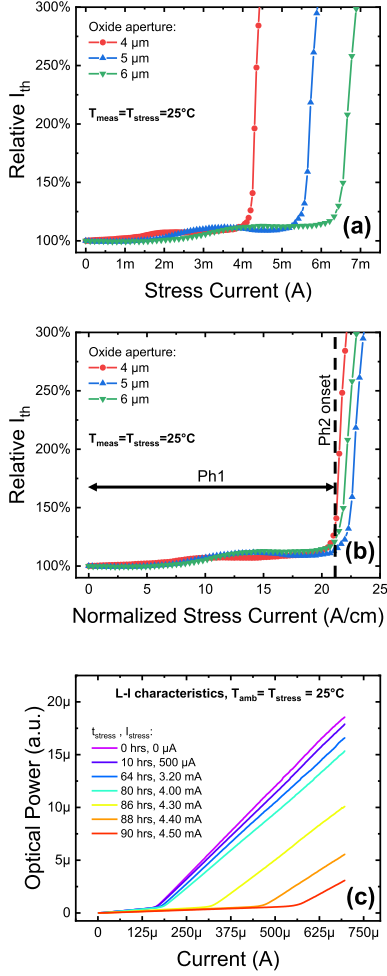


Fig. 2. (a) Relative threshold current kinetics for three different geometries (4, 5, and 6 μm oxide aperture width) during a current step-stress experiment (b) the stress current was normalized for the oxide radius. The graph shows that the onset of Ph2 degradation process is related to the oxide aperture width. (c) Representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the current step-stress experiment.

50 μA . This experiment was carried out for all device geometries under investigation (4, 5, and 6 μm oxide apertures). From the experimental data, we extracted the degradation kinetics of the threshold current (I_{th}) as a function of the stress current (Fig. 2(a)). Each curve exhibits two distinct phases: initially, I_{th} shows a mild degradation (an overall 10-15% increase), referred to as Ph1. This is followed by the onset of a second, faster degradation process, indicated as Ph2. The degradation process observed in the devices under investigation has been previously reported. In particular, in [17] we demonstrated that, regardless of the final substrate [18], devices based on such III-V epitaxy are affected by the diffusion of impurities, which initially move across the top DBR, causing a limited worsening in optical performance (Ph1). Subsequently, when these impurities reach the active region, they lead to significant optical degradation (Ph2).

By looking at the kinetics, we can see that the 6 μm aperture device shows the onset of Ph2 at higher currents (≈ 6.5 mA) compared to the other two devices (≈ 5.5 mA for the 5 μm aperture

and ≈ 4 mA for the 4 μm aperture device). Generally speaking, these results indicate that, for comparable operating current levels, devices with larger diameters have better reliability. To investigate the origin of these results, we normalized the stress current of the three devices by the radius of the oxide aperture, obtaining degradation kinetics as a function of the stress current per unit length (A/cm). The outcome of this normalization is shown in Fig. 2(b): remarkably, now the three degradation curves are nearly superimposed, and, in addition to that, the onset of Ph2 occurs at the same current per unit length (i.e., ≈ 21 A/cm). Fig. 2(c) shows representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the current step-stress experiment, from which the threshold current kinetics were extracted. Noticeably, the relative variation in threshold current is stronger than the change in slope efficiency. In order to look for correlation between device geometry and specific driving forces of the ageing process, we decided to evaluate device temperature in the three different scenarios, first. To do this, we leveraged the expression for the VCSELs' thermal impedance, R_{th} [22]:

$$R_{th} = \frac{1}{2\xi S} \quad (1)$$

where ξ is the material's thermal conductivity and S is the device diameter. This formula was derived by considering the 3D heat flow from a disk-shaped heat source of diameter S on a half-space. Therefore, it is valid for a small-diameter VCSEL mounted on the top side of a relatively thick substrate, as in our case. Equation (1) shows an inverse dependence on the aperture radius, as indicated by normalized degradation kinetics in Fig. 2(b)). Based on this observation, we hypothesize that the onset of Ph2 (and consequently the degradation) depends on the thermal impedance of the devices, i.e., to its operating temperature. Since the degradation phenomena are related to a diffusion process, it is reasonable to assume that the internal temperature plays a fundamental role in determining the speed of the degradation process. To confirm this, we measured the thermal impedance of the three devices to figure out the dependence of this quantity with respect to the aperture radius.

B. Thermal Impedance Measurement

To probe the internal temperature, we measured the voltage drop across the device over short time periods at specific currents and temperatures. Details on the method used to assess the thermal impedance can be found in [20]. To determine the dependence of the voltage drop on temperature, we measured this quantity before the device began self-heating. For this purpose, we employed a voltage pulser to apply short pulses (≈ 2 μs) to observe the voltage drop before it decreases due to the rise in internal temperature. To limit self-heating, we set a pulse repetition period of 1 ms (the maximum allowed by the instrument), resulting in a duty cycle of 0.2%. Under this configuration, we can assume that the measured voltage drop, V_j , can be directly related to the internal temperature $T_j = T_{amb}$ (where T_{amb} is the baseplate temperature). We decided to map the currents between 1 to 4 mA over the 20–70 $^\circ\text{C}$ range. The results of the thermal maps for the 5 μm aperture

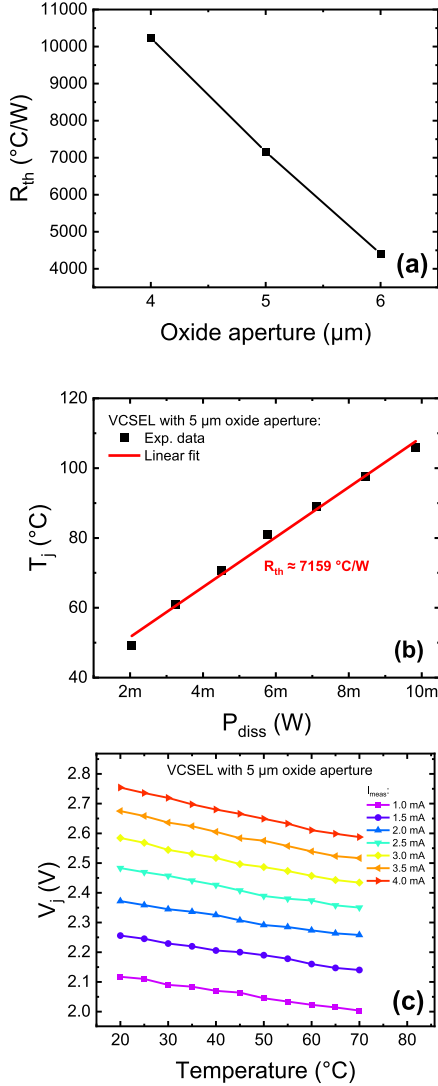


Fig. 3. (a) Dependence of thermal impedance on the oxide aperture. The trend appears to represent a linear approximation of a $1/r_{ox}$ function. (b) Extrapolation of R_{th} from junction temperature estimation for different dissipated power values (4 μm oxide aperture VCSEL). (c) Thermal map extrapolated for seven currents (from 1 to 4 mA) in a 5 μm oxide aperture VCSEL.

device are shown in Fig. 3(c)). Subsequently, we recorded the CW voltage drop after internal temperature stabilization for the same set of currents. These measurements were carried out at $T_{amb} = 25^{\circ}\text{C}$ (i.e., equal to T_{stress}). By comparing the steady-state voltage drops after the thermal transients (caused by the device's self-heating) with the previously calculated thermal maps, we determined the internal temperature T_j by fitting the experimental data. Finally, to calculate the thermal impedance R_{th} , we extrapolated the corresponding dissipated power, P_{diss} , for each current:

$$P_{diss} = P_{el} - P_{opt} = V_j^{CW} \times I - P_{opt} \quad (2)$$

Equation (2) shows that the dissipated power, P_{diss} , is determined by subtracting the emitted optical power, P_{opt} , from electrical power, P_{el} , which is the product of the current (I)

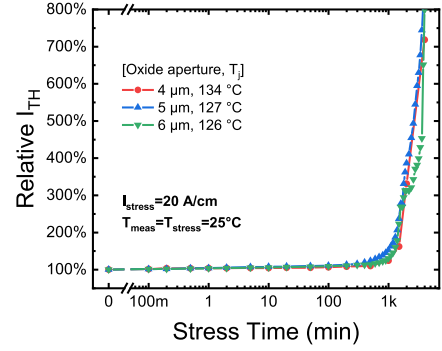


Fig. 4. Threshold current kinetics for constant current stress experiments carried out at 20 A/cm (i.e., for the current normalized by the aperture radius). The outcome of the aging test confirms that the degradation of the devices depends on the oxide aperture.

and the CW voltage drop (V_j^{CW}). Fig. 3(b)) shows the T_j vs. P_{diss} graph for the 5 μm aperture device, from which a thermal impedance of about $7 \cdot 10^3^{\circ}\text{C/W}$ was calculated. The numerical results of the R_{th} for the three devices are consistent with previous reports on VCSELs [23]. We eventually compared results for the three geometries under test (Fig. 3(a)), confirming that the thermal impedance decreases with increasing the aperture diameter. This feature can be physically explained by noting that the oxide aperture confines the current within the III-V stack. In VCSELs with a larger aperture, the current density is distributed over a larger volume. Consequently, power is dissipated over this larger volume, resulting in a lower internal temperature. A 2D simulation of current density distribution across a similar VCSEL stack is illustrated in [18].

C. Constant Current Stress Results

Based on the results of the current step stress experiments, we hypothesized that the speed of the degradation process (impurity diffusion) depends on the internal temperature of the devices. Since the thermal impedance is inversely related to the aperture radius, we conducted the constant current stress tests with the same current per unit length to ensure that the experiments were carried out at similar internal temperatures, T_j . To observe the worsening of the threshold current within a reasonable time period (≈ 5 kmin), we selected a stress current of 4 mA for the 4 μm aperture device based on our previous results [17]. This stress current corresponds to 20 A/cm (i.e., 4 mA normalized to a radius of 2 μm), which means that the 5 μm aperture device will be stressed at 5 mA, and the 6 μm aperture device at 6 mA.

The experimental results shown in Fig. 4 indicate that the devices exhibit the same degradation kinetics, confirming our hypothesis on the role of internal temperature in the diffusion process. The legend in the graph indicates the T_j calculated from the resulting R_{th} obtained in Section IV-B. The calculated internal temperatures are approximately 130 $^{\circ}\text{C}$. Minor differences between the three temperatures may arise from the fact that the thermal maps presented in Section IV-B were based on experimental measurements carried out between 20 $^{\circ}\text{C}$ and 70 $^{\circ}\text{C}$. Consequently, the estimated T_j values, which exceed the

experimental range of mapping, suffer from a certain level of uncertainty.

D. Constant Current Stress Results: Temperature Dependence

In this section, we report the results of constant current stress tests carried out at fixed stress current for various temperatures. We chose to test the 4 μm aperture device with a stress current of 3.5 mA ($\approx 27 \text{ kA/cm}^2$) at $T_{\text{stress}} = 40, 55$, and 70°C . The 3.5 mA stress condition used for the 4 μm oxide aperture VCSEL is about 20 times its threshold current ($\approx 180 \mu\text{A}$, see figure Fig. 2(c)) and lies well beyond the thermal rolloff point. Such high current densities are not relevant for practical operation, but they are useful from a reliability perspective because they accelerate degradation and allow Ph2 failure mechanisms to be observed within a reasonable experimental timeframe. The degradation kinetics of I_{th} are shown Fig. 5(a). Clearly, the onset of Ph2 occurs at shorter stress times as the baseplate temperature, and consequently, the internal temperature, is increased.

To better illustrate the impact of temperature on the degradation rate, we built an Arrhenius plot of the time-to-failure (TTF), defined as the time required for the aging procedure to increase the initial threshold current of the device by specific amounts: 25%, 50%, and 75%. The resulting Arrhenius plot is shown in Fig. 5(b). Depending on the failure criterion considered, the resulting activation energy ranges from 0.43 to 0.68 eV. The observed spread in activation energy reflects the limited statistical sampling in this study. Nevertheless, the data unambiguously show that higher temperatures accelerate the onset of Ph2 degradation, consistent with a thermally activated process. For a representative visualization of the device degradation during this experiment, Fig. 5(c) shows the evolution of the L-I characteristics collected throughout the constant current stress test. The trends of threshold current and slope efficiency are analogous to the ones discussed for Fig. 2(c).

V. CONCLUSION

In summary, we analyzed the reliability of 845 nm VCSELs for silicon photonics featuring three different widths of the oxide aperture, by means of accelerated aging experiments. First, we examined the optical degradation of the devices as a function of the stress current through current step stress experiments. As the oxide aperture increased, the devices demonstrated improved reliability with respect to the stress current. The experimental curves revealed a dependence of the second (main) degradation phase on the stress current normalized by the aperture radius, leading us to hypothesize that degradation is influenced by the internal temperature of the devices. To confirm this hypothesis, we measured the thermal impedance using pulsed characteristics, and determined that its value decreases with increasing oxide aperture diameter, approximately following a $1/r_{\text{ox}}$ relation. Additionally, a constant current stress experiment carried out at 20 A/cm, to maintain the same internal temperature across all three devices, verified our hypothesis by showing that the Ph2 onset occurs at the same stress time for all three geometries. Finally, additional stress tests carried out at different T_j allowed

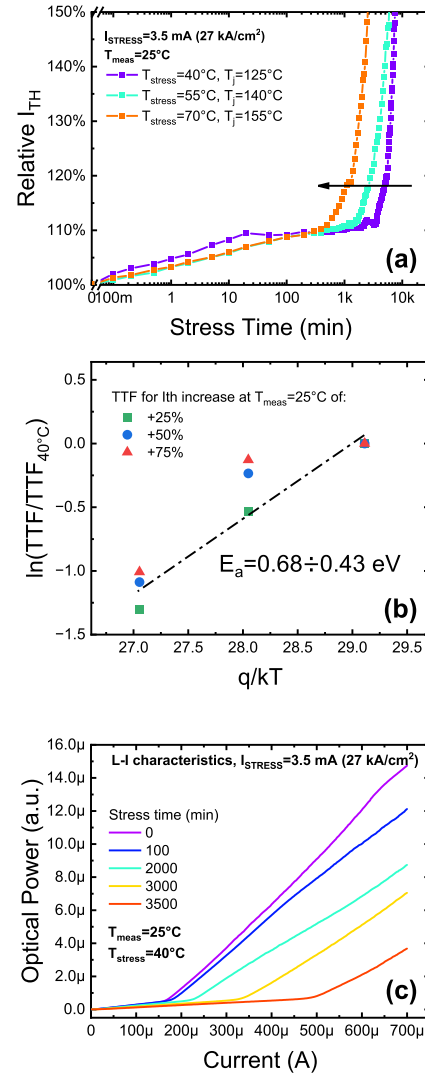


Fig. 5. (a) Constant current stress results at 3.5 mA for different stress temperatures (40, 55, and 70°C): The Ph2 onset is activated for shorter stress time at increasing operating temperature. (b) Arrhenius plot extrapolated for three different TTF conditions: +25%, +50%, and +70% degradation of the I_{th} . The resulting activation energy hovers between 0.43 eV and 0.68 eV. (c) Representative L-I characteristics of the 4 μm oxide aperture VCSEL collected during the constant current stress experiment.

us to identify the thermal activation energy of the main optical degradation, which falls within the 0.43 to 0.68 eV range.

The reported data ultimately demonstrate that VCSELs featuring larger apertures exhibit higher optical reliability. This improvement is closely related to the resulting thermal impedance: as the oxide aperture increases, the thermal impedance decreases, which in turn reduces the internal temperature during stress for the same current. This is beneficial for reliability because a lower internal temperature slows the diffusion process that eventually causes the severe optical degradation occurring for longer stress times. However, the choice of oxide aperture affects not only the thermal impedance but also the threshold current, series resistance and the optical behavior of the laser diode. This indicates the presence of a tradeoff between performance and reliability.

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