Photonic Ising node in a programmable wavelength-division multiplexing silicon photonic integrated circuit

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We propose a scalable, energy-efficient photonic Ising node architecture using spontaneous symmetry breaking (SSB) in coupled silicon photonic nonlinear microrings. Compared to bulky, high-power implementations using OPOs [1] or SLMs [2], our integrated design achieves a much lower power threshold. We use programmable heaters to compensate fabrication errors and demonstrate an SSB threshold of ~2.1 mW in the bus waveguide, substantially outperforming the state-of-the-art [3]. This material-agnostic blueprint supports diverse nonlinearities and wavelength-division multiplexing (WDM) for parallelism, providing a foundation for low-power, large-scale probabilistic optical computing. Fig. 1(a) shows the Ising node schematic, consisting of a 50/50 MMI splitter and n pairs of coupled nonlinear microrings with distinct wavelengths. The top-right inset depicts a single pair: amplitudes a_1 and a_2 in the upper/ lower rings, couple to bus waveguides (coefficient d) and to each other (coefficient κ). (b) Microscope image of the fabricated device with 6 ring pairs.

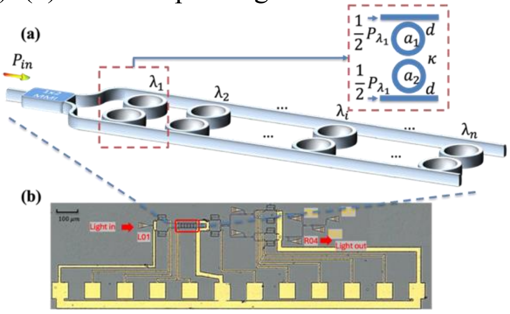

Figure 1: Photonic Ising node device in programmable photonic integrated circuit. (a) WDM coupled ring schematic and (b) microscopic picture of the chip.

Fig. 2 characterizes the onset of SSB by measuring the power of the anti-symmetric mode. A zero output baseline indicates a preserved symmetric state. The results validate the SSB power thresholds for both supercritical and subcritical pitchfork bifurcations. Additionally, the response of two resonator pairs shows SSB can be induced at multiple wavelengths concurrently, confirming the chip's parallel operation capability.

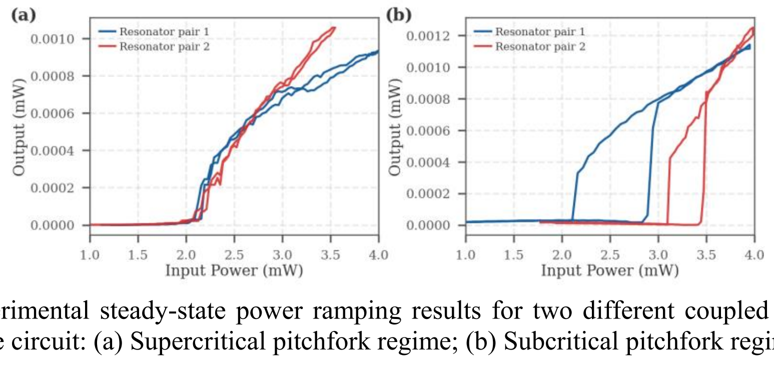

Figure 2: Experimental steady-state power ramping results for two different coupled resonator pairs within the same circuit: (a) Supercritical pitchfork regime; (b) Subcritical pitchfork regime.

We plan to conduct high-speed experiments to leverage other optical nonlinearities inherent in the silicon circuit. Additionally, we aim to scale the architecture into a fully integrated on-chip Ising machine, connecting multiple nodes to solve hard optimization problems.

[1] T. Honjo et al., Sci. Adv. 7 (2021), eabh0952.
[2] J. Ouyang et al., Commun. Phys. 7 (2024), 168.
[3] Y. Rah and K. Yu, Phys. Rev. Research 6 (2024), 013234.