Nano-opto-electro-mechanical phase shifter integrated in silicon photonic circuits and fabrication methods

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A silicon photonic integrated MEMS-based optical phase shifter is proposed to overcome the limitations of the conventional thermo-optic phase tuners using local heaters. Device concept, fabrication process and first experimental results are presented.

I. Introduction

Silicon photonics explores and applies optical systems through CMOS-compatible fabrication techniques, emerging as the leading solution to increase bandwidth in telecom and datacom networks. Today, standardized silicon photonics technology platforms offer electro-optical actuators with low loss and a compact footprint with the conventional phase shifters relying on thermo-optic tuning, where the injected current passes through a resistive heater placed beside an optical waveguide and generates heat that alters the material's intrinsic refractive index. Nonetheless, their scalability is constrained by high power consumption (up to tens of milliwatts per switch) and limited integration density of active components, imposed by thermal crosstalk between neighboring components. Micro-electro-mechanical systems (MEMS) can simultaneously overcome these limitations: by mechanically changing the waveguide geometry, they allow for short switching times ($\sim$ 1 μs) without cross-talk and nearly zero static power consumption for their electrostatic actuators, keeping low optical loss and footprint comparable to the heaters [1]. Being silicon-compatible, MEMS leverage the mature processes of platformed flows and enable continuous scaling of silicon photonic circuits, although they are still limited in performance by the high actuation phase shift voltage, on the order of 10 V [2]. Furthermore, the existing approaches always result in un-sealed cavity, preventing the phase shifter to be encapsulated by dielectric material and to continue the back-end-of-line (BEOL) processes. Here, a new process flow is proposed to achieve compact actuator in a sealed cavity. This scheme with vertical integration replaces the state-of-the-art horizontal approach and leads to device miniaturization, whose potential impact is also to reduce the driving voltage down to 2 V.

II. Device concept

Figure 1 presents the cross-sectional view of the proposed integrated nano-opto-electro-mechanical (NOEM) phase shifter, which consists of a suspended beam positioned above an optical waveguide. The beam features a heavily doped poly-silicon core that forms a capacitor with the heavily doped crystalline silicon patch beneath. The operating principle is as follows: the beam functions as a cantilever, deflecting in response to electrostatic forces induced by an applied voltage across the capacitor. As the cantilever approaches the waveguide, the effective refractive index of the propagating light increases, resulting in a phase shift. Preliminary optical simulations were performed for this NOEM phase shifter integrated on a 180° third-order polynomial interconnected circular (TOPIC) bend [3]. The NOEM phase shifter configuration includes a poly-silicon thickness A = 100 nm, a cantilever protection oxide thickness C = 15 nm, and a cantilever-waveguide gap B = 100 nm. As illustrated in Fig. 2, the cantilever tip displaces 78 nm toward the waveguide under a driving voltage of 17.48 V, yielding an optical phase shift of 1.31 rad. Further simulation results indicate that the pull-in voltage decreases with reductions in both the cantilever thickness (A+2C) and gap B. Consequently, the objective of this work is to develop a fabrication process capable of producing a thin cantilever with a minimal gap to the waveguide reliably.

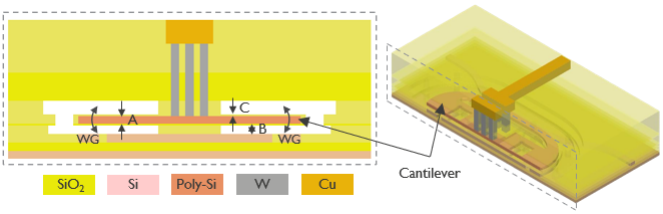

Fig. 1. Cartoon of the proposed NOEM phase tuner integration in silicon photonic flow. The poly-Si cantilever (A), protected by a thin silicon oxide liner (C), is placed above the silicon waveguide and separated by bottom gap (B). Metallic contacts reach the cantilever to induce the electrostatic force.

III. Process flow

The fabrication of the current configuration of the NOEM phase shifter (Fig. 1), integrated in silicon photonic flow with BEOL processes [4], starts with 300mm silicon-on-insulator (SOI) wafer, where the top Si layer is patterned and doped to form the waveguide. The bottom sacrificial layer, the cantilever and the top sacrificial layer are, respectively, deposited, patterned and planarized. Poly-Si is chosen as

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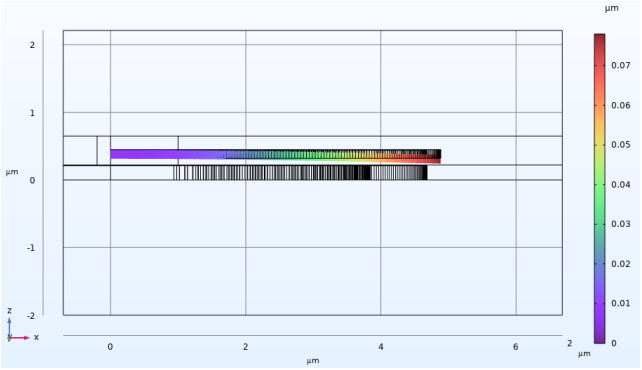

Fig. 2. The simulated cantilever's displacement.

both cantilever and sacrificial material because of the very high selectivity of the available etching process towards the dielectric stack above the device. To separate the mechanical beam from the outer regions, a thin SiO_2 protective layer is used for encapsulation. The next step consists of the opening of chimney holes that reach the sacrificial material and removing the exposed poly-Si by isotropic SF_6 dry etch, targeting very high selectivity (>1:300) toward the oxide material, ensuring correct protection of the cantilever. After that, the chimneys are sealed with thick oxide deposition to create the closed cavity. Tungsten contacts and copper lines are added, connecting the phase modulator to the external environment.

IV. Results

The first experiments have been conducted on 300 mm bulk Si short loop wafers to assess the critical process steps and capture the mechanical behavior of the cantilever without external perturbations. Thicknesses of poly-Si cantilever and bottom gap were set 160 nm, upper gap 200 nm and SiO_2 cantilever's protective liners 40 nm, deposited with plasma-enhanced atomic layer deposition (PEALD) technique. SF_6 dry Si etch was optimized in several process iterations with increasing etching times (from 300 s up to 1200 s) to achieve desired lateral undercut (>1.5 μm) and smooth oxide surfaces without residues (Fig 3). Minimal oxide recess (<5 nm) is detected during the sacrificial material's removal, demonstrating high selectivity of the etching process. The chimney sealing was tested with a DOE of dielectric combinations, ranging from physical-vapor-deposition (PVD) to plasma-enhanced chemical vapor deposition (PECVD) oxides at different temperatures (250°C, 370°C), resulting in PVD technique to have better non-conformal deposition compared to PECVD, but slower sealing rate. Combining first 100 nm PVD SiO_2 with thicker (>1 μm) PECVD SiO_2 is the option selected for our wafers. Mechanical stability of the cantilever can be studied at this stage with inline and out-of-line methodologies, provided that the ideal response is to stay flat when there is no driving voltage applied. Interferometric measurements are carried out by using coherent white light source to estimate the cantilever's deflection, and the results indicate that the beam is consistently bending upward because of materials intrinsic stress (Fig 4). Maximum deflection values stay below 150 nm for cantilever lengths of 4.7 μm ($\sim$ typical device dimension), proving that a 200 nm top gap can prevent the beam to stick to the upper cavity. Further investigation is required to better formulate the model and tune the cantilever's materials and thicknesses to compensate the intrinsic stress and minimize its displacement.

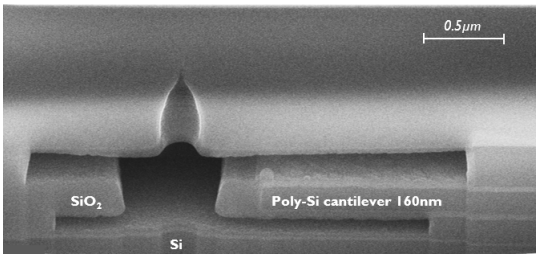

Fig. 3. Inline CrossSEM image of a test structure from short loop wafer. 160 nm poly-Si cantilever is released and suspended inside the sealed cavity.

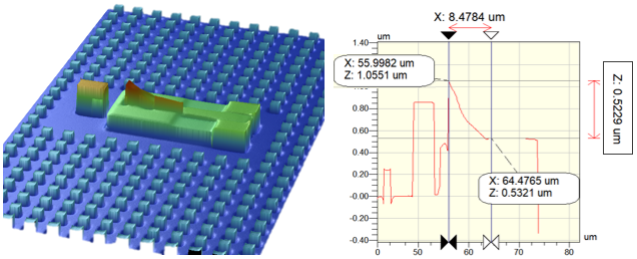

Fig. 4. Out-of-line interferometry measurements on a test structure with free-standing 8.7 μm cantilever's length to estimate the deflection before the cavity formation.

V. Conclusion

This work introduces a NOEM phase shifter with nearly zero static power consumption and low optical loss integrated into silicon photonics. The innovation lies in the small MEMS-based device dimensions that allow for encapsulation with vertical integration and CMOS-compatible actuation voltages. The presented experimental results on the short loops are promising for the full device vehicle under fabrication.

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