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General-Purpose Hexagonal Programmable Photonic Integrated Circuit with a >30 GHz Free Spectral Range

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ABSTRACT

A programmable photonic circuit is demonstrated based on a 7-cell hexagonal waveguide mesh of 2 × 2 Mach–Zehnder interferometer gates. Benefiting from undercut heaters, the optical gates have a small insertion loss of 0.28 dB/gate and a short optical delay of 5.5 ps, which results in a compact circuit with a large free spectral range (FSR) of 31 GHz for a 6-gate ring resonator. We demonstrate the advantages of this circuit through the applications of beam splitters, wavelength multiplexers, and wavelength filters. To enable a larger FSR, Vernier rings and a dual-injected ring configuration can be constructed, showing an improved FSR of 93 GHz.

1 | Introduction

Benefiting from the maturity of industrial CMOS technology, silicon photonic integrated circuits (PICs) are widely used in many applications such as data communication, sensing, and information processing, steadily growing in the number of building blocks and the complexity of the functionality. To accelerate the research and development (R&D) process of these PIC applications, there is a need for development tools to rapidly prototype new functionalities without going through a time-consuming foundry fabrication process. Such a tool would play a similar role as field-programmable gate arrays (FPGAs) in programmable digital electronic hardware. In the past decade, a new kind of programmable PICs [1] has emerged, consisting of optical networks of on-chip waveguides in which the optical paths can be rearranged using tunable couplers and phase shifters. This way, the functionality of the PIC can be altered in software via a layer of electronics.

The performance of a PIC is often susceptible to fabrication variations, so active tuners are commonly used to compensate for the imperfections in the PIC, or to tune the transmission response. Programmable PICs take this one step further and use the active tuners to fully configure the circuit's functionality. One particular class of such programmable circuits is implemented in the recirculating mesh architecture [2–4], in which the optical gates are arranged in a loop-shaped topology. In this way, a variety of functions, such as optical distribution networks and wavelength filters with Mach–Zehnder interferometers (MZIs) or ring resonators, can be programmed into this generic photonic circuit. Similarly to FPGAs, this can be extremely beneficial for accelerating the development of new PICs [5].

As they are more generic, such recirculating mesh circuits have a larger footprint than the typical application-specific PICs, and the light will travel through a much longer optical path as it passes many more individual building blocks. Therefore, the

optical gates should perform well on different characteristics, by having low crosstalk, low insertion loss, and low electrical power consumption. Moreover, they need to have a short optical length, to be compact enough to enable interferometric optical filters configuration with a large free spectral range (FSR).

In this paper, we describe a programmable PIC based on the hexagonal recirculating waveguide mesh topology, which has a compact structure thanks to optical gates with a short optical delay and a low insertion loss. As the performance of the individual gate determines the maximum scale of the circuit, our optical gate implementation will be beneficial for many applications requiring a large-scale configuration or a large FSR. To show the advantages of our circuit, we experimentally demonstrate different optical functions, such as a 1×8 optical splitter, a three-channel wavelength multiplexer, an MZI lattice interleaver, and a tunable band-pass filter with two coupled rings. To apply these in real applications, the FSR of the wavelength filters is a main limitation. In this paper, we experimentally demonstrated two configurations with 3× the FSR of a single ring cell: a Vernier ring filter and a dual injection ring filter, with which the total FSR can be boosted to 93 GHz.

2 | Circuit

Shown in Figure 1a, our programmable PIC is constructed in a mesh structure with seven hexagonal cells, with one optical gate on each edge of a hexagonal cell. The layout of this circuit is shown in Figure 1c. This circuit consists of 42 optical gates in total, where each optical gate is implemented as a balanced-arm MZI as shown in Figure 1b. The MZI itself is constructed by two multi-mode interferometers (MMIs) with a thermo-optic phase shifter in both arms, bringing the total to 84 actuation tuners. The thermo-optic phase shifters are implemented as doped silicon phase shifters using local undercut. This chip is fabricated in IMEC's iSiPP200 process, and the fabricated chip is shown in Figure 1e. By delivering electrical power to the two phase shifters in each gate, the phase response θ_1 and θ_2 on the two arms of the MZI can be shifted. In this way, both intensity and phase response of the MZI optical gate can be tuned. The power coupling ratio of the gate can be fully altered between 0 (bar state) and 1 (cross state) by tuning the differential phase $\Delta\theta = \theta_1 - \theta_2$ of the two phase shifters in each gate, while the phase response of the gate is also tunable by simultaneously driving the common phase $\theta_c = (\theta_1 + \theta_2)/2$ of both phase shifters in each gate.

To ensure the structural uniformity of the circuit, the connecting waveguides between each pair of gates have the same optical length. Each hexagonal cell has the same number of connecting waveguides with the same number of optical bends, which will result in an equivalent round-trip loss for different hexagonal cells. The circuit has 24 optical input/output ports, which are accessible via a fiber array connected through grating couplers, as shown in Figure 1d. The bond pads of the phase shifters are wire-bonded to a printed circuit board (PCB) and connected to a multi-channel current driver. To program the circuit's functionality, a Python software library is used to define the circuit configurations, visualize the schematics, and control the multi-channel current driver to deliver the desired electrical power to the targeted optical gates on the chip [6].

3 | Measurement

To conveniently access the 24 optical ports of the circuit and take measurements, an optical switch (Polatis 6000i) connects the fiber array of the packaged programmable circuit with different measurement instruments, such as a wavelength tunable laser (SANTEC TSL-550), a power meter (HP 81532A), and an optical vector analyzer (LUNA OVA 5000). The driving currents for the phase shifters in the programmable PIC are delivered from a home-made multichannel current source. The optical circuit is placed on a temperature controller (TEC) to maintain a stable ambient temperature. All the instruments are automatically controlled by the Python script from a computer. The whole schematic of the measurement setup is shown in Figure 2. With this measurement setup, the programmable PIC can be programmed, and the optical transmission or the frequency response between any two ports of the circuit can be measured.

Ideally, the initial state of the balanced arm MZI is a perfect cross state, and the thermo-optic phase shifters have the same electrical, thermal, and optical response. Due to the fabrication variation, the initial state of each optical gate is not in a perfect cross state, and the thermo-optic efficiency of the phase shifters of each gate will differ. To precisely control the coupling ratio and common phase shift of each optical gate, all the phase shifters of the circuit are precisely calibrated by sweeping the driving current and measuring the optical transmission, and sequentially, the current-phase relationship of each phase shifter is extracted from the optical transmission response curve. This relationship contains the information of the initial phase difference between the two arms of the optical gates, and also the tuning efficiency of the phase shifters under different driving voltage/current. With this retrieved relationship, the driving voltage/current of the gate can be precisely set to the target value for the desired coupling value κ of each gate. The detailed calibration routines are as follows:

a. Measure the transmission curve of the optical gate to be calibrated. As the optical gates are embedded in the mesh structure, the laser and the power meter should connect to the corresponding measurement ports to measure transmission curves of the optical gates. Then sweep the driving voltage/current of the gate, and measure the optical transmission under different driving voltage/current.

b. Extract the relationship between the phase shift and the driving voltage/current. The value of the optical transmission curve is normalized to the range of 0 to 1, corresponding to the κ value of the gate under different driving voltages/current. Based on the κ value of the measurement curve, the differential phase $\Delta\theta$ between the two arms of the gate can be retrieved, and then the relationship between the driving current and $\Delta\theta$ can be extracted. This relationship can be either stored as a lookup table or fitted with a high-order polynomial.

c. Repeat step a-b for both phase shifters in the optical gates and for all optical gates in the mesh. When an optical gate is calibrated, it can be initialized to the cross state to mitigate the influence of the parasitic effects [7].

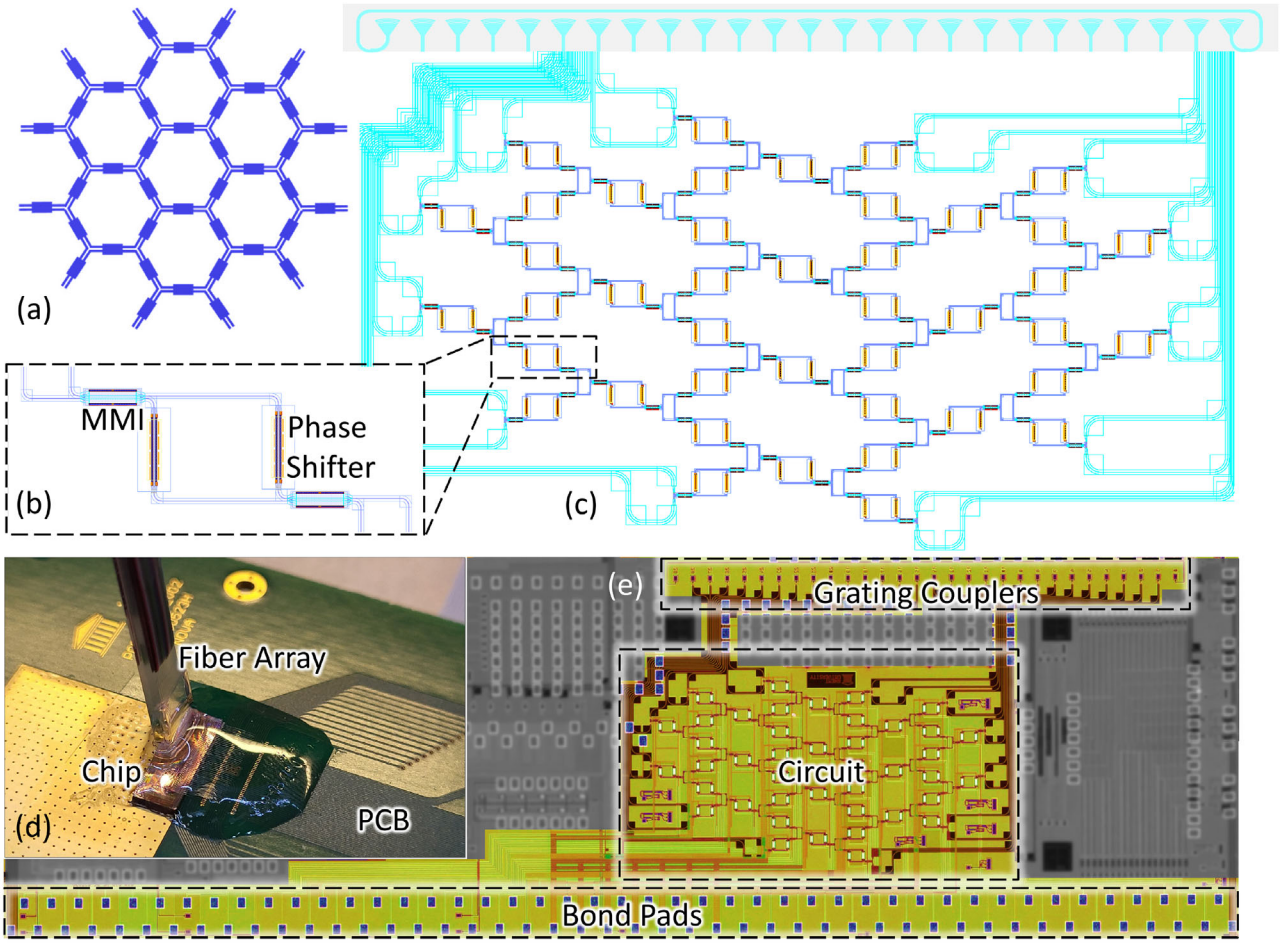

FIGURE 1 | (a) The schematic of the programmable circuit with the seven-cell hexagonal mesh structure. (b) The layout of an optical gate: an MZI constructed by two MMIs and two thermo-optic phase shifters. (c) The optical layout of this programmable circuit. (d) The photo of a packaged circuit with a PCB and a fiber array. The chip is wire-bonded to the PCB and aligned to the fiber array with the UV light-cured glue. (e) The fabricated circuit under the iSiPP200 process of IMEC.

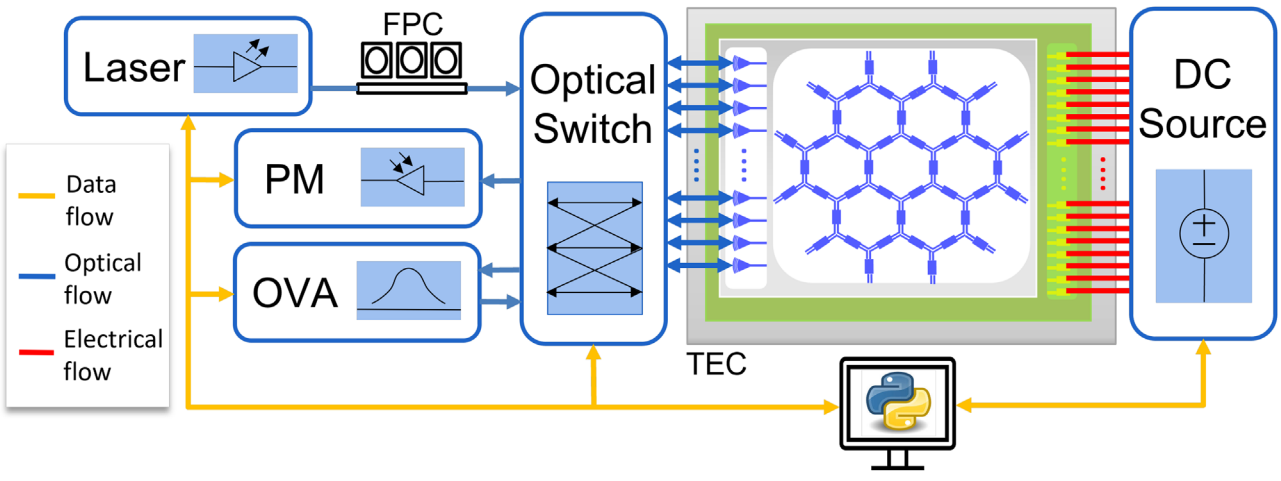

FIGURE 2 | The schematic of the measurement setup for the programmable circuit. PM: power meter, OVA: optical vector analyzer, FPC: fiber polarization controller, TEC: temperature controller.

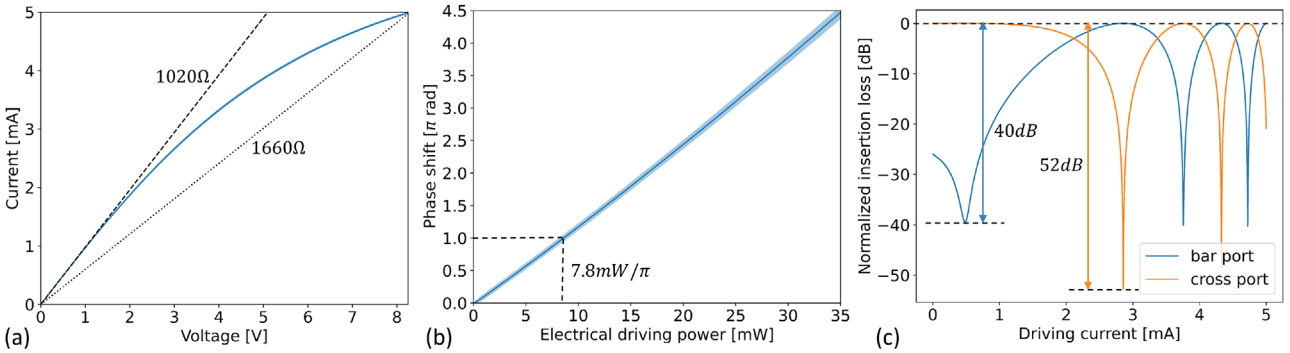

FIGURE 3 | (a) The I–V curve of the thermal-optical phase shifter used in the optical gates. (b) The relationship between the electrical driving power and the phase shift of the thermal-optical phase shifters. (c) The optical transmission curve of a single optical gate was measured by sweeping the driving current.

4 | Characterization: Properties of the Mesh

4.1 | Optical Gate

Constructed by two 50:50 splitting MMIs and two thermal-optical phase shifters, the balanced arm MZI is the fundamental building block of the programmable circuit. The MMIs used in the optical gates have a full physical length of 53 μm, the length of the undercut thermo-optic phase shifters is 58 μm, and the distance between two thermo-optic phase shifters is set to be 100 μm to conform to the design rule of the undercut, together with the waveguide bending between MMIs and phase shifters and the junctional waveguide between different gates, the physical length of the gate is 403 μm.

To improve the thermal tuning efficiency, each thermal-optical phase shifter has a local undercut. These thermo-optical phase shifters are implemented as doped silicon phase shifters, and their resistances have a strong dependence on the local temperature. Due to the undercut, the thermal dissipation is trapped in a small volume, and the phase shifters go up to a high temperature (hundreds of °C). Therefore, the heaters have a very nonlinear I–V response, and their resistances increase nonlinearly from 1020Ω to 1660Ω with the increasing driving current, as shown in Figure 3a. Despite the nonlinearity of the resistance, the optical phase shift still maintains a linear relation with the driving electrical power. As shown in Figure 3b, the measured average thermal efficiency of the 84 thermal phase shifters used in the circuit is 7.8 ± 0.4 mW/π.

As the fundamental building block of the reconfigurable optical circuit, the characterization of a single optical gate determines the performance of the circuit as a whole. The extinction ratio of the cross or bar port of the optical gate is a good figure of merit (FOM) about how well the optical gate can be tuned from 0 (bar state) to 1 (cross state) coupling ratio. To extract the extinction ratio of the gate, the driving current of the thermal phase shifters is swept, and the optical transmission is measured with the power meter. The digital-to-analog converters (DACs) delivering the electrical driving power have a precision of 16 bits, and we limited the driving current to 5 mA to prevent the over-driving of the thermal phase shifters. This limited range gives the DACs an effective precision of 12 bits. Taking one optical gate as an example, the measured extinction ratio of the bar port can reach 40 dB, and for the cross port, it achieves 52 dB, as shown in Figure 3c. These extinction ratios correspond to a 49.6:50.4 splitting ratio of MMIs, very close to the ideal 50:50. As we expect some wavelength dependence of the building blocks, we performed this measurement at different wavelengths, as shown in Figure 4a: the extinction ratio of the bar port is above 35 dB over a 100 nm wavelength range around the C-band, and the cross port keeps a extinction ratio value of around 50 dB, which shows the optical gates used in this circuit can achieve a broadband bar or cross state with high extinction ratios. Shown in the orange curve of Figure 4a, the extinction ratio of the bar port drops off for longer wavelengths, where the splitting ratio of the MMIs in the optical gates starts to deviate further from 50:50. A higher extinction ratio of the optical gates can be achieved by using multi-stage MZIs to compensate the imperfection of the MMIs [8–10], with the tradeoff of a longer physical gate length with a higher optical delay.

The total insertion loss of the configuration increases linearly with the number of optical gates in the configuration paths, so an optical gate is desired to have a low insertion loss. This requires the optical gates to have a short optical length if the average insertion loss of the waveguide is taken as a constant. Moreover, a shorter optical gate will result in a smaller group delay as well, which contributes to a larger FSR in the filter configurations or a smaller time domain resolution when defining an optical delay line. By configuring various optical delay lines with different numbers of optical gates in the path, the insertion loss and the group delay are measured. As an example, the configuration of the delay line with 46 gates, which is the longest delay line that can be configured in this circuit (passing through all edge gates once and all internal gates twice), is shown in Figure 4c. These delay lines are configured between the same pair of optical input and output ports, which eliminates any measurement errors due to variation in the fiber coupling ports. The averaging window of 0.4 nm is taken to process the measured transmission spectrum of the delay lines, to mitigate the influence of small interferences due to parasitic optical paths [7]. The detailed analysis of the parasitic effects on the optical delay line measurement is shown in the Supporting Information 1. The results are shown in Figure 4b, which shows a linear relationship between the insertion loss and the group delay with the number of optical gates in the delay line path. By taking linear regression, the measured insertion loss of a single optical gate is 0.28 dB, and the group delay is 5.5 ps per gate.

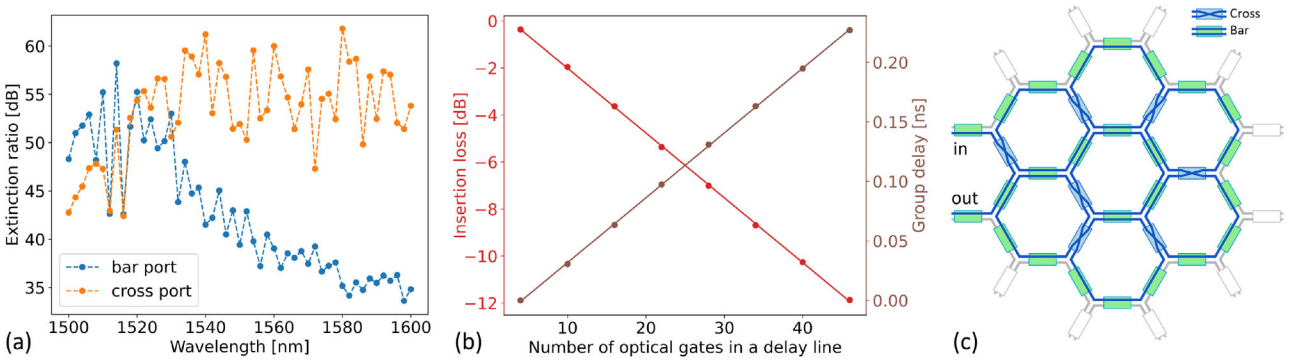

FIGURE 4 | (a) The extinction ratios of the bar port and the cross port under the wavelengths from 1500 to 1600 nm. (b) The linear relation between the insertion loss and the group delay of the optical delay lines with different numbers of optical gates in the delay line path. (The insertion loss is referenced to the shunt waveguide for fiber array alignment. The group delay is referenced to the shortest delay line with four gates configured in the measurement.) (c) The configuration of the longest optical delay line, featuring 46 optical gates, is used for measuring the insertion loss and the group delay.

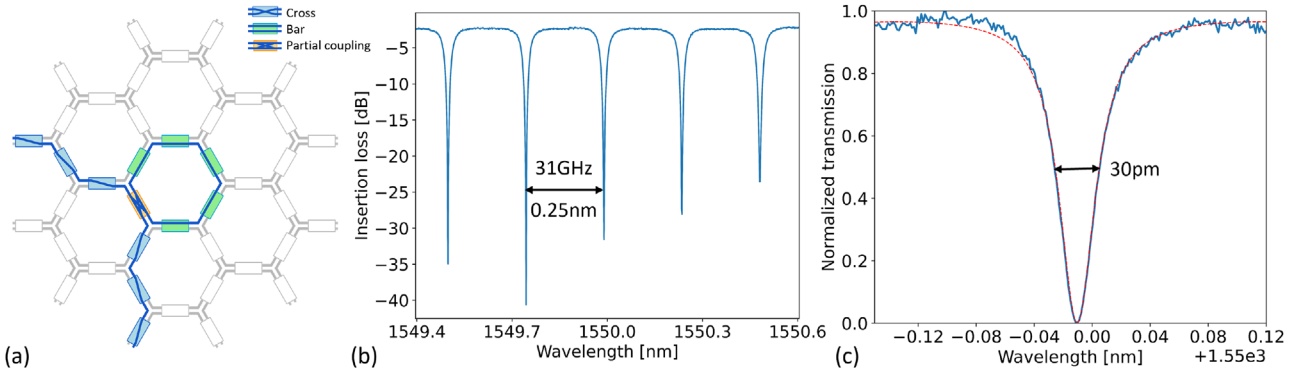

FIGURE 5 | (a) The configuration of a ring resonator on the programmable PIC. (b) The transmission spectrum of the ring resonator with an FSR of 0.25 nm, which corresponds to 31 GHz in the frequency domain. (c) The fitted ring resonant peak at critical coupling state around 1550 nm wavelength with an FWHM of 30 pm, which corresponds to a Q factor of 52 000.

4.2 | Ring Resonator

Constructed by six optical gates, a single hexagonal cell forms the most compact ring configuration. The free spectrum range (FSR) and the quality factor Q play an important role in many applications, such as optical filter synthesis. Shown in Figure 5a, five optical gates are tuned in the bar state while the other one is tuned in the partial coupling state. The transmission response of this ring configuration is shown in Figure 5b, the measured FSR of the ring is 0.25 nm, which corresponds to a 31 GHz frequency range. At the critical coupling state, the full width at half maximum(FWHM) is 30 pm as shown in Figure 5c, and the calculated Q factor of the ring at critical coupling state is around 52 000. As the Q factor is determined by the total round-trip loss of the ring resonator, the average single gate loss retrieved from the Q factor is 0.27 dB, which matches well with the delay line measurement result mentioned above.

5 | Applications

5.1 | Optical Splitter

Since the optical gate can provide an arbitrary splitting ratio between two output ports, an optical splitter can be synthesized by cascading multiple optical gates in a splitting-tree configuration, as shown in Figure 6a. This structure was configured on our programmable chip, as shown in Figure 6b, it consists of three stages of 1×2 optical splitters, with each stage giving a 50:50 splitting ratio for the incoming optical signal. The optical paths are balanced by ensuring the same number of optical gates in each path. The transmission spectra from the input port to each of the eight output ports are presented in Figure 6c.

With each stage giving a 3 dB splitting ratio and three stages in total, together with around 1 dB insertion loss from the optical path compared to the reference shunt waveguide in each channel, the total optical transmission of each channel is about –10 dB, which matches well with the measurement. The variation of the insertion loss between each channel is mainly caused by measurement variation of the connection links between the OVA to the grating couplers, including different optical switch channels with the connected fiber array channels.

5.2 | Three-Channel Multiplexer

For an add-drop ring configuration, the optical transmission under a certain wavelength is decided by the round-trip phase response of the ring and the coupling ratios of the two coupling

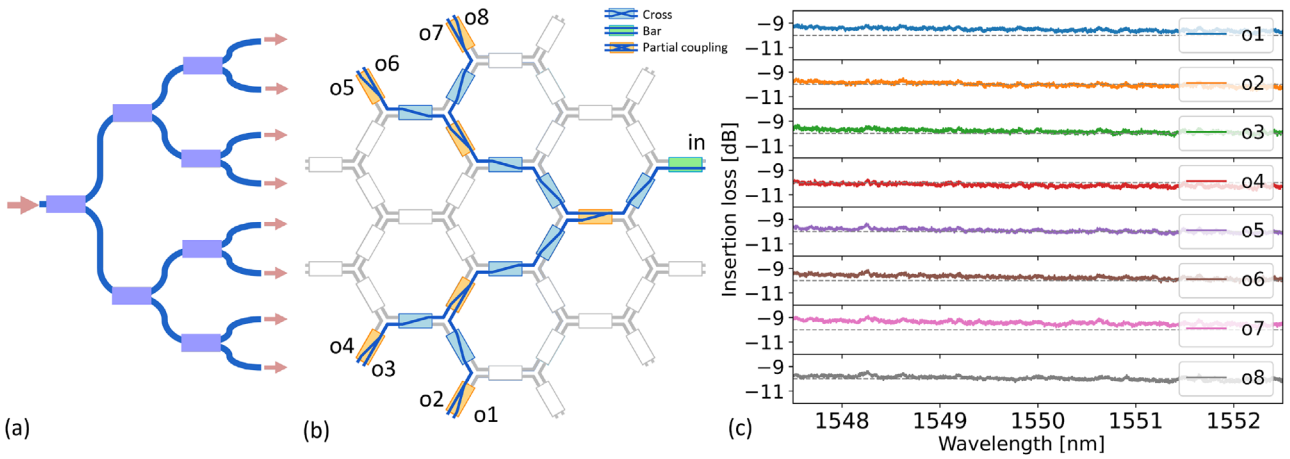

FIGURE 6 | (a) The schematic of the three-stage 1 × 8 splitter. (b) The configuration of the splitter on the programmable circuit. (c) The transmission spectrum from the input port to the eight output ports.

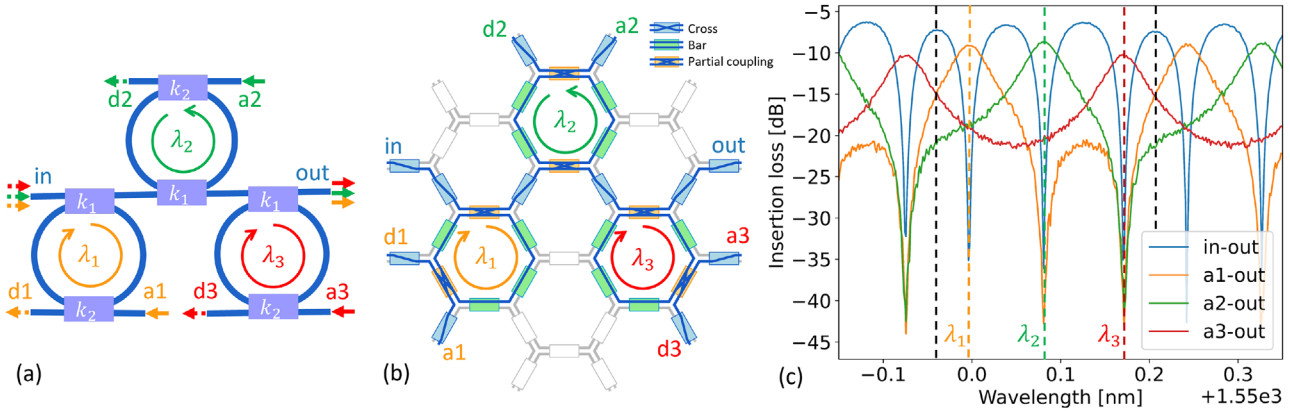

FIGURE 7 | (a) The schematic of a three-channel multiplexer based on cascaded three add-drop rings under resonance wavelengths λ_1, λ_2 and λ_3. (b) The configuration of the three-channel multiplexer on the programmable circuit. (c) The transmission spectrum of the configured multiplexer circuits.

gates in the ring [11]. The input field under a certain wavelength can be maximally transmitted to the drop channel by tuning the coupling gates, and by tuning the common phase of one arbitrary gate that constructs the ring, the resonant wavelength can be targeted to a desired wavelength. As shown in Figure 7a, by sequentially cascading the add-drop rings, a three-channel wavelength multiplexer can be used for wavelength division multiplexing applications. This add-drop ring-based multiplexing circuit can be configured on the programmable PIC as shown in Figure 7b.

To maximize the extinction ratio and minimize the insertion loss of the add-drop channels, the coupling ratio k_1 between the rings and bus waveguide is optimized to 0.44 separately, and the coupling ratio k_2 to the add-drop waveguide is corresponding tuned to 0.19. The wavelengths of the add-drop channels are tuned by adjusting the round-trip phases of the rings. The transmission curves of different channels are shown in Figure 7c. It shows three dropping channels located at λ_1, λ_2, and λ_3 in the spectrum range of one FSR from the input port *in* to the output port *out*, which match to the resonance peaks of the three add-drop rings cascaded in the optical path. And correspondingly from ports *a1*, *a2*, and *a3*, three adding channels under wavelengths λ_1, λ_2, and λ_3 are shown in the transmission spectrum to the output port *out*.

5.3 | Optical Filters

Optical filters enable the manipulation of optical signals modulated onto different wavelengths, and play an important role in different photonic applications such as wavelength demultiplexing, tunable microwave filters, or dispersion compensation etc. Inspired by the counterparts in digital signal processing, the most commonly used structures for optical filters can be divided into two types: finite impulse response (FIR) and infinite impulse response (IIR) filters [12]. The output of optical FIR filters is determined by a finite number of optical delay lines, and it exhibits a linear phase response and inherent stability. Typically, the optical FIR filters are implemented using arrayed waveguide gratings (AWGs) or cascaded MZI lattices [13, 14]. In contrast, optical IIR filters feed the output signal back into the input, creating a resonant circuit with feedback loops in the system. This feedback mechanism allows the IIR filter to achieve a spectral response with a high roll-off, but it also induces a nonlinear phase

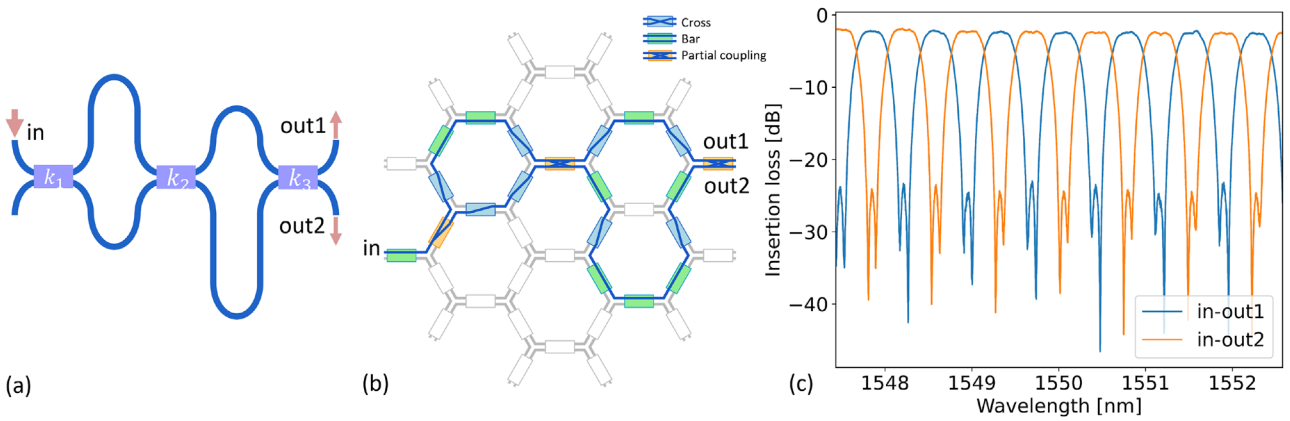

FIGURE 8 | (a) The schematic of the two-stage MZI-lattice filter. (b) The configuration of the MZI-lattice filter on the programmable circuit. (c) The transmission spectrum from the input port to the two output ports.

response and potential instability (when gain is included). The structures of optical IIR filters typically use ring resonators, such as coupled resonator optical waveguides(CROW) or ring-loaded MZI filters. Here, we will show two configurations of both types of filters: an MZI-lattice filter as an FIR interleaver and a coupled double-ring filter as an IIR tunable band-pass filter.

5.3.1 | MZI Lattice FIR Filter

The MZI-lattice filter is constructed by two stages of the MZIs as shown in Figure 8a. The first stage of the MZI has an optical delay length of two gates, and the second stage of the MZI has a delay length of four optical gates, making it a third-order filter. The corresponding configuration on the programmable circuit is shown as Figure 8b. The coupling ratios k_1, k_2, and k_3 of the three connection gates are set to be 0.5, 0.29, and 0.08, and the phase difference between the two arms in each stage can be tuned as well. In this way, this filter is configured as a flat-top interleaver where the passband width of each output port is half of the FSR. The well-balanced transmission spectrum of the two ports is shown in Figure 8c, the insertion loss of the filter is around 3 dB, and the extinction ratio of the stop band is larger than 20 dB.

5.3.2 | IIR Filter

By parallelly connecting two or multiple ring resonators, a coupled ring filter can be configured. An example of a coupled two-ring filter is shown in Figure 9a, and the corresponding configuration on the circuit is shown in Figure 9b. Compared to the feedforward MZI-lattice filter with the same order, the coupled ring filters have the advantage of a sharper roll-off between the passband and the stopband. By adjusting the coupling ratios k_1, k_2, and k_3 with the phase relationship between two rings, the bandwidth and central wavelength of the passband can be tuned. Shown in Figure 9c, we demonstrated a tunable passband filter with the adjustable passband bandwidth varying from 0.1 FSR (3 GHz) to 0.3 FSR (9 GHz). The transmission spectrum is measured from the port *in* to the port *drop*. When the passband bandwidth is smaller, the extinction ratio of the stopband increases at the tradeoff of a higher insertion loss. The configured filter of 3 GHz passband bandwidth can achieve an extinction ratio of more than 20 dB under the insertion loss of 9 dB. When the pass bandwidth is configured larger, the insertion loss decreases at the cost of a smaller extinction ratio, as shown in the transmission spectrum of 9 GHz passband bandwidth.

The free spectral range (FSR) is one of the important characteristics of the filter configuration in programmable PIC. It is the characterization of the maximally tunable bandwidth of an optical filter, and it is determined by the group delay of a single optical gate constructing the filter circuit. We show an FSR of 31 GHz for a single hexagonal ring cell constructed by six gates, to our knowledge, the largest reported in uniform general-purpose programmable PICs. Still, some filter configurations can achieve even a larger FSR that surpasses the limit of a single-cell ring. Here we will give two kinds of ring-based filter configurations that will benefit a larger FSR: the Vernier rings configuration [15] and the dual injection ring configuration [16].

The Vernier rings filter uses two coupled ring resonators with different FSR, as shown in Figure 10a. The first ring has a round trip length of 6 gates with $FSR_1 = 0.25$ nm, and the second ring has a larger one of 10 gates with $FSR_2 = 3FSR_1/5$, so the total FSR of the filter can be given as $FSR_t = 3FSR_1 = 0.75\,nm$, which corresponds to 93 GHz in the frequency domain. This Vernier ring schematic is configured on the programmable PIC as Figure 10b. To optimize the insertion loss and extinction ratio of the filter response, the coupling ratios of k_1, k_2, and k_3 are adjusted to be 0.29, 0.08, and 0.29. By measuring the transmission from the port *in* to the port *out*, the spectrum of the Vernier filter is shown in Figure 10c. The measured FSR of the Vernier filter is 93 GHz, as expected, three times the FSR of a single ring, so corresponding to a delay of two gates. The extinction ratio of the stopband is around 7 dB, and the insertion loss of the passband is around 8 dB, both of which are limited by the round-trip loss in the Vernier ring filter.

As shown in Figure 11a, in the dual injection ring filter, the input optical signal is split into two optical paths, and the two parts of the optical signal are injected into the same ring, with a group delay ΔL and phase delay ϕ. As an IIR filter, this double injection ring circuit gives a higher roll-off in the filter response, and the filter response can be tuned by adjusting the splitting ratio k_1 of the input signal, the phase delay ϕ between the two split paths, and the coupling ratios k_2 and k_3 to the ring. This configuration

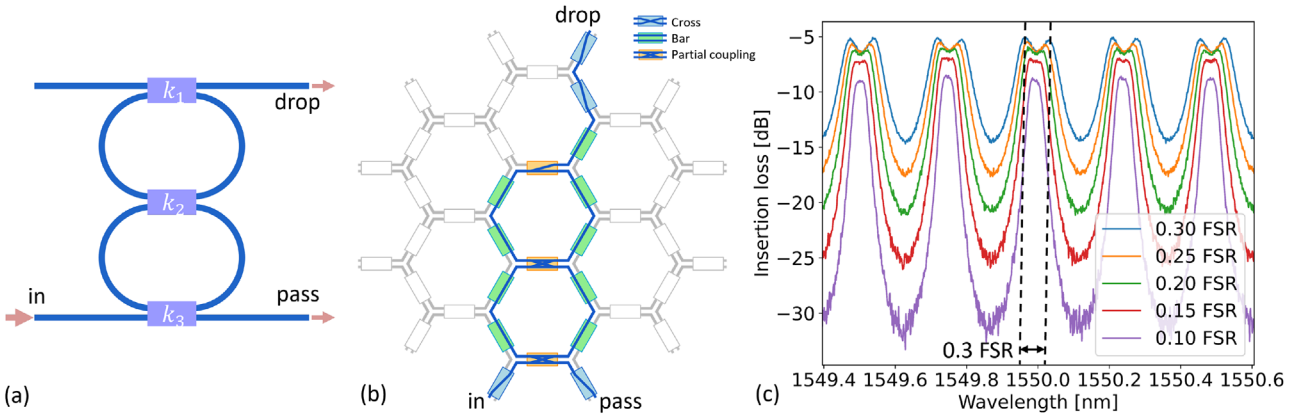

FIGURE 9 | (a) The schematic of the coupled two-ring filter. (b) The configuration of the coupled two-ring filter on the programmable circuit. (c) The transmission spectrum from the port *in* to port *drop* with different passband bandwidths varying from 0.1 FSR to 0.3 FSR.

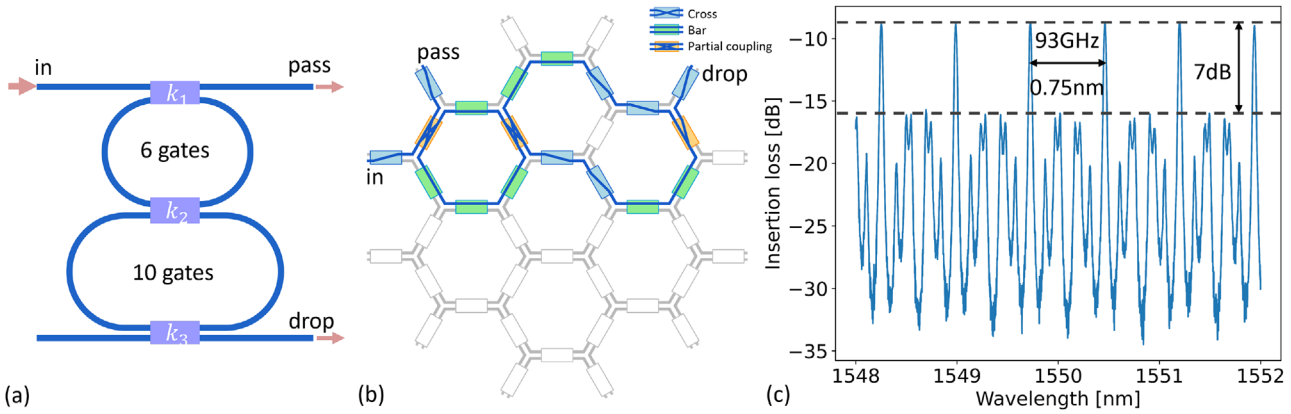

FIGURE 10 | (a) The schematic of a Vernier ring filter. (b) The configuration of the Vernier ring on the programmable circuit. (c) The transmission spectrum of the input port to the drop port.

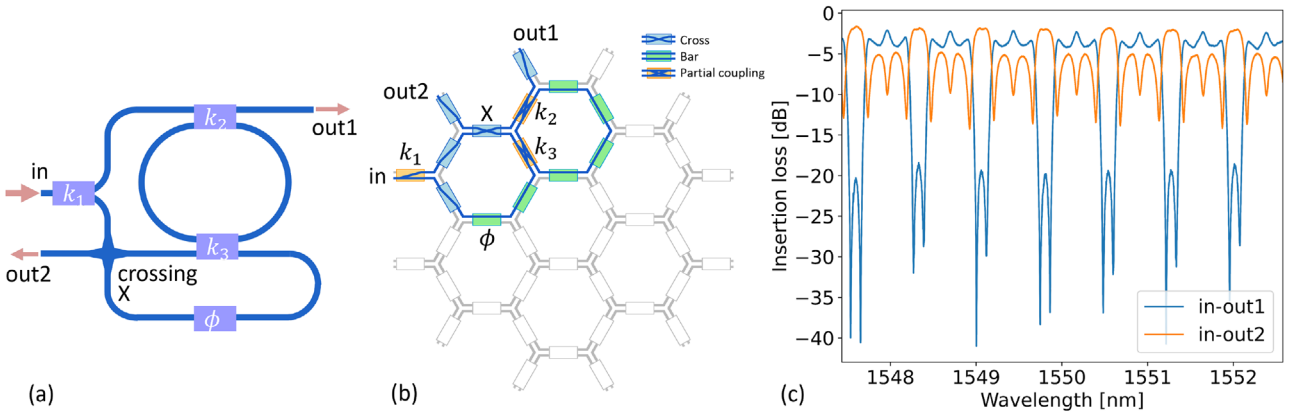

FIGURE 11 | (a) The schematic of a dual-injection ring. (b) The configuration of the dual-injection ring on the programmable circuit. (c) Transmission spectrum of the input port to the two output ports.

is implemented on the programmable PIC as shown in Figure 11b. A waveguide crossing is necessary to route the two output ports in the configuration of Figure 11a, while in the programmable PIC, the crossing is just implemented by programming one of the optical gates, since the programmable PIC takes advantage of the fact that an optical gate can be simultaneously used by two separate optical paths.

The total FSR of the filter will be decided by the group delay between the two split optical signals. As shown in Figure 11b, the two optical paths injected in the ring have an optical path length difference of two optical gates. This will result in an FSR of 0.75 nm in the transmission response, which matches well with the measured filter response shown in Figure 11c. By tuning the intensity couplings $k_1 = 0.3$, $k_2 = 0.5$, and $k_3 = 0.7$, a bandpass

TABLE 1 | The comparison of this work with selected recently published programmable PICs with different mesh structures.

	Pérez–López 2024 [17]	Shawon 2024 [18]	Catalá–Lahoz 2025 [19]	This work
Mesh structure	Hexagonal	Square	Non-uniform	Hexagonal
Number of gates in the circuit	72	67	21	42
Thermal efficiency (mW/π)	1.3	25	1.26	7.8
Physical gate length (um)	811	550	900	403
Time delay per gate (ps)	11.25	10[a]	12.5	5.5
Insertion loss per gate (dB)	0.48	N.A.	0.48	0.28
FSR of a single mesh cell (GHz)	14.98	25	13.3	31
Maximum FSR of IIR filters (GHz)	44.94	25	132.9	93

[a]Calculated from the FSR of a single square cell.

filter response from the port *out1* with an extinction ratio of 16 dB is shown in the blue curve of Figure 11c. By cascading more stages of the dual injection ring, a transmission response with a higher extinction ratio can be achieved at the tradeoff of a higher insertion loss.

6 | Discussion

In this work, we demonstrate a general-purpose programmable PIC fabricated in IMEC's iSiPP200 platform with the driving electronics and the control software layer. The optical gate is the basic building block of the mesh. This means that the properties of this component determine the performance of the programmable PIC. In this demonstration, the FOMs (e.g., insertion loss, optical delay length, thermal efficiency, and extinction ratio of two ports) of the optical gates are optimized to improve the performance of the mesh circuit. The heaters are undercut, which improves the average thermal efficiency to 7.8 mW/π. Together with the optimized MMIs, the optical gates have both a low insertion loss and a short optical length, resulting in a compact structure of the programmable photonic circuit. Currently, the gate has an insertion loss of 0.28 dB/gate with a compact physical length of 403 μm, which can result in a tunable optical delay with a resolution of 5.5 ps or a ring configuration with an FSR of 31 GHz. The advantages of the gates for the programmable PIC are demonstrated in many applications, as mentioned above. A larger FSR is desired in some applications, such as IIR wavelength filters. To make this programmable circuit useful in a real-world scenario, the fundamental limitation of the FSR of a single ring cell can be overcome by resorting to Vernier rings or a dual injection ring configuration. Both configurations boost the FSR to 93 GHz, which is three times larger compared to the single ring cell.

There is a comparison between recently published different programmable PICs with varying mesh structures shown in Table 1. As the basic building block, the optical gate in this work has the smallest average insertion loss with the shortest time delay, which translates to a larger FSR of a single mesh cell. Using the Vernier effects of the coupled rings with different round-trip lengths, we can effectively enhance the FSR by three times. In the work of Catalá-Lahoz et al. [19], a programmable PIC with a non-uniform mesh structure is put forward to enhance the FSR of filter configurations with the Vernier effect, and the maximum FSR that can be achieved is 133 GHz, as ten times that of a single cell. While the non-uniform structure has an intrinsic shortcoming for the configurations that require path balancing or routing flexibility, such as tunable delay lines or feedforward matrix multiplication. For this reason, the non-uniform mesh structure might have limited application scenarios compared to the uniform mesh structure. For the thermal efficiency of the tunable phase shifters, the result of this work can be further improved. One potential way is to replace the thermo-optic phase shifters with other power-efficient phase shifters, such as MEMS [20–22] or liquid crystal [23, 24]. A compact physical length of 403 μm of the optical gate is demonstrated in this work, while this compact physical length can be further optimized by replacing the MMIs with more compact directional couplers (DCs) [25] with a physical length of 23 μm, and the full length of the optical gate can decrease by 60μm contributed by the two DCs.

7 | Summary

In this paper we presented a compact implementation of a 7-cell hexagonal recirculating waveguide mesh, featuring 2×2 optical gates optimized for a short group delay, which enables the implementation of FIR and IIR filter circuits with a free spectral range of up to 93 GHz, corresponding to a delay length of two optical gates in the interferometric structures of the filters.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: lpor70773-sup-0001-SuppMat.pdf.