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56 GBPS CPO SILICON PHOTONICS TRANSCEIVER WITH RADIATION HARDENED ELECTRONICS FOR CPO HSSL ON SATELLITE PAYLOADS

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56 GBPS CPO SILICON PHOTONICS TRANSCEIVER WITH RADIATION HARDENED ELECTRONICS FOR CPO HSSL ON SATELLITE PAYLOADS

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ABSTRACT

The increasing demand for higher data throughput and high-frequency telecom payloads in satellites is driving the shift toward onboard optical interconnects as a solution for digital payload architectures. Traditional electrical interconnects face significant limitations at high data rates, including reduced transmission distance, higher power consumption due to complex modulation and DSP requirements, and increased electromagnetic interference (EMI). Optical interconnects offer advantages such as reduced mass, EMI immunity, and scalability to higher data rates. Current space-qualified optical transceivers, primarily based on mid-board VCSEL technology, are evolving from 12.5 Gb/s to 25 Gb/s. However, rising data rate demands and a shift toward O- and C-band wavelengths are pushing the limits of directly modulated VCSELs. Reflecting developments in terrestrial data centers, co-packaged optics (CPO) offers a promising solution for satellites by integrating optical transceivers near ASICs or FPGAs. This enables low-power, short-reach SerDes, supports higher data rates, and ensures better signal integrity and EMI resilience in next-generation satellite systems.

1. INTRODUCTION

Satellite serial links for higher data throughput and higher frequency telecom payloads necessitate increased use of on-board computer processing resulting in the emergence of optical interconnects as the preferred solution for digital payloads on board satellites. In particular, data rate increases have exacerbated the challenges associated with electrical domain interconnects where the transmission distances reduce significantly with increased bit rates. This has both limited the reach of SerDes lanes from ASICs while also resulting in the need for more complex modulation formats and increased DSP, both of which result in increased power consumption. Optical interconnects also benefit from reduced mass and immunity to EMI. To date, optical transceivers for satellite payloads have focused on mid-board VCSEL based technology with first generation transceivers at 12.5 Gb/s[1] demonstrated in orbit and second-generation devices targeting 25 Gb/s expected to be demonstrated next. However, in a similar trend to terrestrial data centers, the data rates are now increasing to a level which is challenging for directly modulated VCSELs while the move to more common comms wavelengths in the O- and C-band also presents many advantages. Co-packaged optics (CPO) is the emerging standard for terrestrial data center applications and there is an opportunity to adopt a similar architecture for satellite payloads. CPO targets the integration of optical transceivers very close to the functional ASIC/FPGA, thus enabling the use of lower power short reach SerDes and facilitating higher data rate transmission, while maintaining signal integrity and mitigating EMI effects.

2. TRANSCEIVER DEVELOPMENT

Through the ESA contract "ProtoBIX" MBRYONICS and imec are developing a silicon photonics-based transceiver designed from the ground up for deployment on satellite payloads. A co-packaged approach with separate Rx and Tx photonic integrated circuits (PICs) has been used to achieve high performance for both the electro-absorption modulator (EAM) and photodiode (PD). EAMs have the advantage due to their larger optical bandwidth over ring

modulators and, compared to ring resonator-based designs, they do not require wavelength tuning. The Tx and Rx PICs are fabricated in imec's iSiPP200 platform while the custom radiation hardened modulator drivers were designed and fabricated on the IHP SG13RH SiGe BiCMOS process[2]. The transceiver has a data rate of 56 Gb/s per channel using NRZ modulation. Through detailed analysis the NRZ format was chosen as the most promising as it allows the use of a direct drive concept where the ASIC/FPGA SerDes drives the modulator driver and eliminates CDR and retiming while also removing the need for DSP. In addition, the linearity required for 28 GBd PAM4 induces a significant power penalty compared to 56 GBd NRZ.

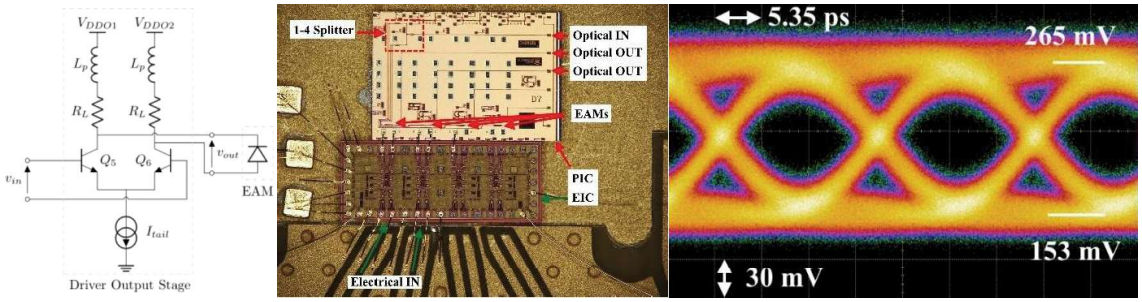

Fig.1: (a): Tx schematic (b) Tx photograph (c) Electro-optical Tx eye diagram at 56Gb/s

Fig. 1(a) shows the schematic of the output stage of the Tx driver and the modulator it drives, clearly indicating that the EAM is connected differentially.[3] In this way, the reverse bias over the modulator is set by the difference between Vddo1 and Vddo2. The shunt peaking inductors Lp are required to boost the electrical 3dB-bandwidth. Fig. 1(b) shows a photograph of the realized Tx, the driver wire bonded to the EAM-based PIC. There is one optical input, which is split between four neighboring channels. The light signal is guided in each channel to an EAM, where data is modulated. Fig. 1(c) shows the optical eye diagram of the Tx measured by a reference 70 GHz photodiode, where the EAMs were biased near the point of optimal Extinction Ratio (ER) versus Insertion Loss (IL) trade-off, meaning a 1.3V reverse bias over the EAM. An ER of 2.8 dB was reached with a reverse bias voltage of 1.5 V.

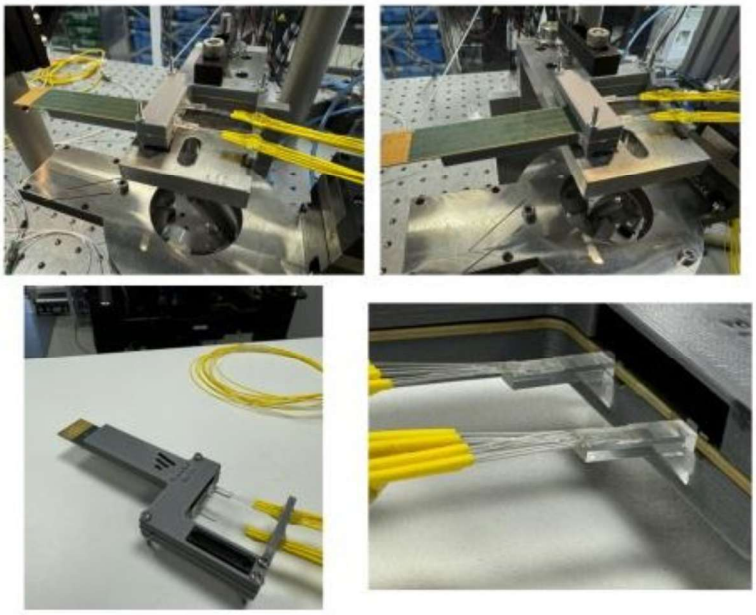

Fig.2: (top row): Images of device during fibre attach process in fibre alignment system. (bottom row): Images of demonstrator once completed with closer view of attached fibre arrays.

3. PACKAGING AND INITIAL RESULTS

To demonstrate the function of receiver and transmitter PICs, driver and TIA a prototype board compatible with QSFP-DD pluggable transceiver slot was designed and produced (see Fig.2). The PICs, TIA and driver were mounted to a high-speed PCB via flip-chip bonding. The PIC edge couplers, produced using the iSiPP200 platform, have a facet etch to ensure good optical quality. This etch produces a ledge at the device facet down to the depth of the facet edge (see Fig.3). To optically interface with the devices a lidless fibre array approach was used. This was required to facilitate fibre array access the appropriate working distance, which would have been otherwise prevented by the facet ledge. Coupling efficiencies after final attach for Tx and Rx PICs were 3 dB and 5 dB, respectively, above the expected coupling loss due to manufacturing difficulties with the PCB (which necessitated post manufacture rework of the board edge to allow of any optical coupling). These issues can be avoided in a CPO package due to the higher tolerances on ceramic or organic interposers used see, for example, [4]

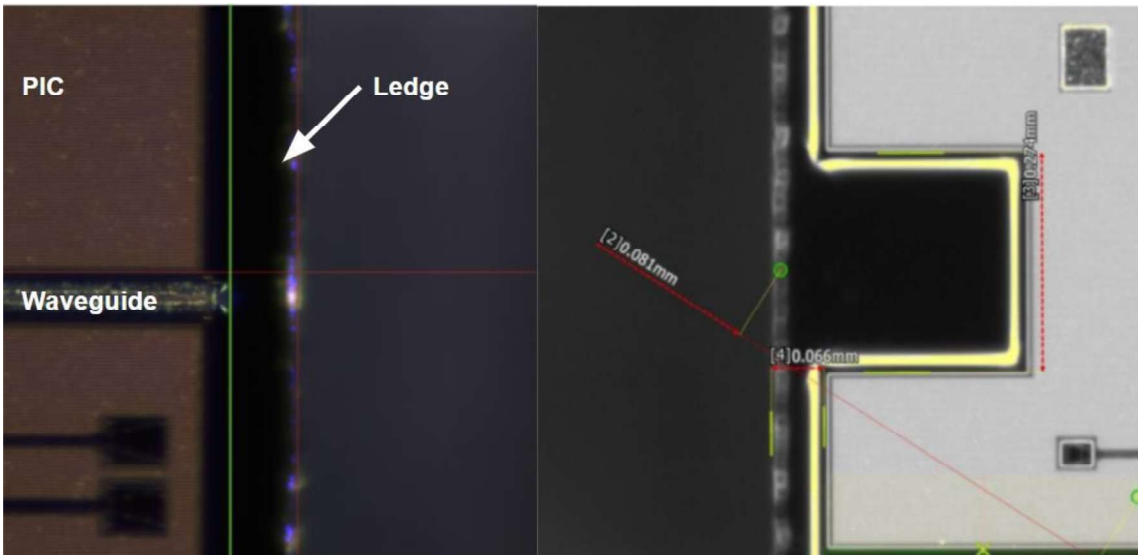

Fig.3: (a): Micrograph of PIC edge showing ledge beyond waveguide end and (b) dimensioned image taken using Keyence LM system. This die had ledge width of 66 µm and depth of 81 µm.

4. CONCLUSIONS

Overall, work on the ProtoBIX project to date has enabled the development of an ultra-low power transceiver consuming <5 pJ/bit at 56Gb/s including a laser capable of seeding multiple transceivers. The final demonstrator is currently in testing.

ACKNOWLEDGEMENTS

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