

Wafer-scale integration of lithium niobate on a silicon photonics 200-mm platform

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Abstract— We demonstrate a scalable approach for integrating lithium niobate onto silicon photonics using wafer-scale micro-transfer printing, enabling high-speed modulators with a 3.8 V half-wave voltage and over 70 GHz bandwidth. As proof of concept, over 200 lithium niobate structures were integrated on a 200-mm wafer.

Keywords—Lithium niobate, Silicon photonics, Micro-transfer printing, Scaling, Heterogeneous integration, Modulation

I. INTRODUCTION

The increasing demand for faster components in data centres, surpassing 100 GHz bandwidth, drives photonic components into the transceivers [1,2]. Silicon photonics is a key platform for straightforward integration with electronics, but emerging standards push its limits [3]. Amongst others [4–6], thin-film lithium niobate (TFLN) can help tackling these new challenges as it offers a low-loss, high-speed electro-optic response. However, CMOS fab production remains challenging due to lithium contamination [7]. Therefore, back-end heterogeneous integration via micro-transfer printing provides a solution that has been proven before [8] to enhance SiPho with non-linear [9] and high speed modulation [10–12].

In this paper, we validate that this approach is also a scalable solution, demonstrated here with over 200 TFLN photonic structures integrated on a 200-mm wafer, enabling high-speed modulators with a half-wave voltage of 3.8 V and over 70 GHz bandwidth for 7-mm long Mach-Zehnder modulators in push-pull configuration.

II. HETEROGENEOUS INTEGRATION OF LN ON A SI-SiN PLATFORM FACILITATING HIGH-SPEED MODULATORS

A. A hybrid LN/SiN Mach-Zehnder modulator

The hybrid lithium niobate/silicon nitride (LN/SiN) unbalanced Mach-Zehnder modulator (MZM) in push-pull configuration, depicted in Figure 1a, consists of LN/SiN electro-optical modulated arms, while the passive routing is done in silicon (Si). To design the passive circuit, including grating couplers, waveguides, and MMI splitters, the process development kit (PDK) of a commercially available silicon photonics (SiPho) platform, containing Si and SiN layers, is utilized. After the full processing of the SiPho wafer, thin-film lithium niobate

slabs are integrated using micro-transfer printing (μ TP). As LN tethering is seen as a contamination source in fabs, resist tethering is used to fabricate the LN devices. Moreover, the printing process does not require any change in the standard 200-mm silicon photonic wafer fabrication, nor is there any processing of the LN coupons required after heterogeneous integration.

To enter the two modulating arms, adiabatic tapering sections are used to transition the light from the Si routing to the hybrid SiN/LN waveguide, where the SiN guides the light and the LN slab provides the electro-optic response. On top of the LN slabs, electrodes consisting of a 10 nm titanium (Ti) layer and a 1 μ m gold (Au) layer are deposited with a gap of 5 μ m. An overview of four such modulators and their cross-section are shown in Figure 1e and Figure 1c, respectively.

First, a wavelength sweep around 1310 nm was performed on the 7-mm-long unbalanced MZM (Figure 1b). The results show an extinction ratio exceeding 25 dB and an insertion loss of 5.0 dB, with 3.9 dB attributed to the SiPho platform and 1.1 dB due to the transition to and propagation through the LN. From this sweep, the quadrature point, 3 dB below a maximum, was identified at 1309.38 nm. At this point, a quasi-DC electro-

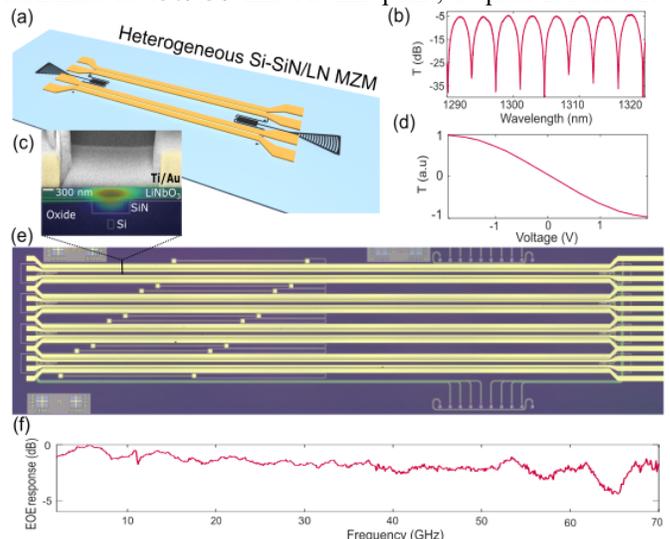


Figure 1: Hybrid LN/SiN modulator and its key performance metrics

optical experiment is conducted by driving the electrodes with a 100 kHz electrical signal. The optical power was recorded through a photodiode and displayed on an oscilloscope, allowing the output voltage to be plotted against the input voltage, as presented in Figure 1d. This recording reveals a half-wave voltage (V_π) of 3.8 V. Lastly, a high-speed measurement is performed, using a vector network analyser (VNA) to determine the electrical-optical-electrical characteristics and. As illustrated in Figure 1f, the bandwidth (BW) exceeds 70 GHz, which is limited by the BW of the measurement equipment.

III. 200-MM-PLATFORM WAFER-SCALE INTEGRATION

A. Single device integration

As a demonstration of process stability, several chips on a 200-mm wafer were populated along the two perpendicular axes and along their diagonal (Figure 2a). Using a commercial μ TP tool, 217 prefabricated LN coupons were successfully integrated on a 200-mm commercial silicon wafer with a 99% yield, including both cut-back and modulator structures. The 3-sigma alignment accuracy is 1 μ m, which can be improved to 500 nm with better alignment markers. One device failed to bond due to a pre-existing local defect at the printing location. This achievement marks the first integration of LN on a commercial 200 mm wafer using micro-transfer printing at a wafer-scale level. Moreover, the entire printing cycle, including device detection, picking, alignment, printing, and stamp cleaning, takes 1 minute and can be fully automated. An example of a fully populated chip, comprising 46 SiN/LN photonic structures, is depicted in Figure 2b, with a close-up view in Figure 2c.

In the loss test site, cut-back structures are used to determine the propagation loss through the hybrid SiN/LN waveguide. The length difference in these cut-backs is 4.2 cm. By comparing the long and short structures across all printed structures, propagation loss data are collected in Figure 2e. The average

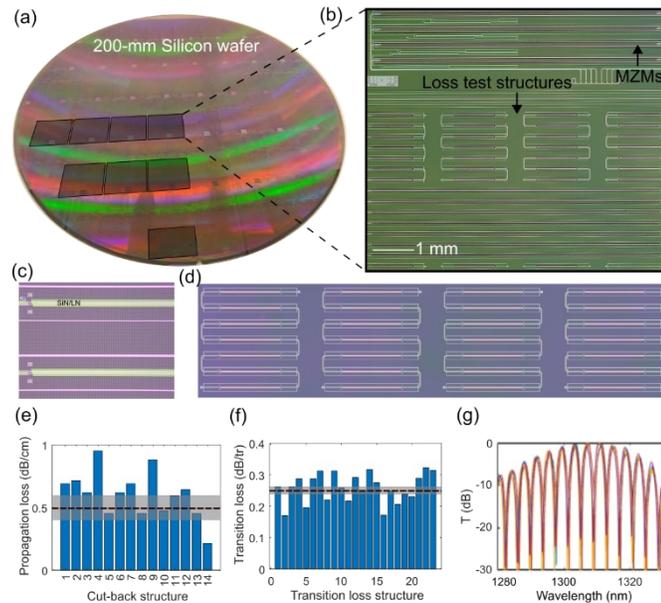


Figure 2: Wafer-scale integration of LN through micro-transfer printing

propagation loss is found to be 0.5 ± 0.1 dB/cm, never exceeding 1 dB/cm. With this propagation loss, the transmission of a single coupon can be compared to that of a chain of seven coupons to distinguish the transition loss from the Si routing to the hybrid LN/SiN waveguide. Across all printed sites, a transition loss of 0.25 ± 0.01 dB/transition is observed, as plotted in Figure 2f.

In addition to the loss test structures, groups of four MZMs are printed per chip. As an example, the transmission of four MZMs in one such a group is depicted in Figure 2g, and stable behaviour can be confirmed over all eight groups.

B. Parallel integration

In the previous section, a large number of coupons was printed one by one, but to improve integration time, also parallel printing is investigated, where the goal is to populate a full die within one printing cycle. By using a dedicated stamp and source, matching the pitch of the target, a first demonstration is conducted by printing 28 coupons of 1 mm in a 4x7 matrix configuration in one printing cycle. As can be seen in Figure 2d, the bonding of the LN slabs appears uniform.

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