Quantum Cascade Laser Integration with Mid-Infrared Photonic Integrated Circuits for Diverse Sensing Applications

Harindra Kumar Kannojia[1,] *, Tingting Zhai[1], Richard Maulini[2], David Gachet[2], Bart Kuyken[1], and Geert Van Steenberge[1]
[1]IMEC and Ghent University, Technologiepark 126, Zwijnaarde, 9052, Belgium
[2]Alpes Lasers, Avenue des Paquiers 1, 2072, Saint-Blaise, Switzerland
*harindra.kumar.kannojia@imec.be

2024 IEEE 26th Electronics Packaging Technology Conference (EPTC) | 979-8-3315-2200-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/EPTC62800.2024.10909783

1. Abstract

Mid-IR gas sensing has revolutionized several applications ranging from industrial process control to environmental monitoring and healthcare. Characteristic absorption lines of many critical molecules lie in the mid-IR region (i.e., 2-25 µm) with sparse spectral distribution allowing selective spectroscopic detection in a fast, reliable and consumables or maintenance free operation. Quantum cascade lasers (QCLs) have enabled fast, and reliable sensing with higher signal-to noise ratio. Heterogeneous integration of QCLs on photonic integrated chips (PICs) allows to achieve low-cost and compact design with multiplexing of many different wavelengths in the individual devices opening wide possibilities with enhanced performances. For example, QCLs having relatively higher power output at different wavelengths can be fabricated on wafer scale and then integrated on separately fabricated PICs. Germanium's advantages like wide transparency in mid-IR range (up to 15 µm) and strong non-linear refractive index has favored its application in the mid-IR range as compared to the standard SiN and SOI platforms. This work presents different hybrid integration techniques to integrate multiple mid-IR lasers to butt-couple with respective Ge waveguides on individual Ge-on-SOI PICs in epi-up and epi-down orientation for several sensing applications.

2. Introduction

Continuous advances in the mid-infrared (mid-IR) spectroscopy field have critically transformed many diverse applications across various fields like medical diagnostics, healthcare, environmental monitoring, defense, and industrial processes [1]. It is an extremely sensitive technique employed for the chemical and biological analysis of several significant molecules, like carbon dioxide (CO2), methane (CH4), nitric oxide (NO), nitrous oxide (N2O), sulfur dioxide (SO2), phosphates, etc. [2] The discrete characteristic absorption spectrum lying in mid-IR region (i.e., 2-25 µm) with orders of higher magnitude absorption in addition to sparse spectral distribution as compared to visible and near-infrared (near-IR) sensing makes mid-IR spectroscopy being highly selective, reliable and sensitive down to parts per million (PPM) or even billion (PPB) levels [2]-[5]. Ground-breaking developments in passive and active optoelectronic technologies, like laser sources (quantum cascade lasers - QCLs), waveguides (Ge-on-SOI), photodetectors, etc. in addition to coupling techniques, integration schemes, has paved ways for fast, and consistent sensing with higher signal-to-noise ratio. Growth in laser technologies has resulted in QCLs having extremely low footprint areas with quite high optical output power in continuous wave operation at room temperatures [6]. Emitting light beam from QCLs exhibit high wavelength tunability which can be easily tailored by band-gap engineering [7].

Silicon photonics has been rapidly evolving utilizing the mature silicon-based complimentary metal oxide semiconductor (CMOS) microfabrication technologies. Innovative integration techniques like monolithic and heterogenous integration can be utilized to realize extremely

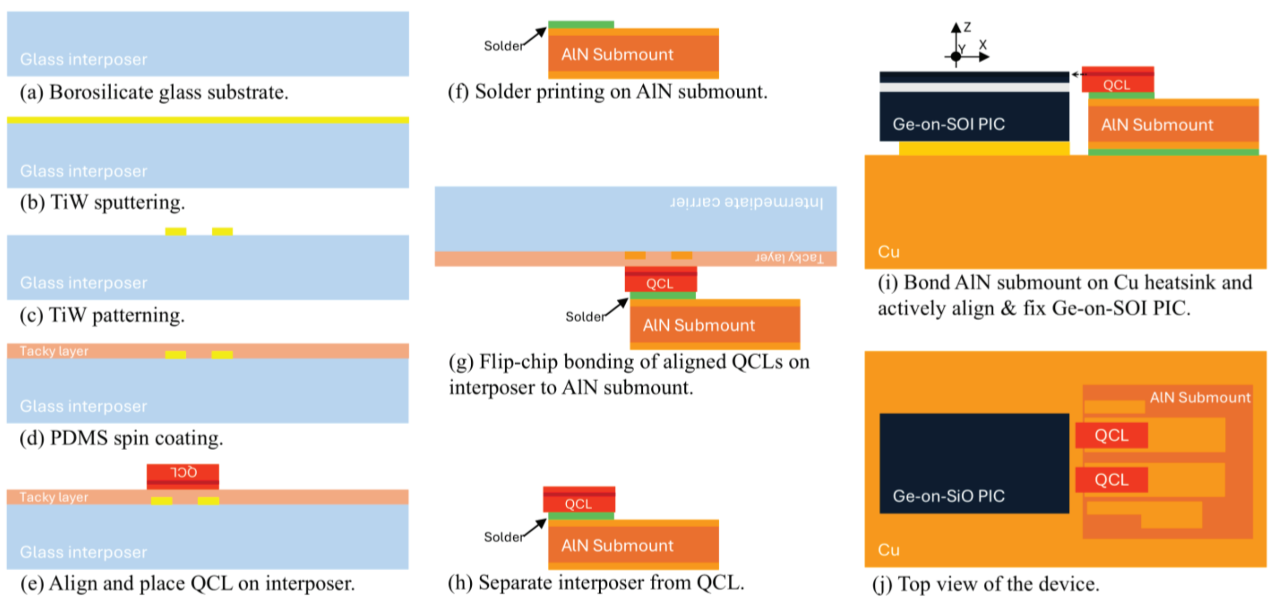

Figure 1: Interposer fabrication and Epi-up assembly of QCLs on AlN submount. (a) glass substrate, (b) TiW sputtering, (c) TiW patterning, (d) PDMS spin-coating, (e) QCL alignment and placement on interposer, (f) solder printing on AlN submount, (g) flip-chip bonding of aligned QCLs on interposer to AlN submount, (h) interposer separation from QCL, (i) AlN submount fixation followed by active alignment and fixation of Ge-on-SOI PIC on Cu heatsink, and (j) top view of the final device.

miniaturized devices. Also, the advanced available expertise in various technological domain like CMOS fabrication, photonic integrated chips (PICs) and components like high-power quantum cascade (QC) chips [8], resonators [9], modulators [10], couplers [11], and multiplexers [12] using dedicated manufacturing techniques could aid miniaturization targets. However, the monolithic and heterogenous integration techniques are still at lower technology readiness level as reported recently [13]. Heterogeneous integration of QCLs on photonic integrated chips (PICs) enables the combination of multiple wavelengths and functionalities on a single chip, reducing the size, cost, and power consumption of traditional mid-IR sensing systems. Ge-on-SOI features advantages in terms of wide transparency and strong non-linear refractive index in mid-IR range which favors its application in the mid-IR range as compared to standard SiN and SOI platforms [14].

In this work, different techniques for hybrid integration of QCLs with germanium-on-silicon (Ge-on-SOI) PICs, utilizing both epi-up and epi-down orientations have been reported to optimize coupling efficiency and device performance. By combining the high output power and tunability of customized QCLs with the scalability and versatility of in-house fabricated Ge-on-SOI PICs, reported approach opens up new possibilities for mid-IR sensing in a wide range of applications, including environmental gas monitoring, industrial process monitoring and safety, along with medical diagnostics and point-of-care health monitoring devices.

3. Experimental details

In this work, hybrid integration of QCLs on submounts in (i) epi-up and (ii) epi-down orientations is presented, which can be later actively aligned with respect to the Ge-on-SOI PICs having specifically designed Ge waveguides. In the epi-up integration, an interposer was fabricated using 2-inch borosilicate glass substrate. At first, the borosilicate glass substrates were thoroughly cleaned using RBS cleaning solution, followed by cleaning in acetone, and isopropyl alcohol. Later the substrates were rinsed with deionized (DI) water and dried using nitrogen gas. In the second step, the cleaned glass substrates were sputtered with 150 nm thick TiW layer which was patterned afterwards using conventional lithography and wet etching process to form dedicated alignment marks in patterned thin metal. These alignment marks were designed in such a way that the metal patterns and the active region on the QCL's top surface can be used as alignment marks for alignment. Additionally, the alignment marks were designed to perfectly align two QCLs with respect to each other in both X- and Y- direction on individual glass substrates or interposers. Thereafter in the third and last step, a transparent layer of 5 µm thick polydimethylsiloxane (PDMS) was spin-coated on top of the patterned alignment marks to achieve a mildly sticky or tacky layer on top, completing the interposer fabrication process.

In epi-up hybrid integration technique, two QCLs were initially aligned and temporarily bonded to the glass interposer in epi-down orientation using dedicated alignment marks and the tacky PDMS layer, respectively. Subsequently, these two QCLs, aligned with respect to each other on glass interposer, were simultaneously flip-chip bonded to Aluminium nitride (AlN) submount having screen printed solder patches resulting in an epi-up integration of two aligned QCLs on AlN submount. AlN submounts were outsourced from external vendor for fast experimental processing. The active regions of the two QCLs would have good alignment in Z-direction as well since both QCLs are held horizontal using glass interposer during flip-chip bonding and solder material will reflow to compensate any minor variation in the QCLs thicknesses or taperedness. The schematic representation of fabrication process flow for glass interposer and epi-up integration steps are shown in Fig. 1.

Ideally, epi-up integration on AlN submount is conveniently favorable for active alignment and superior thermal properties of AlN. However, sometimes QCLs have thickness variations of few tens of microns due to variations in backside thinning or if they belong to different wafers or batches. This would jeopardize the QCL's alignment in Z-direction, i.e., active regions of two QCLs will not be on same height anymore using the first discussed epi-up integration. Therefore, the second solution of hybrid integration in epi-down orientation was proposed where QCLs were directly flip-chip integrated on in-house fabricated Si submount. The fabrication of Si submount was very standard wafer scale processing, where 4-inch Si wafers were first cleaned. Followed by the wafer scale alignment marks fabrication by patterning sputter deposited 70 nm TiW and 350 nm Al stack using standard lithography and wet-etching processes. Thereafter selective electroless nickel-gold plating was performed to form various pads for solder-based flip-chip & wire bonding. QCLs were directly flip-chip bonded to the Si submount in epi-down orientation using alignment marks on the Si submounts and QCL's Au metallization patterns to align them in X- and Y-direction with respect to each other, similar to the glass interposers for epi-up integration (as explained before). In the epi-down orientation, the active region of the QCLs will be on same height with respect to the

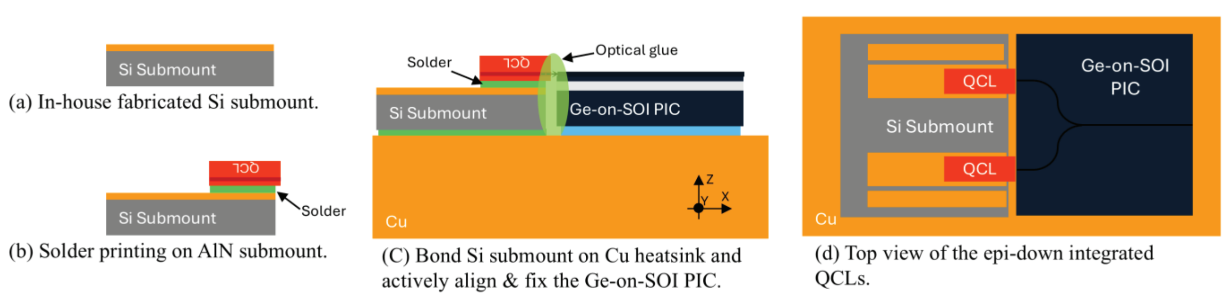

Figure 2: Epi-down assembly of QCL on Si submount. (a) Si submount, (b) Epi-down QCL assembly on Si submount, (c) Si submount fixation followed by active alignment and fixation of Ge-on-SOI PIC on Cu heatsink, and (d) top-view of the final assembled epi-down QCLs on Cu heat sink

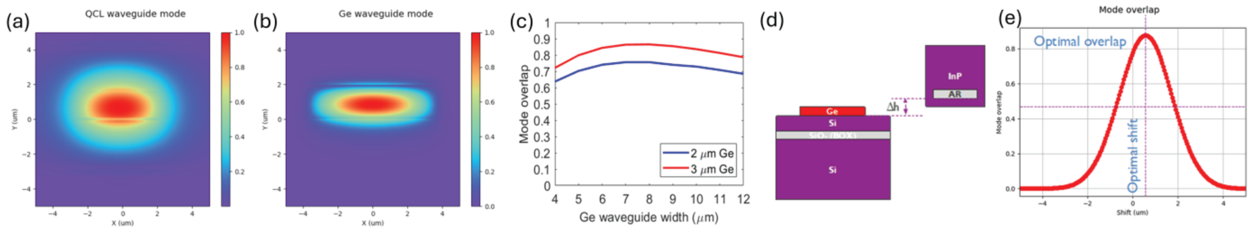

Figure 3: Ge-on-SOI PICs design for optimal coupling. Amplitude of the electrical field (TM polarized) in (a) QCL and (b) 2 um thick Ge waveguide, (c) Mode overlap between the QC chip and the Ge waveguide as a function of Ge waveguide width, (d) Definition of vertical shift between the QC chip and the Ge waveguide, and (e) Mode overlap as a function of the vertical shift between the active region of the QC chip and the 3 um Ge waveguide on PIC.

Si submount since the QCL's top side layers will have least thickness variation (i.e., ~100 nm) owing to standard optimized microfabrication techniques. The epi-down integration is schematically illustrated in Fig. 2.

4. Simulation

Numerical simulations were performed to investigate the optimal coupling as well as alignment accuracy on optical losses in order to co-design the QCLs and Ge-on-SOI PICs. The electrical field of TM-polarized fundamental mode in a QC chip emitting at 1,900 cm-1, with a 4.65 µm wide, 1.7 µm thick active region and a 7.5 µm wide, 2 µm thick Ge waveguide on PIC are depicted in Fig. 3(a-b). The coupling efficiency between a QCL and a Ge waveguide is primarily determined by the mode overlap, which can be calculated using the integral of electric fields of QCL and Ge waveguide (in terms of energy), with the assumption that the electrical fields are oriented in the same direction:

$$\eta = \frac{\left|\iint E_{QC}^{*} E_{Ge} dA\right|^2}{\iint \left|E_{QC}\right|^2 dA \times \iint \left|E_{Ge}\right|^2 dA}$$

where E_{QC} and E_{Ge} are scalar values of the electrical field in QC and Ge waveguide's modes, respectively. Crucial point to be noted here is that neither the longitudinal offset nor the parasitic reflections between the between the QC chip and the Ge waveguide have been considered. Therefore, the values of the mode overlap computed here constitute an upper bound to the coupling efficiency that can be achieved for the perfect alignment. Simulation showed that the maximum power coupling between the QCL and PIC is obtained for a given 2 µm thick Ge waveguide with 7.5 µm width. Meanwhile, an increase in Ge waveguide thickness from 2 to 3 µm increases the maximum power coupling between the QCL and Ge waveguide from 79% to 88%, as shown in Fig. 3(c).

Additionally, the effect of misalignment between QC chip and Ge waveguide on mode overlap was investigated as well. The definition of vertical shift between QC chip and Ge waveguide are depicted in Fig. 3(d). For the 2 µm thick Ge waveguide on Ge-on-SOI PICs, the overlap is maximized when there is no vertical shift between the active region of QC chip and Ge waveguide on PIC (i.e., for Δh = 0). However, a misalignment of ± 1.3 µm in the vertical direction resulted in 3 dB or 50% drop in the mode overlap (Fig. 3(e)). Furthermore, for lateral directions, a misalignment of ± 2.33 µm resulted in 3 dB mode overlap degradation. While in 3 µm thick Ge waveguide on Ge-on-SOI PICs, mode overlap is maximized for a non-null vertical shift, i.e., Δh = 500 nm and ± 1.27 µm tolerance was observed for 3 dB drop in mode overlap in the vertical direction. This effect should be accounted for while co-designing the QC chips and Ge-on-SOI chips.

5. Results and Discussion

The step-by-step fabrication results from the epi-up assembly of QCLs on AlN submount is presented in Fig. 4. The fabricated glass interposer with zoomed-in view of the alignment marks is shown in Fig. 4(a-b). Two QCLs were aligned and placed on the glass interposer in epi-down orientation one by one, as shown in Fig. 4(c-e). The alignment accuracy of the QCLs on glass interposer after the first flip-chip bonding step, i.e., in face-down configuration, was measured by observing the assembled QCLs through glass interposer (Fig. 4(c-d)). The alignment accuracy of ~ 2 µm was measured in X- and Y- direction. Tilting in X- and Y-directions was measured to be ~ 4 µm pertaining to the variations in the Au metallization on the QCLs. However, these tilts in both directions were flattened out during the second step, i.e., flip-chip bonding step on AlN submount. The two QCLs temporarily bonded to the glass interposer and aligned with respect to each other using alignment marks are shown in Fig. 4(e). In the second step, the aligned QCLs on interposer were simultaneously bonded to AlN submounts (Fig 4(f)) having screen printed solder patches as shown in Fig 4(g). No critical alignment was required in this bonding step since AlN submount had no alignment marks. However, during this bonding it was made sure that the QCLs were centered as well as parallel to the AlN metal pads and both QCLs perfectly land on them to achieve proper bonding.

The soldered QCLs to the AlN substrate were easily separated from the glass interposer since the bond strength of the solder would be much higher than the bond strength between the QCL and the glass interposer where bonding is basically due to tacky PDMS layer. The resulting epi-up assembled QCLs on AlN submount is presented in (Fig. 4(h)). Optical profilometry showed that the two QCLs assembled on a single AlN submount had a height variation of ~ 7±3 µm. The solder reflow would have compensated some height variations but not completely since the QCL's thickness showed variation of 10-30 µm This was mainly attributed to the thickness variation in the QCLs owing to processing variations as explained in the experimental details section. The final wire-bonded sample for the electrical connections to the topside of the QCL is presented in Fig. 4(i).

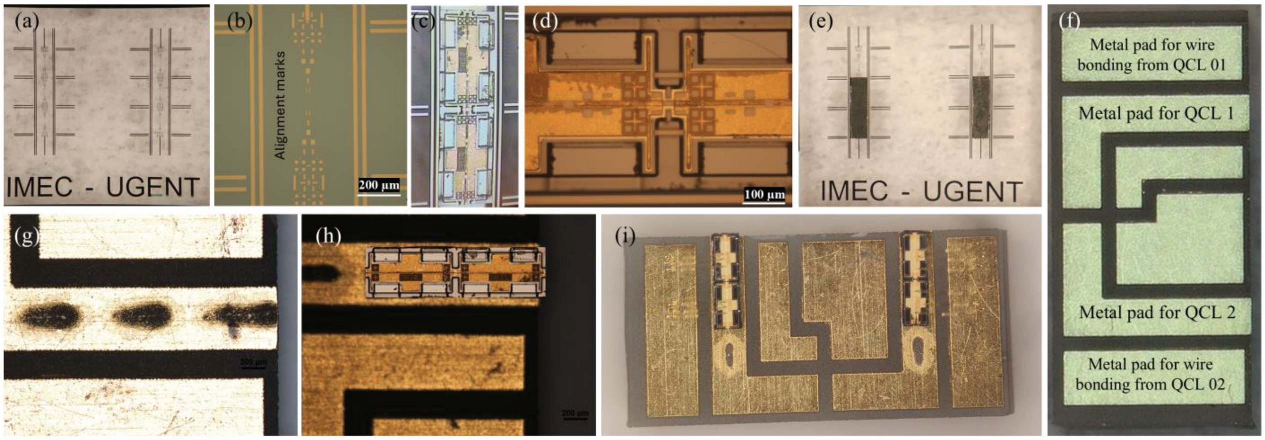

Figure 4: Epi-up assembly results. (a) glass interposer, (b) interposer alignment marks. (c) Aligned QCL on an interposer, (d) zoomed-in image showing alignment accuracy, (e) two QCLs on a single interposer, (f) AlN submount, (g) screen printed solder on AlN submount, (h) an epi-up assembled QCL, and (i) Final two epi-up assembled QCL on AlN submount with wire bonding.

As mentioned before, to compensate for the height variations of the QCLs which would result in challenging active alignment requirements for the Ge waveguides on the Ge-on-SOI PICs, epi-down integration was carried out as demonstrated schematically in Fig. 5. Since the topside of the QCL has a few µm in total of InP cladding and Au metallization, where variations are very less likely due to controlled deposition techniques involved. Nevertheless, variation in the range of a few tens to a few hundreds of nanometers is still possible which can be easily compensated during the active alignment of Ge waveguides on Ge-on-SOI substrates.

The in-house fabricated wafer scale Si submounts with magnified images of individual Si submount and alignment marks are shown in Fig. 6(a-c). The epi-down integration results of a QCL showing screen printed solder, flip-chip bonding and finally wire-bonded QCL to electrically connect the QCL's backside are presented in Fig. 6(d-f). In the epi-down integration, lateral alignment accuracy could not be measured after the flip-chip bonding step since there were no reference alignment marks on the back side of the QCL and the top-surface was not visible anymore as the QCLs were bonded in epi-down orientation. However, the tip and tilt of the assembled QCLs were measured using non-contact optical profilometry which were less than 2 µm in both X- and Y-directions.

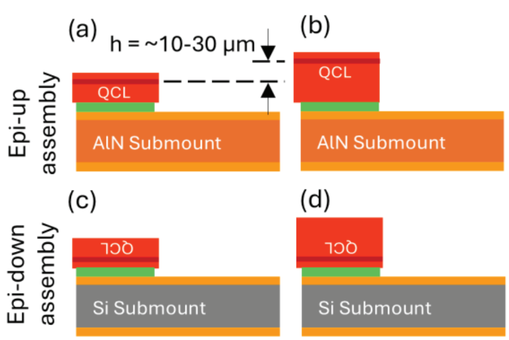

Figure 5: Comparison of epi-up and epi-down assembly to illustrate the importance of QCL thickness variation.

In both epi-up and epi-down assembly on respective submounts, an offset of 75 µm was provided in the longitudinal direction so that the coupling facet of the QCLs are protruding few tens of micrometers out of the submount edge as shown in Fig. 4(h) and Fig. 6(e), respectively. This offset was introduced for two reasons. The first reason was to avoid any contamination of the QCL's emitting facet with any solder and/or flux material during the flip-chip bonding and solder reflow process. The second was to facilitate the butt coupling process during the active alignment of the Ge waveguides on Ge-on-SOI PICs so that there is negligible to no gap between the QCL's emitting facet and the Ge waveguide's facet, and thus avoiding any extra optical losses due to larger gaps during butt coupling.

The assembled QCLs were characterized for the I-V characteristics and optical output power. The submounts having wire bonded QCLs on top of them in both epi-up and epi-down orientations were placed on a copper heat sink attached to thermo-electric cooler (TEC) stage to excite the QCL at controlled temperatures. The characterizations were performed at 15°C and the driving current was swept from 0 mA to 300 mA. All measurements were performed with continuous-wave mode driving current signal. The measured I-V characteristics of an assembled QCL is presented in Fig. 6(g) exhibiting that good electrical connections were obtained during the QCL flip-chip soldering and wire-bonding processes. Fig. 6(h) illustrates the variation of optical power output with respect to the increasing driving current for the assembled QCL. The maximum optical output power was measured to be 3.7 mW for the driving current of 220 mA for the assembled QCL. A clear thermal roll-over was observed, however, a shallow positive slope was observed for the optical power output variation with driving current below the lasing threshold between 50 mA to 160 mA (Fig. 6(h)). This can be attributed to the thermal noise during the characterization of the QC chip on the water cooled TEC stage, which is a rudimentary setup for preliminary characterizations of hybrid assembled QCLs on submounts before active alignment. Additionally, the Ge-on-SOI PIC processing is ongoing for active alignment and hybrid integration QCL assembled on submounts to Ge waveguides on the Ge-on-SOI PICs.

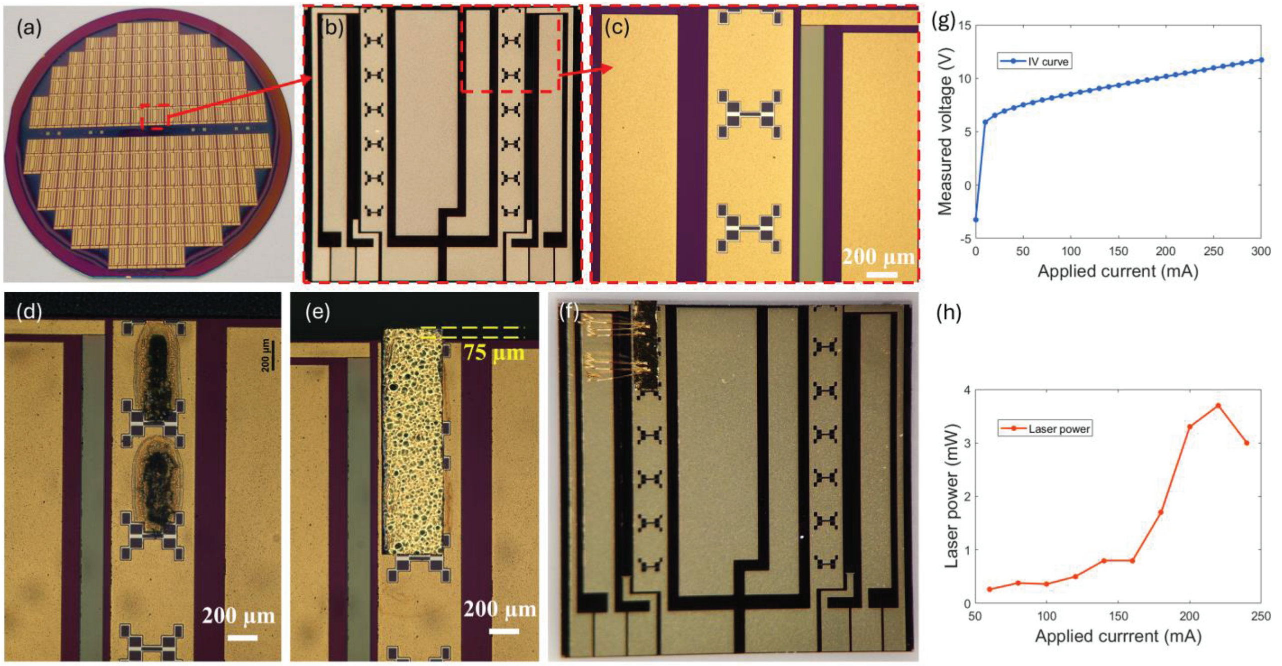

Figure 6: Epi-down assembly results. (a) wafer scale Si submount, (b) single Si submount, (c) zoomed-in alignment marks on Si submount, (d) screen printed solder patches on Si submount, (e) flip-chip bonded QCL in epi-down configuration on Si submount, (f) final wire bonded QCL on Si submount in epi-down configuration, (g) measured I-V characteristic, and (h) measured optical output power variation with respect to driving current.

This work presents the preliminary results of the hybrid integration techniques being developed within the M3NIR (integrated, modular, multi-sensing mid- and near- IR sensing platform) project. Dedicated high power lasers and Ge-on-SOI PICs are under fabrication for hybrid integration and active alignment of the QCLs and Ge-on-SOI PICs, followed by final packaging in a high heat load (HHL) package with TEC to realize a sealed sensing platform for harsh environment applications.

6. Conclusions

Hybrid integration of independently fabricated quantum cascade chips and photonic integrated chips are particularly useful for harnessing the potential of individual fabrication technologies. This work reports epi-up and epi-down integration of multiple QCLs on different submounts, i.e., AlN and Si submounts with an accuracy of less than 2 µm in X-, Y- and Z- directions. Simultaneous integration of more than one QCLs having different wavelengths on a single submount was successfully demonstrated. The assembled QCLs were characterized to exhibit standard I-V characteristics indicating good electrical contact between the QCL and the submounts. Furthermore, the maximum optical output power of the QCL assembled on a submount was measured to be 3.7 mW at 15 °C for a continuous wave driving current of 220 mA. The reported technology allows for multiple QCLs with different wavelengths to be integrated on single PIC resulting in low-cost, compact, and high-performance modular sensing platform for many different applications like monitoring greenhouse gases, breath analysis for health, detecting phosphates & nitrates in water, ships emissions, and well-being related applications.

Acknowledgements

This work was supported by the European Union's Horizon Europe Research and Innovation Program under Agreement 101093008 and by the Swiss Secretariat for Education, Research, and Innovation (SERI) for M3NIR (integrated, modular, multi-sensing mid- and near- IR sensing platform).

References

[1] G. Flores Rangel, L. Diaz de León Martínez, L. S. Walter, and B. Mizaikoff, "Recent advances and trends in mid-infrared chem/bio sensors," TrAC - Trends in Analytical Chemistry, vol. 180, Nov. 2024, doi: 10.1016/j.trac.2024.117916.

[2] A. Dabrowska, S. Lindner, A. Schwaighofer, and B. Lendl, "Mid-IR dispersion spectroscopy – A new avenue for liquid phase analysis," Spectrochim Acta A Mol Biomol Spectrosc, vol. 286, Feb. 2023, doi: 10.1016/j.saa.2022.122014.

[3] D. Wang, H. K. Kannojia, P. Jouy, E. Giraud, G. Van Steenberge, and B. Kuyken, "Mid-infrared dual-comb QCLs integrated with beam combiner based on Ge-on-Si platform," in IEEE International Conference on Group IV Photonics GFP, IEEE Computer Society, 2023. doi: 10.1109/SiPhotonics55903.2023.10141936.

[4] A. Lambrecht and K. Schmitt, "Mid-infrared gas-sensing systems and applications," in Mid-infrared Optoelectronics: Materials, Devices, and Applications, Elsevier, 2019, pp. 661–715. doi: 10.1016/B978-0-08-102709-7.00016-4.

[5] A. Genner, P. Martín-mateos, H. Moser, and B. Lendl, "A quantum cascade laser-based multi-gas sensor for ambient

air monitoring," Sensors (Switzerland), vol. 20, no. 7, Apr. 2020, doi: 10.3390/s20071850.

[6] A. Wittmann et al., "Room temperature, continuous wave operation of distributed feedback quantum cascade lasers with widely spaced operation frequencies," Appl Phys Lett, vol. 89, no. 14, 2006, doi: 10.1063/1.2358939.

[7] S. Radosavljevic et al., "Thermally Tunable Quantum Cascade Laser with an External Germanium-on-SOI Distributed Bragg Reflector," IEEE Journal of Selected Topics in Quantum Electronics, vol. 25, no. 6, Nov. 2019, doi: 10.1109/JSTQE.2019.2933784.

[8] H. Nguyen-Van et al., "Quantum cascade lasers grown on silicon," Sci Rep, vol. 8, no. 1, pp. 1–8, Dec. 2018, doi: 10.1038/s41598-018-24723-2.

[9] S. Radosavljevic et al., "Mid-infrared Vernier racetrack resonator tunable filter implemented on a germanium on SOI waveguide platform [Invited]," Opt Mater Express, vol. 8, no. 4, pp. 824–835, Apr. 2018, doi: 10.1364/ome.8.000824.

[10] T. H. N. Nguyen et al., "Integrated PIN modulator and photodetector operating in the mid-infrared range from 5.5 µm to 10 µm," Nanophotonics, vol. 13, no. 10, pp. 1803–1813, Apr. 2024, doi: 10.1515/nanoph-2023-0692.

[11] S. Radosavljevic, B. Kuyken, and G. Roelkens, "Efficient 5.2 µm wavelength fiber-to-chip grating couplers for the Ge-on-Si and Ge-on-SOI mid-infrared waveguide platform," Opt Express, vol. 25, no. 16, pp. 19034–19042, Aug. 2017, doi: 10.1364/oe.25.019034.

[12] A. Malik et al., "Germanium-on-silicon mid-infrared arrayed waveguide grating multiplexers," IEEE Photonics Technology Letters, vol. 25, no. 18, pp. 1805–1808, 2013, doi: 10.1109/LPT.2013.2276479.

[13] S. Shekhar et al., "Roadmapping the next generation of silicon photonics," Nat Commun, vol. 15, no. 1, pp. 1–15, Dec. 2024, doi: 10.1038/s41467-024-44750-0.

[14] D. Wang et al., "Innovative Integration of Dual Quantum Cascade Lasers on Silicon Photonics Platform," Micromachines (Basel), vol. 15, no. 8, pp. 1–13, Aug. 2024, doi: 10.3390/mi15081055.