Integrated Photonics and Electronics for Optical Transceivers Supporting AI/ML Applications

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***Abstract*—The recent proliferation of artificial intelligence and machine learning applications relying on large language models is fueling unprecedented demand for compute capacity. Associated with this is a need to scale capacities of short-reach optical transceivers towards multiplex Terabit/s, while maintaining integration density (frontpanel or beachfront density) and energy efficiency (pJ/bit). One option to scale transceiver capacity is to increase the bandwidth per lane from today's 200 G to 400 G or even higher: coherent transceiver technology is then expected to play an ever more important role. Photonics and electronics with higher bandwidths beyond 100 GHz will play a crucial role. Integration of thin-film LiNbO3 modulator onto a Silicon Photonics platform is shown to be a viable option to meet the needs for new generations of optical transceivers. Front-end electronics such as linear modulator drivers and transimpedance amplifiers can rely on traveling-wave design approaches to allow continued bandwidth scaling despite (relative) slowing transistor speeds. Novel wireline data converter architectures can be used to overcome limitations of existing implementations. Maintaining signal integrity from photonics and electronics can be facilitated using both 2.5D and 3D integration approaches. While the introduction of novel materials and architectures will require time to further mature, optical transceivers operating at baudrates up to and beyond 200 Gbaud are now just beyond the horizon.**

***Index Terms*—Photonic integrated circuits, electronics integrated circuits, wireline data converters, coherent communications, optoelectronics, silicon photonics.**

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I. Introduction

GENERATIVE artificial intelligence (AI) applications rely on foundational and large language models, whose largest implementations now contain over a trillion parameters [1, Figure 1.3.5]. Training such models requires unprecedented amounts of computational power. Fig. 1 illustrates the published amount of compute used for training some notable machine learning models, expressed as floating point operations (FLOPs, in particular petaFLOPs) versus year published (data taken from [2]): a rapid exponential growth has occurred and is still on-going [3]. The underlying hardware relies on large amounts (tens of thousands, set to scale to hundreds of thousands) of central, graphical or tensor processing units (CPUs, GPUs, TPUs, generally abbreviated as xPUs) [4], [5]. These processors are arranged into modules, boards and racks, all interconnected through a hierarchical network. At the core of these networks are electronic switches, which route traffic throughout the data centers that host the compute hardware. In some cases, optical circuit switches are used or considered to create reconfigurable machine learning clusters [6], [7]. Training large-scale machine learning models is done in parallel over large collections of processing

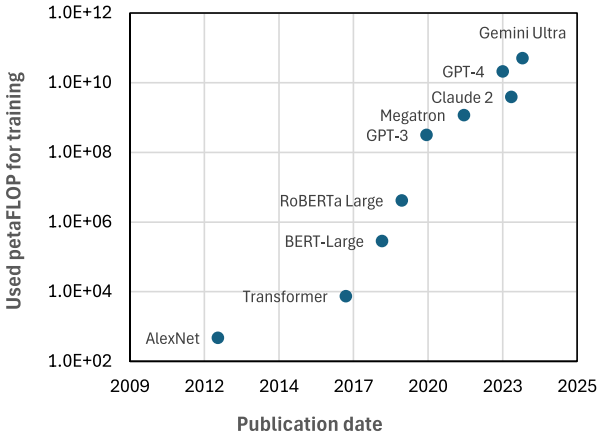

Fig. 1. Compute capacity used for training AI systems [2].

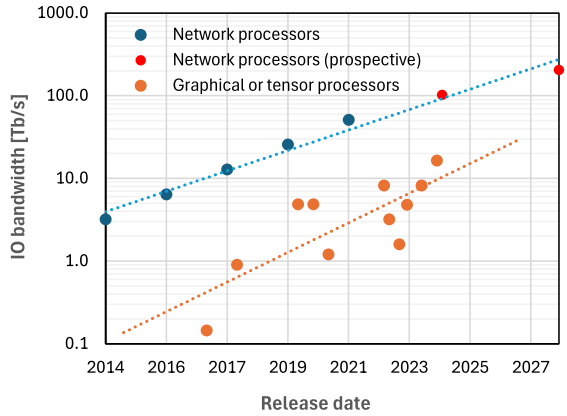

Fig. 2. Input and output bandwidth of network processors and graphical or tensor processors [4].

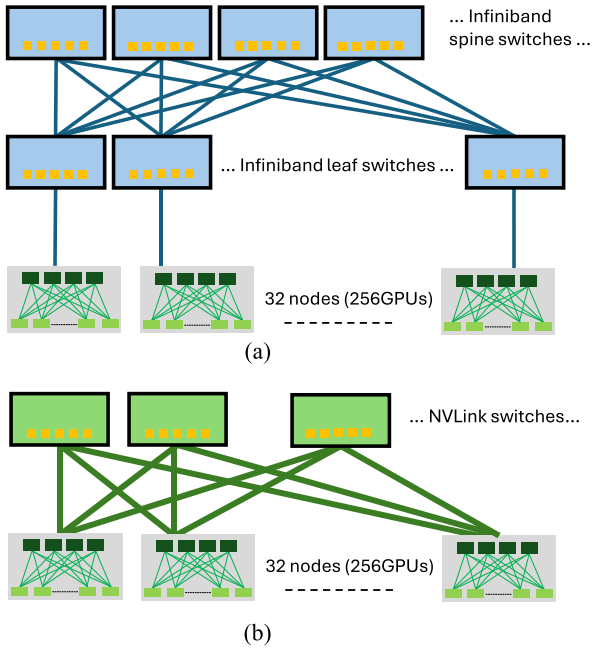

Fig. 3. Compute and network configurations relying on high-speed interconnect for machine learning applications: (a) Leaf and spine, (b) 2:1 tapered fat free.

units, and therefore involves significant data traffic on top of accessing nearby memory. As a result, the need for IO bandwidth (which does not include the interface to high bandwidth memory chips) of both xPUs and network processors continues to grow exponentially. Fig. 2 shows IO bandwidths of selected chips or platforms, including both realizations and projections in the case of network processors: the highest demonstrated IO bandwidth today is 51.2 Tb/s, while it is expected that 100 Tb/s and even 200 Tb/s devices will emerge by the end of the decade [8].

Fig. 3 shows an example how GPU clusters are connected using Infiniband (or Ethernet) interconnect and switches (top) or NVLink and NVSwitch technology (bottom) [9]. These networks rely on short-reach optical transceivers with reaches ranging from 50 m up to 500 m and even up to 2 km. Transceiver capacities range from 400 G and 800 G to 1.6 T, with for example the Ethernet Alliance projecting a need for 3.2 T capable transceivers by 2030 mostly driven by AI and machine learning (ML) applications [10]. Such capacities are achieved through multiplexing different lanes, relying on space-division multiplexing (using multiple parallel fibers) or wavelength-division multiplexing (WDM, multiple wavelengths per fiber). State-of-the-art short-reach interconnect uses 200 G/lane intensity-modulated, direct detect (IMDD) technology, using a 106 Gbaud PAM-4 (4-level pulse level amplitude modulation) modulation format [11]. Apart from a rapidly growing need for bandwidth, training AI models also benefit from reduced latency in the optical links connecting the xPUs [12]. The very high amount of deployed xPUs necessary to train the largest AI models, also bring forward the need to further drive down the energy consumption of the transceivers, as well as improving their reliability and reducing failure rates.

Different approaches can be used to integrate the optical transceivers with the xPUs and network processors: Fig. 4 provides an overview. Widely adopted in industry today are so-called pluggable optical transceivers: these modules house the optics (modulator, detectors, wavelength (de-)multiplexers and lasers), front-end electronic (modulator driver and transimpedance amplifier arrays) and in many cases a DSP and SerDes (retiming) chip, usually implemented using a scaled CMOS process. In addition, auxiliary circuitry and components for control and cooling may be integrated in the module. As shown in Fig. 4, note that the CMOS DSP&SerDes chip in the module handles signal processing to overcome impairments not only of the optical channel (line-side) but also the electrical channel connecting the xPU with the module (client-side). This can be an expensive proposition especially from a power consumption point-of-view. If the convolved response of the electrical and optical channel can be overcome by signal processing only in the xPU itself, then the power-hungry DSP can be eliminated from the pluggable module: this is referred to as so-called linear pluggable optics (LPO) [13]. An additional advantage is the reduction of the overall latency of the link, which is critical for AI/ML applications. Note that the front-end electronics need to be linear, and includes analog-domain equalization (e.g., continuous-time linear equalization, CTLE) to overcome the losses of the electrical link (which, for example, can be as high

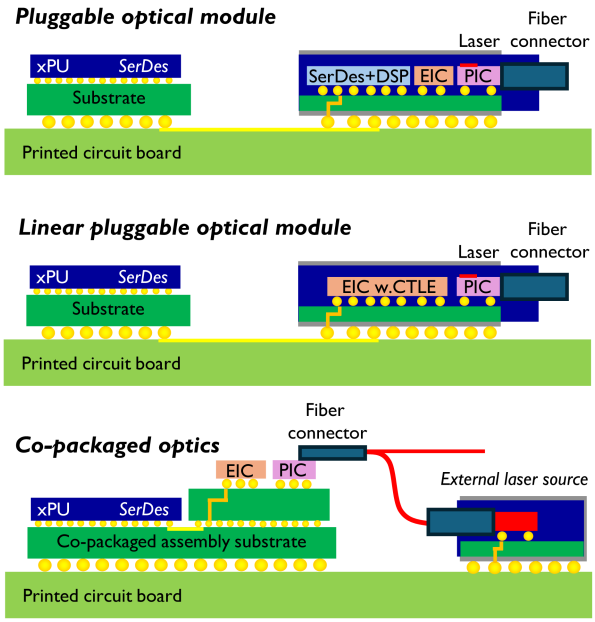

Fig. 4. Integration approaches for optical transceivers (SerDes: serializer/deserializer, DSP: digital signal processing, PIC: photonic integrated circuit, CTLE: continuous-time linear equalizer, EIC: electronic integrated circuit, xPU: processing unit).

as 12 dB for ~53 Gbaud PAM-4 links) and the constituent components [14]. Hybrid forms such as linear receive optics (where only the transmit-side still uses retiming and/or DSP inside the module) may be considered in case the bandwidth and/or linearity of the optical modulator are not sufficient to close the optical link budget. Another approach to eliminate the impact of the electrical connection between pluggable module and the xPU is called co-packaged optics (CPO), see Fig. 4 [15]. In this approach, the optical transceiver is actually integrated in the same package as the xPU, by integration on a suitable substrate or interposer. Significant challenges in terms of integration need to be overcome. In particular, due to the high power dissipation of the xPU, the temperature of the devices in the package can be high, in which case it is advantageous to use an external laser source (ELS). In addition, stringent requirements need to be put on the reliability of the optics in the CPO module, to avoid reducing the lifetime of the resulting (expensive) xPU. Finally, the assembly chain needs to be constructed in such a way that only known-good photonic devices or integrated circuits are assembled with known-good xPUs, to avoid a costly drop in overall yield.

This paper explores different options to scale transceiver capacity towards multiple Terabit/s both from a system and technology point of view. Section II discusses scaling options for optical transceivers, while Sections III and IV provide an overview of relevant photonic and electronic technologies respectively. Section V addresses options for integration of photonics and electronics, a conclusion and outlook is provided in Section VI.

II. Scaling Options for Optical Transceivers

Three different options exist to continue scaling optical transceiver capacity. Firstly, one can scale the number of parallel fibers or number of wavelengths per fiber (or a combination of both), although, this only provides linear scaling against an exponentially increasing demand for higher capacity. Increasing the number of lanes through wavelength division multiplexing can eventually be limited by linear crosstalk introduced by the required wavelength multiplexer and demultiplexer components. So far, short-reach optical interconnect applications do not even remotely approach the maximum capacity of standard single-mode optical fiber.

Secondly, the baudrate on each optical lane can be scaled, although this will eventually be limited by the achievable signal-to-noise ratio and bandwidth of the link and used components. Indeed, note that the receiver's optical sensitivity worsens when its detection bandwidth widens, as this raises its noise floor. While increasing the transmit power helps, non-linear impairments such as four wave mixing can become limiting factors. Polarization interleaving can help mitigate its impact, the resulting complexity is readily addressed by integrating the necessary optical functionality in a photonic integrated circuit (PIC) [16]. Chromatic dispersion can also become limiting even in the O-band for sufficiently long reaches and high baudrates. Techniques such as introducing chirp through appropriate biasing of electro-absorption modulators [17], combined differential (push-pull) and common-mode (push-push) drive of a Mach-Zehnder modulator [18], [19] or IQ modulation [19] are known techniques to mitigate the detrimental impact of chromatic dispersion. Of course, digital signal processing (DSP, including both pre-equalization at the transmitter side and receiver-side equalization) is widely used today to compensate chromatic dispersion, at the expense of added power consumption and complexity.

Finally, higher-order modulation formats can be used to increase the number of bits per transmitted symbol, although this only provides logarithmic increase in capacity. Again, the limit will be the required signal-to-noise ratio to achieve a certain bit-error rate. A combination of all three may be necessary to further scale capacity, and the exact choice will be application dependent.

For the following discussion, the rate overhead associated with error correcting codes (notwithstanding the fact that these error correcting codes are essential for closing the link budget of many optical link classes) will be neglected without affecting the conclusions. Looking back at 25 G/lane technology which was used to realize 100 G short-reach optical transceivers constructed from 4 such lanes, different steps can be distinguished on the route to today's 800 G capable transceivers. Industry took a first major step by doubling the spectral efficiency to 50 G/lane through ~25 Gbaud 4-level pulse amplitude modulation (PAM-4) [21]. This allowed to realize 200 G optical transceivers relying on essentially the same photonic and electronic processes (approximately the same modulation and detection bandwidths of the optics and the front-end electronics) as the 25 G/lane devices. Significant effort was required to realize *linear* opto-electronic front-ends [22] and PAM-4 capable SerDes (mixed-signal or DSP-based) with a power consumption and physical size that fits pluggable modules, but no new process development was necessary [23], [24]. Further leveraging the same photonic and electronic processes, in a next step the number of lanes was

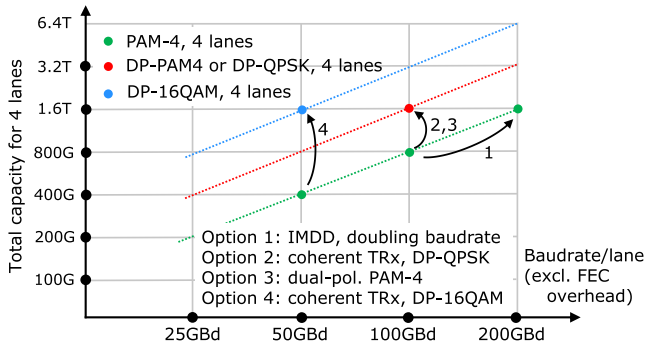

Fig. 5. Scaling options towards 400 G/lane capacity, 4 lanes making a 1.6 T transceiver.

increased from 4 to 8, thus realizing 400G transceivers. Given the high component count for such 8-lane (8 transmitters, 8 receivers) transceivers, obviously the use of photonic integrated circuits is beneficial in terms of fabrication cost, provided the process has sufficiently high yield. However, doubling the number of lanes one does not gain much in terms of energy efficiency (pJ/bit) nor frontplate density on the switches, and reduces production yield compared to 4 lanes. This explains the move towards 100 G/lane (∼53 Gbaud PAM-4) technology relying on new photonic and electronic processes, from which again 4-lane 400 G optical transceivers were built [25], [26], [27], [28]. 800 G modules were first constructed using an 8 × 100 G/lane approach. As soon as the technology to achieve >50 GHz optics and electronics became available, 4 × 200 G modules were being introduced, including the necessary 200 G/lane capable DSP [29].

For emergent 1.6 T transceivers, the same approach is being followed: first 1.6 T transceivers are using an 8-lane, 200 G/lane approach [30]. Scaling to 400 G/lane can then be a next step: one option is to again double the baudrate to ∼200 Gbaud PAM-4 (not taking into account overhead for error correcting as mentioned before), however given the need for >100 GHz opto-electronics and >200 GS/s wireline data converters it is worthwhile to explore other options as shown in Fig. 5.

A first step could be to use higher-order multilevel modulation formats such as PAM-6 or even PAM-8 [31]. To achieve 400 G per lane capacity, 160GBaud PAM-6 (5 bits per two symbols, resulting in 36 different 2-symbol words of which 32 are used) or 133 Gbaud PAM-8 (3 bits per symbol) is then required. While the advantage of such modulation formats is of course the reduced bandwidth and wireline data converter sampling rates, the drawback is the significantly higher required signal-to-noise ratio to achieve a given bit-error rate. For example, PAM-8 requires a 6.3 dB higher SNR compared to PAM-4, which may make closing optical link budgets challenging.

An alternative (see Fig. 5) is to exploit polarization multiplexing and optical phase modulation to further increase the spectral efficiency and hence capacity per lane while relying on existing ∼50 GHz EO/OE bandwidth photonics and electronics. A first interesting option is to independently generate two signals using for example 200G (∼100 Gbaud) PAM-4, and multiplex both signals on orthogonal polarizations using a polarization beam combiner before coupling into standard single-mode fiber [32], [33]. At the receiver side, a polarization beam splitter and polarization controller [34] can be used to demultiplex both polarizations, after which regular direct detection using two photodetectors can be used to recover the signals from both polarizations. Feedback from the DSP [32] or marker tones (added to e.g., a single polarization at the transmitter) can be used to appropriately tune the polarization controller [35]. While the disadvantage of this approach is the higher link loss due to the polarization beam splitters and tracker (which can be overcome by simply increasing the laser power), the advantage is that no new (higher baudrate) DSP chip nor high-speed front-end electronics needs to be developed. The additional complexity of the polarization beam splitters and polarization tracker can be easily integrated into a single PIC.

Another option is ∼100 Gbaud (the exact baudrate depends on the selected error correcting code) dual-polarization quadrature phase shift keying (DP-QPSK) which allows 400 G/lane capacity relying on coherent technology. Optical functionality such as polarization splitting/combining, and optical hybrids are required but these can be readily integrated into the PIC with marginal additional cost [36], [37]. Conventional coherent transceivers widely used for long-haul and metro applications rely on intradyne detection (the local oscillator is tuned to within a few GHz of the transmit laser) with mixing relying on optical hybrids. A critical function is then wavelength monitoring and locking to ensure the local oscillator laser remains tuned to within a few GHz of the transmit laser irrespective of temperature fluctuations [38]. Polarization rotation, recovery of the remaining optical frequency difference and phase recovery are done through digital signal processing after high-speed analog-to-digital conversion [39]. This approach, while allowing highly sophisticated signal processing, can be expensive (due to the required circuit area on an advanced CMOS chip) and power hungry. Therefore, other approaches to perform polarization rotation as well as optical frequency and phase recovery have been pursued through both optical and analog/mixed-signal techniques, resulting in coherent transceiver with power consumption in the lower pJ/bit region [35], [40], [41], [42].

Another option is ∼50 Gbaud DP-16QAM, leveraging existing 400 ZR technology but with simplified DSP (dependent on selected wavelength band and target fiber reach). With the power and density for coherent and IMDD DSP converging [43, Fig. 4], the differential to move to coherent technology then mainly originates from the need for a cooled laser with improved linewidth (e.g., <500 kHz) to provide the local oscillator. Indeed for example for 400G capable modules, a coherent transceiver was found to consume x1.5 higher power compared to an IMDD transceiver [43, Fig. 4]. In [44], the coherent DSP chip (assuming 5 nm CMOS, including ADCs, DAC, and DSP) was estimated to use only 25% more power compared to an IMDD chip with the same capacity (DP-16QAM vs. 4-channel PAM-4, for a total capacity of 425 Gb/s). Dependent on the system-level implementation, either a single higher power laser (whose output is split between the transmitter and the local oscillator) or two lasers per module can be used. Alternatives that avoids such additional laser are interferometric detection schemes.

It is interesting to compare these different options from an optical budget point-of-view as a function of the modulator

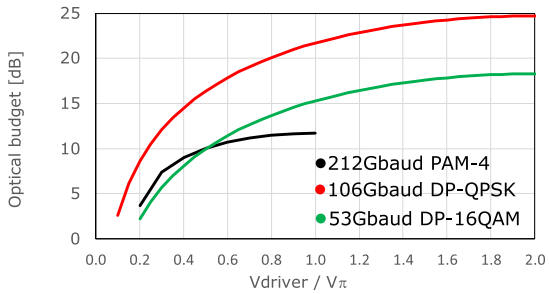

Fig. 6. Optical budget as a function of relative drive voltage for different 400 G/lane scaling options (laser power: +10 dBm, laser RIN: −145 dB/Hz, modulator excess loss: 4 dB (2 dB extra loss for polarization combiner), photodetector responsivity: 0.7 A/W, input-referred noise density receiver: 20 pA/Hz$^{1/2}$, 3 dB receiver bandwidth: 60% of baudrate, hybrid loss: 10 dB incl. polarization splitting, coherent receiver common-mode rejection: 20 dB, laser coherent transceiver 50/50 split between DP-IQ modulator and local oscillator, target bit-error rate: 2×10^{-4}).

drive voltage (a measure for the modulator driver's power consumption, note that the driver's power consumption scales quadratically with the drive voltage). Fig. 6 shows achievable optical budgets under the simplifying assumptions that sufficient electro-optic bandwidth is available in the opto-electronic components such that impact of intersymbol interference is negligible, the reach and wavelength is such that the penalty due to chromatic dispersion is negligible and the linewidth of the lasers is small enough that resulting penalty is negligible. This optical budget therefore provides a best-case baseline. For low drive voltages (lowest energy consumption for the driver electronics) up till 0.5xV_π (halfwave voltage), PAM-4 modulation slightly outperforms DP-16QAM, mainly due to the high loss of the modulator in the coherent case. Above 0.5xV_π, the loss of the modulator for the DP-16QAM case becomes sufficiently low such that the sensitivity gain due to mixing with the local oscillator outperforms PAM-4. DP-QPSK gives best performance irrespective of the modulator drive voltage, which is mainly due to its fundamental sensitivity advantage: the spacing of the symbol points in the constellation is largest (for a fixed average optical power). If no transmit-side equalization is necessary, DP-QPSK has the further advantage that no linear drive electronics would be required, simplifying the overall transmitter and reducing its power consumption. The picture painted here will change depending on the amount of chromatic dispersion and bandwidth limitations in the transceiver components, and the sophistication of DSP equalization to overcome these. Clearly, ∼100 Gbaud DP-QPSK can be an interesting option for future 400 G/lane transceivers.

III. Photonics for 400 G/Lane Transceivers

Scaling photonics to enable 1.6 T, 3.2 T, … transceivers while relying on 200 G/lane and 400 G/lane channels will require significant advances in the underlying photonics platforms.

Regarding passives, firstly broadband coupling to single-mode fibers or polarization maintaining fibers (in the case of external light sources) is critical, especially when large amounts of wavelengths need to be supported. For parallel fiber interfaces, low-loss (<1 dB) and low-pitch fiber couplers (either vertical using grating couplers or horizontal through edge couplers) are essential, the latter to minimize the area on the PIC. Wavelength multiplexers and demultiplexers with low insertion loss and low crosstalk terms are critical, when scaling to dozens of wavelengths. For example, the CW-WDM MSA (continuous-wave wavelength division multiplexing multi-source agreement) envisions the use of up to 32 200 GHz spaced wavelengths, spanning 36 nm in the O-band [45]. As such high wavelength counts may result in significant amounts of optical power, care needs to be taken to ensure non-linear (e.g., due to two-photon absorption in silicon-on-insulator (SOI) waveguides) and even damage thresholds inside optical waveguides are not exceeded [46]. When operating over a large temperature range (e.g., 0 °C to 70 °C environmental temperature range for data center equipment can be a typical requirement, noteworthy is that some data center operators have revised the lower temperature boundary to 15 °C), (de-)multiplexer central wavelengths need to track the laser wavelengths or vice-versa. Splitters or taps to monitor e.g., power inside the PICs provide critical auxiliary functionality. Coherent transceivers will require integrated optical hybrids, with low loss and low phase errors (typically <5degrees over the intended optical bandwidth) at their outputs. Polarization-mode multiplexing requires devices such as polarization beam combiners or splitters, rotators, or active polarization controllers. Such devices need to have low insertion loss, and good extinction on their complementary ports. Note that in some (mainly telecom, such as amplified DWDM – dense wavelength division multiplexing - systems) applications, the coherent receiver may need to be able to handle significant optical powers, especially if the receiver's selectivity is used to filter a given wavelength from an incoming set, possibly with added amplified spontaneous emission (ASE) noise. For example, OIF implementation agreement OIF-IC-TROSA-01.0 (implementation agreement for integrated coherent transmit-receive optical sub assembly) specifies that the coherent receiver needs to be able to handle up to +16 dBm optical input power: reducing the local oscillator power can then be used to keep the total generated photocurrents to reasonable limits [47]. Of course, lowering the local oscillator power goes hand in hand with a reduction in the achievable signal-to-noise ratio, since the signal photocurrent is proportional to the squareroot of the local oscillator optical power. Variable optical attenuators can be used to control the input power as well. Finally, as mentioned above, optical wavelength monitors are essential to lock the local oscillator wavelength (generated by a cooled laser) with respect to the target signal wavelength [38].

High-speed external modulators and detectors are obviously critical to convert signals from/to the electrical domain to/from the optical domain. Supporting ∼200 Gbaud operation will require an EOE modulator bandwidth of at least 100 GHz, with similar numbers at the detector side. Scaling towards ∼240 …280 Gbaud as considered in for example the OIF 1600 ZR project will push those bandwidth requirements even beyond 140 GHz.

Lasers and semiconductor optical amplifiers (SOAs) are the final set of important photonic components on which transceivers rely. Considering pluggable transceivers, the laser is integrated

directly into the transceiver package and hence integration (either monolithic or heterogeneously) on the PIC is the preferred route to reduce cost. For co-packaged optics, where the transceivers are located close to the xPUs, the laser is currently preferably located outside the module under the form of a so-called external laser source. This reduces the temperature at which the laser needs to operate, and allows to replace the laser in case it fails without the need to replace the entire processor. The laser indeed is usually the component with the lowest lifetime. The disadvantage of placing the laser outside of the co-packaged optics modules is the higher insertion loss associated with the different fiber-coupling interfaces. Lasers that can continue to operate at temperatures up to 100 °C and beyond are therefore of significant interest: one option are quantum-dot GaAs lasers, which can operate in the O-band and deliver high powers up till very high temperatures [48].

A. *Integrated Photonic Platforms*

Indium Phosphide (InP) processes allow the integration of multiple photonic devices, including waveguides, modulators, detectors and gain sections to construct lasers and optical amplifiers. A dual-channel 800 Gb/s capable InP PIC that integrates the lasers, SOAs, Mach-Zehnder modulators, detectors and couplers was demonstrated to achieve up to 96 GBd operation [49]. Note that the polarization management devices (polarization beam splitter at the receiver side, combiner at the transmitter side) were not integrated. InP-based polarization rotators have been achieved, promising a route to also integrate such components eventually as soon as sufficiently high extinction ratios between the different polarizations are achieved [50]. Both transmitter and receiver were shown to have >50 GHz bandwidths. In [51], a 90 GHz InP Mach-Zehnder IQ modulator was demonstrated. An InP based electronic driver was flip-chip integrated onto the PIC: using a highly optimized flip-chip interface and peaking in the modulator driver EIC, over 100 GHz bandwidth was achieved. At the detector side, [52] demonstrated a module containing a waveguide InP detector, with an overall bandwidth of 146 GHz, promising for >200 Gbaud applications.

Silicon photonics with its higher integration density and manufacturing throughput (due to the larger wafer sizes such as 200 mm and 300 mm) can integrate both photodetectors (e.g., Ge devices) and various modulators that are suitable. Polarization management devices with good extinction ratios can be readily integrated [53], [54]. As mentioned before optical hybrids with low phase errors have been demonstrated [36], [37]. Wavelength multiplexers and demultiplexers can be integrated relying on for example cascaded Mach-Zehnder interferometers (MZIs) [55] or microring resonators [56]. As outlined in [57], Silicon Nitride (SiN) waveguides and associated passive structures can offer significant benefits over conventional pure SOI based silicon photonics platforms. In particular, SiN allows operation over wider optical bands, and have lower propagation losses compared to SOI-based waveguides. Finally, the non-linear threshold of SiN waveguides is far higher than SOI waveguides which can be useful in applications with very high wavelength counts or coherent transceiver applications with significant input signal powers as explained before. New generations of Silicon Photonic platforms are directly integrating Silicon Nitride waveguide layers [58].

Lasers and optical amplifiers are not native to silicon photonics and require heterogeneous integration which is addressed in the next paragraph. The previously mentioned target of 500 kHz linewidth for the laser is easily achieved by through hybrid integration of an InP reflective semiconductor optical amplifier (RSOA) with a SiN external cavity [59]. High-speed silicon Mach-Zehnder modulators based on carrier depletion optical phase shifters face trade-offs between insertion loss and bandwidth on one hand versus required drive voltage on the other hand. Indeed, increasing the length of the phase shifters reduces the half-wave voltage V_π, but increases the insertion loss and reduces the bandwidth due to the increasing capacitance (in the case of a lumped modulator) or RF losses (in the case of traveling wave modulators) of the electrodes. For a given optical phase shifter technology, the trade-off between drive voltage and modulator length is captured by the half-wave voltage-length parameter $V_\pi L$. This parameter depends on both the material from which the modulator is constructed and its detailed design (cross-section and electrodes). Typical $V_\pi L$ values for Silicon Photonic Mach-Zehnder modulators (plasma dispersion based) range between 0.8 Vcm up to 3.0 Vcm [60]. The optical insertion loss of the phase shifter can range from 8 dB/cm up to 27 dB/cm [60]. Lower $V_\pi L$ products can be achieved by relying on InP, for example in [61] a $V_\pi L$ as low as 0.7 Vcm was achieved. Recently, the use of thin-film LiNbO3 has raised significant interest: the $V_\pi L$ product is typically about 2 Vcm [62]. The advantage of this material platform lies with the low optical losses of the phase shifters: below 0.1 dB/cm has been demonstrated in [63] for example. The bandwidth of these modulators are essentially only limited by the RF losses of their electrodes, implying high bandwidths can be achieved even for long modulators. Again in [63] the authors achieved ∼100 GHz for a 5 mm long modulator. If the modulation rate is sufficiently low, a lumped design can be used [64]. High baudrate operation requires a traveling wave design: 37 GHz bandwidth was achieved in [65] for a Silicon Photonic modulator, with a V_π of 10.5 V and insertion loss less than 1.5 dB. The trade-off between V_π and bandwidth can be broken to some extent through the use of e.g., optical equalization [66]. The Mach-Zehnder modulator in [67] achieved 67 GHz bandwidth by segmenting the traveling wave phase shifters into three parts: this has the disadvantage that each segment requires a dedicated driver increasing transmitter power consumption. A remarkable result for Silicon Photonic modulators was achieved in [68], where the modulation efficiency of the optical phase shifters was enhanced by slowing the light through the use of Bragg gratings. The resulting bandwidth of the 124 μm long modulator was 110 GHz, with an overall insertion loss of 6.8 dB (stemming from both the phase shifters and losses due to routing waveguides and directional couplers). The optical bandwidth was 8 nm, limited by the use of the Bragg gratings in the optical phase shifters. Up to 3 dB extinction ratio was measured with a 5 V_{pp} drive voltage.

Carrier depletion optical phase shifters can also be arranged in small radius microrings, which allow simultaneous high-speed modulation and multiplexing functionality [69]. In [70], up to 240 Gb/s (120 Gbaud) PAM-4 modulation rate was achieved by using a ring with a small 4 μm radius. The small radius also enabled a 16.3 nm free spectral range (FSR), which allows to place up to 12 DWDM channels at 200 GHz spacing. Rather than optimizing for the highest modulation bandwidth, rings can also be optimized to achieve best possible electro-optic (minimizing required drive voltage for modulation) and thermo-optic efficiency (minimizing the required heater power for tuning the ring resonance) [71]. The resonance frequency of microrings is highly susceptible to temperature and manufacturing tolerances. To align the modulator ring resonance with respect to the incoming laser wavelength, heaters are required whose power consumption may be a significant fraction of the total power consumption of a transceiver [72]. An option to reduce the power consumption due to the heaters is to remove part of the silicon surrounding the heater itself: [73] showed how this approach can help to improve the heater efficiency by a factor x3. One important advantage of a microring is that these devices represent only a small capacitive load to the electronic driver. This allows direct connection to CMOS style drivers [74].

The drawback of silicon photonic microrings is the requirement for additional heaters to tune their resonance with respect to the incoming laser wavelength: the additional power consumption and associated (potentially complex) control circuitry may be difficult for some applications [75], [76]. An alternative is then to use GeSi based Franz-Keldysh effect electro-absorption modulators (EAMs) [77], [78]: again from an electrical point-of-view these device represent a small capacitive load. Care needs to be taken though that the electronic driver can handle the current generated by the EAM when in its absorptive state [79]. A critical advantage when using GeSi EAMs integrated in an SOI-based silicon photonic platform is the fact that both its terminals (cathode and anode) are electrically fully isolated. This allows to apply a differential drive to the EAM, and through an appropriate driver design simultaneously the necessary dc-bias [79], see Fig. 7. The EOE bandwidth of these modulators can be in excess of 50 GHz for well-designed devices [78]. A silicon photonic IQ transmitter relying on EAMs was demonstrated in [80], showing up to 100 Gbaud single-polarization QPSK generation. Franz-Keldysh GeSi EAMs integrated in silicon photonics can only be used in the C-band, however recently progress is being made in the integration of quantum-confined stark-effect (QCSE) EAMs suitable for the O-band [81].

High-speed detectors can be realized relying on Ge and GeSi photodiodes: in [82] beyond 50 GHz bandwidth was reported for a C-band GeSi detector. By sandwiching a Germanium fin between complementary in situ-doped silicon layers, detectors with 265 GHz (0.3A/W responsivity at 1550 nm) and 240 GHz (0.45A/W responsivity at 1550 nm) 3 dB bandwidths were reported in [82], more than sufficient for next-generation 400 G-capable optical receivers. Remarkably, this bandwidth also far exceeds what has been reported till now for InP photodetectors. With increasing baudrates, the receiver bandwidth needs to scale accordingly, which increases the total receiver noise and hence reduces the achievable signal-to-noise ratio. One solution is the use of avalanche gain: [83] reported a 35 GHz bandwidth at 2A/W responsivity in the O-band (1310 nm) for an integrated avalanche photodetector.

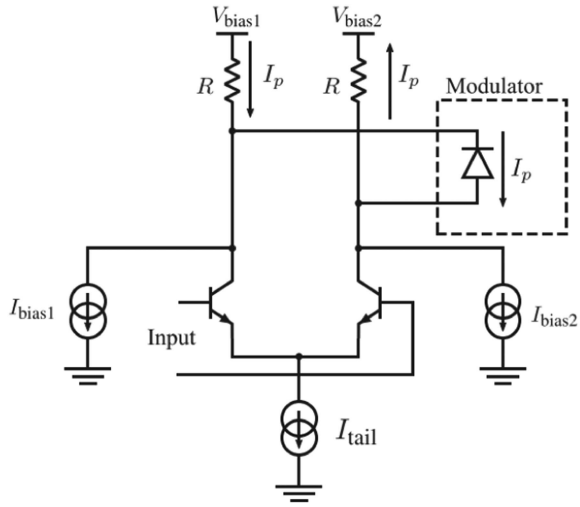

Fig. 7. Differential drive of a GeSi EAM integrated in a Silicon Photonic platform: Vbias1 > Vbias2 to apply a reverse bias to the modulator.

B. Extending Functionality and Performance Through Heterogeneous Integration

As outlined in the previous paragraph, neither InP nor Silicon Photonic processes currently allow to monolithically integrate the full range of devices necessary for fabricating complete transceivers, especially in the case of complex coherent transceivers.

In particular in the case of silicon photonics, neither lasers nor optical amplifiers are native to the process: heterogeneous integration of III-V optical gain elements is required to facilitate such devices. In addition and as discussed before, a high bandwidth (>>100 GHz) silicon photonics modulator that can operate over a wide optical band with low optical insertion loss remains an elusive target, even for the most sophisticated carrier-depletion based designs. An interesting option are thin-film lithium niobate (LiNbO3) modulators, which as explained before have shown to achieve bandwidths beyond 100 GHz, with very low optical losses (e.g., 0.1 dB/cm to 0.2 dB/cm optical phase shifter loss) and can operate with low half-wave voltage $\times$ length product $V_\pi L$ (e.g., 1.7 Vcm) [62], [63], [84], [85].

An interesting technique to heterogeneously integrate such devices is micro-transfer printing [86], [87], see Fig. 8. Starting from a source wafer with fabricated devices (for example a III-V wafer with optical gain sections), MEMS etching techniques are used to almost fully release coupons (sometimes also called chiplets in this context) from the wafer, apart from small bridges or tethers. This typically requires an additional so-called release layer with suitable material properties (e.g., etch selectivity) to be processed during fabrication of the source wafer. The

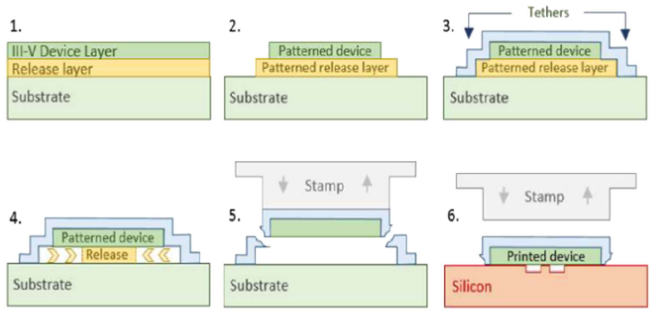

Fig. 8. Micro-transfer printing of (for example) optical gain sections from a III-V source wafer onto a Silicon target wafer. Reproduced with permission from G. Roelkens et.al., IEEE J. Sel. Topics Quantum Electronics (2023).

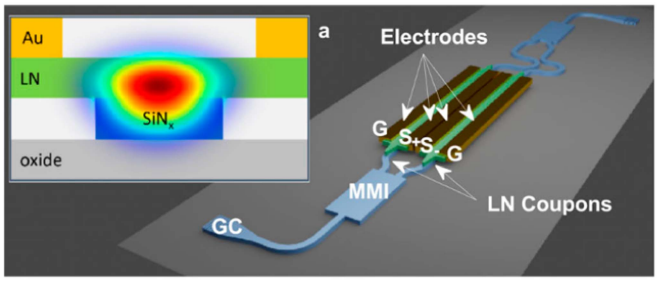

Fig. 9. Mach-Zehnder modulator constructed from LiNbO3 optical phase shifters transfer printed on SiN waveguides. Reproduced with permission from T. Vanackere, APL Photonics, 2023.

release layer then facilitates undercutting the device to be transfer printed. Next, a soft stamp (fabricated from for example poly-dimethylsiloxane PDMS) with posts corresponding to the location of the coupons is laminated against the source wafer. By moving the stamp away from the source wafer at an appropriate speed, the coupons are broken free from the source wafer and attach to the posts on the stamp. The thus loaded stamp is then moved over to the target wafer, where by again laminating the stamp to the target wafer and moving away at an appropriate speed the picked up coupons are transferred from the stamp to the target wafer. Typically, the target wafer needs to be coated with a thin adhesive layer, such as for example divinylsiloxane-bisbenzocyclobutene (BCB) [88], [89]. By carefully aligning both the stamp with the target using state-of-the-art equipment, very high positional accuracies better than $+/-0.5\ \mu$m (3σ) have been demonstrated with this technique [87]. When printing on silicon photonic wafers, optical gain elements can be printed inside cavities (openings in the back-end of the wafer) where the optical waveguides have been exposed, which allows to fabricate lasers or optical amplifiers. Arrays of devices can be transferred in this way, thus facilitating massively parallel assembly of lasers or optical amplifiers. The approach works for a wide variety of source material systems, such as InP but also GaAs quantum dots [90], [91].

Micro-transfer printing also works for integrating coupons with very high aspect ratios, and therefore can be used to integrate thin-film $LiNbO_3$ optical phase shifters thus constructing high-speed Mach-Zehnder modulators [92]. As shown in Fig. 9,

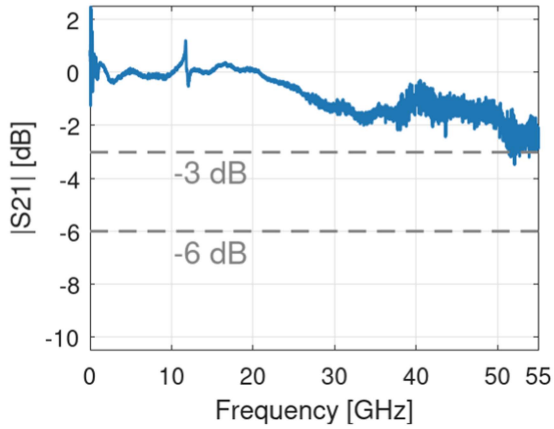

Fig. 10. Measured small-signal response of the micro-transfer printed thin-film LiNbO3 modulator. Reproduced with permission from T. Vanackere, APL Photonics, 2023.

such an integrated device consists of LiNbO3 coupons integrated on top of SiN optical waveguides. The coupons contained tapers on both interfaces reduce coupling losses when transitioning to and from the SiN waveguides to the hybrid waveguides. GSSG gold electrodes were patterned to enable high-speed driving. The device is 2mm long with a half-wave voltage Vp of 14.8 V, the insertion loss was 3.3 dB. Fig. 10 shows the measured frequency response of the proof-of-concept device demonstrating ~50 GHz bandwidth. Further research is on-going to integrate longer modulators with improved performance, by e.g., printing on high-resistivity substrates. The micro-transfer printing technology can also be used to integrate III-V (InP) phase modulators onto the silicon photonic platform, again with a view to equip this platform with high bandwidth modulators.

IV. High-speed Electronics

With baudrates now needing to scale beyond 200 Gbaud, careful co-development of the high-speed electronics (modulator drivers and transimpedance amplifiers) that interface with the optics is ever more critical [93]. Some processes offer monolithic integration of both photonics and electronics [94], [95], however for the baudrates that would be required for 400 G/lane applications, new process generations are necessary whose cost may be prohibitive and are therefore not considered further in this paper.

A. Front-end Electronics

Modulator drivers and transimpedance amplifier intended for ~53 …64 Gbaud applications can still be readily implemented using cascades of suitably designed amplifier stages [25], [96], [97]. However, with required bandwidths (50 …70 GHz for 200 G/lane, >>100 GHz expected for new 400 G/lane transceivers) now becoming a significant fraction of the so-called transition frequency f_T of the used electronic processes, traveling-wave designs become an appealing option [98], [99]. Using a 130 nm SiGe BiCMOS process (f_T/f_{MAX} = 330/370 GHz), a linear modulator driver relying on a cascade

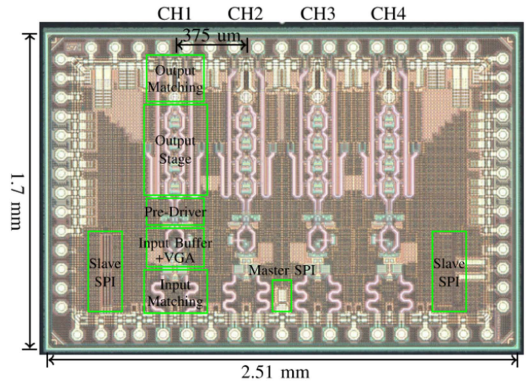

Fig. 11. Microscope image of the 4-channel linear modulator driver relying on a traveling-wave amplifier design. Reproduced with permission from S. Niu, IEEE Trans. Microwave Theory and Techniques, 2024.

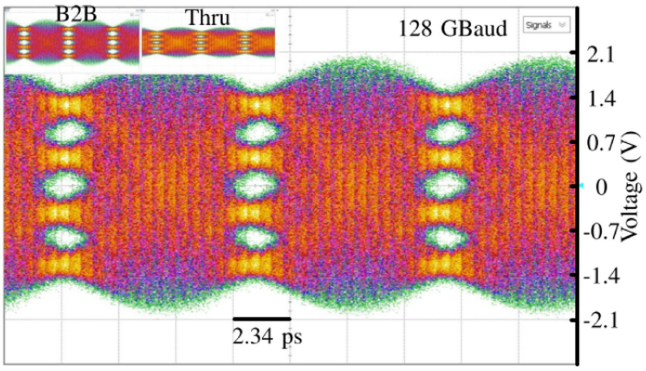

Fig. 12. 128 Gbaud PAM-4 output signal, 3.4 Vpk-pk swing measured according to IEEE 802.3 cu standard. Reproduced with permission from S. Niu, IEEE Trans. Microwave Theory and Techniques, 2024.

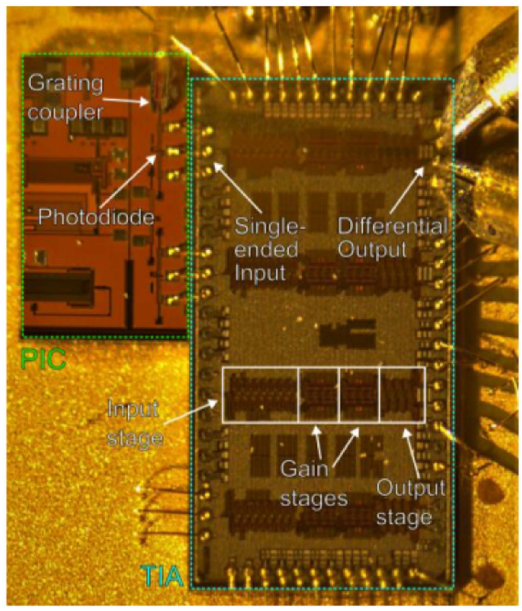

Fig. 13. Transimpedance amplifier channel wirebonded to Ge photodiode on iSiPP50G process. Reproduced with permission from J. Declercq, European Conference on Optical Communications 2023, IET.

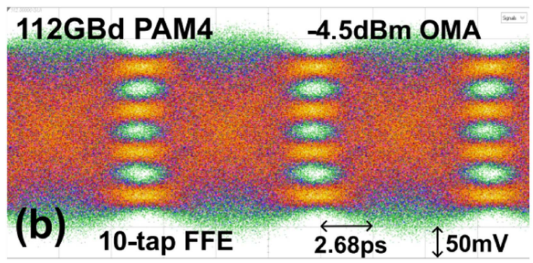

Fig. 14. 112 Gbaud PAM-4 measured at the output of the transimpedance amplifier, optical modulation amplitude onto the photodetector was −4.5 dBm, a 10-tap feedforward equalizer was applied. Reproduced with permission from J. Declercq, J. Lightwave Technol. 2025.

of a two lumped amplifiers and a traveling-wave output stage achieved >70 GHz electrical bandwidth with up to 21.8 dB gain and 3.4Vpp differential output voltage swing. Through careful layout of the transmission line sections (see Fig. 11), the required area can be kept sufficiently small to fit a 4-channel driver in a 2.51 × 1.7 mm^2 chip, allowing integration into common pluggable module form factors. Fig. 12 shows how up to 128 Gbaud PAM-4 signals can be generated with such design. At the receiver side, traveling-wave amplifier designs can help to realize frequency-transfer curves with less ripple and group-delay variation compared to lumped designs, especially when taking into account the (usually inductive) connection to photodetectors. For typical values of the inductance to the photodetector (e.g., ∼200 pH) and photodetector capacitance (e.g., ∼50 fF) this resonance occurs close to or even well inside the bandwidth of the receiver, as soon as this bandwidth needs to scale far beyond 50 GHz. The traveling-wave design presented in [99] achieved a 65 GHz 3 dB bandwidth and 6.9 kOhm gain using a 55 nm SiGe BiCMOS process. Fig. 13 shows a proof-of-concept assembly whereby one channel of a 4-channel transimpedance amplifier was wirebonded to a Ge photodiode from imec's iSiPP50G silicon photonic process. Up to 112 Gbaud PAM-4 operation was measured (see Fig. 14), with a bit-error rate of 2×10^{-4} for an input optical modulation amplitude of −4.5 dBm, whereby the receiver's output was equalized with a 10-tap feedforward equalizer.

B. Wireline Data Converters

A critical part of modern optical transceivers are the wireline analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). These enable DSP, which is necessary to overcome distortion introduced by the transmission channel, and perform data recovery which in the case of a coherent receiver consists of polarization rotation and demultiplexing, IQ and skew imbalance correction, symbol estimation, optical carrier phase & frequency estimation, and error correction. For intensity-modulated, direct detection transceivers, the sampling rate usually equals the baudrate, which requires feedback to the ADC sampling clock to align the sampling instances with the center of the incoming signal pulses [29]. In the case of coherent transceivers a rational oversampling ratio (e.g., 3/2 × baudrate)

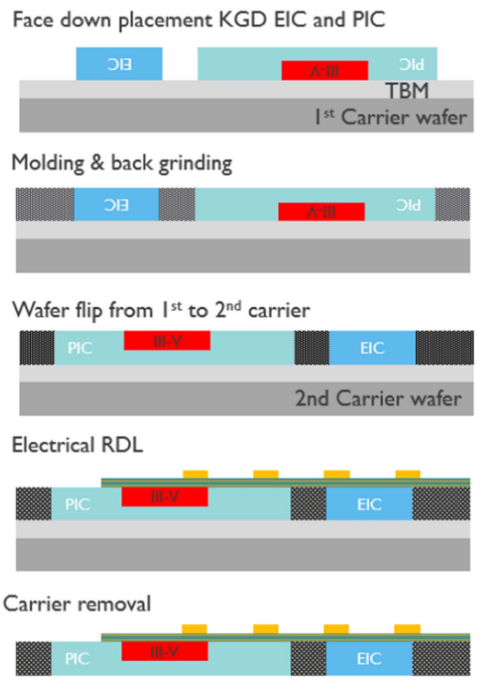

Fig. 15. Fan-out wafer-level packaging relying on wafer-level reconstitution and interconnect through electrical redistribution layers. KGD = known good die, TBM = temporary bonding material. Reproduced with permission from G. Van Steenberge, IEEE Electronic Components and Technology Conference.

is used [100]. The required resolution is typically a moderate 7…8 bits to support the most common modulation formats.

At the DAC side, first attempts to achieve the necessary sampling rates for ∼100 Gbaud transceivers relied on analog interleaving of the outputs of appropriately clocked sub-DACs. For example, in [101] up to 100 Gbaud PAM-4 was generated using a 4:1 analog interleaver, realized in 55 nm SiGe BiCMOS. The analog bandwidth of the interleaver was 73 GHz. Since then, several DAC implementations have shown how such sampling rates can be achieved directly in highly-scaled CMOS. Using a 5 nm FinFET CMOS process, [102] achieved a sampling rate as high as 160 GS/s for an 8-bit DAC with 57 GHz bandwidth in a design intended for 800 G coherent optical transceiver applications.

Wireline analog-to-digital converters are usually constructed from time-interleaved so-called successive approximation register (SAR) sub-ADCs. For example, [103] achieved up to 200 GS/s sampling rate using 256 time-interleaved sub-ADCs arranged in an array. When scaling the sampling rate, the number of time-interleaved sub-ADCs scales accordingly due to the difficulty to drastically increase the sampling rate of those sub-ADCs. The network and circuitry that samples the input signals and routes it to the sub-ADC array then can eventually become limiting in terms of bandwidth. An alternative solution proposed in [104] is to construct the high-speed ADC from an array of time-interleaved slope sub-ADCs. From an area point-of-view such a slope sub-ADC is usually the smallest today's known ADC architecture, and is therefore well suited to construct ultra-high sampling rate ADCs. Work is currently on-going to scale this concept towards ∼170 GS/s in a 5 nm FinFET 7-bit ADC prototype, jointly with a 7-bit DAC that targets the same sampling rate [11]. New generations of these wireline data converters will need to be implemented in an even more advanced CMOS node such as 3 nm or 2 nm: indeed on one hand the DSP complexity (e.g., number of logic gates) scales with increasing baudrate. On the other hand however, the coherent transceivers need to be implemented within a power consumption budget constrained by typical pluggable module form factors. The use of more advanced CMOS nodes then helps to offset the increased power consumption to some extent due to the smaller transistor sizes: the data converters are then preferably realized on the same chip given the very high data bandwidth at their input (DAC) and output (ADC) respectively. Indeed for example assuming a x1.5 (x1.2) oversampling ratio, the total data bandwidth at the output of the four 7-bit ADCs necessary for a dual-polarization, ∼100 Gbaud coherent transceiver is ∼4.2 Tb/s (3.36 Tb/s), not taking into account any redundant bits. Scaling the sampling rate even further may require external de-interleavers: using a 130 nm SiGe BiCMOS process, [105] demonstrates a 4-channel de-interleaver that facilitates sampling rates as high as 256 GS/s.

V. Integration of Photonics and Electronics

With both complexity (e.g., higher channel count with associated increased number of photonic devices per PIC) and required bandwidth (∼100 GHz to even ∼140 GHz required soon) rapidly increasing, integration of photonics and electronics plays a crucial role in the realization of new generations of transceivers. Remarkably complex devices have been realized relying on wirebonding: e.g., [93] describes a pair of 1.2 Tb/s optical transceivers that used ∼6000 wirebonds and >7.5 m Au wire. Even optical receivers with bandwidths as high as 50 GHz can still be realized with well-designed wirebonds between the photodetector and the EIC [106]. Nevertheless, clearly better solutions that are more scalable and have less parasitics (capacitance, inductance) are crucial for today's and tomorrow's optical transceivers.

A first option consists of flip-chip integration of both PICs and high-speed EICs onto silicon interposers in a so-called 2.5D assembly approach as in [107]: high-speed transmission lines and connections can thus be realized without the need for any wirebonds between PICs and EICs. The connections between PICs and the high-speed front-end EICs can be made even shorter through flip-chip mounting of the EICs directly on the top surface of the PIC in a 3D assembly approach as demonstrated in [108]. On the PIC's frontside, Cu micro-bumps with 30 μm diameter and 50 μm pitch were plated thus realizing dense and low-parasitic flip-chip interconnect with the EIC. Electrical connectivity from the PIC's frontside to its backside was facilitated using through-silicon vias (TSVs), using which interconnect with >110 GHz bandwidth has been demonstrated [109]. Cu-Ni-Sn pillars with 50 μm diameter and 150 μm pitch were plated on the backside of the PIC, on top of the redistribution layer (RDL), which allows flip-chip assembly to the package substrate through thermocompression.

The process complexity and associated cost of the 3D assembly approach relying on TSVs may be prohibitive for some

applications. An alternative assembly approach relies on fan-out wafer-level packaging (FOWLP) [110]. As shown in Fig. 15, FOWLP starts from known-good dies assembled face-down and side-by-side on a 1st carrier wafer. The dies are embedded in an epoxy mold compound, and then back-grinded to ensure a planar surface. The thus reconstructed wafer is released from the 1st carrier wafer, flipped and bonded onto a 2nd carrier wafer. An electrical redistribution layer (ERDL) based on thin-film technology can now be applied to the top surfaces of the EICs and PICs, thus interconnecting them, and also enabling connectivity to and from the outside world. In a final step, the resulting optical engines are released from their 2nd carrier wafer. Multiple pre-tested PICs and EICs can be placed with very high accuracy (down to 100 μm) during the reconstitution, resulting in optical engines with very short interconnect. The ERDL itself can have line widths and spacing as low as 10 μm, thus facilitating very high density interconnect. Multiple layers of ERDL are possible which helps to realize complex devices, built from a multitude of PICs (can be III-V or Silicon Photonics) and EICs.

VI. Conclusion and Outlook

Training large-scale machine learning models currently requires enormous amounts of compute, which in turn is putting huge pressure on short-reach optical interconnect to further scale capacity towards multiple Terabit/s per transceiver. Several system-level options to scale towards such capacities by increasing the bitrates from today's 200 G/lane towards 400 G/lane have been explored. An overview of photonic and electronic technologies and approaches to realize some of these options have been discussed, with focus on techniques for bandwidth scaling. Integration of thin-film LiNbO3 modulators onto silicon photonics using micro-transfer printing is an attractive option to create complex PICs with EOE bandwidths above 100 GHz. Ge photodetectors directly integrated in the silicon photonics have already shown bandwidths even up to 200 GHz. Traveling-wave amplifiers can be used as an essential building block to create linear modulator drivers and transimpedance amplifiers again with bandwidths likely scalable beyond 100 GHz. Leveraging the possibilities of scaled CMOS, novel approaches to wireline data converters, possibly in combination with external (de-)interleavers show a route to scale sampling rates up till at least 250 GSamples/s or higher. Finally, a selection of technologies to integrate photonics and electronics with dense and low-parasitic interconnect have been presented, which will be essential to maintain the necessary high bandwidth from PIC to EIC.

While undoubtedly still challenging, the technologies are in place to further scale the baudrates of optical transceiver up till ~250 Gbaud or even higher.

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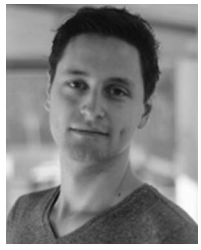

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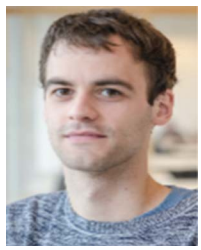

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