Enhancing modulation efficiency and reducing transmission penalty in double-layer graphene modulators through waveguide design optimization

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Abstract:

This paper presents simulation results demonstrating how mode-shifting through a silicon slab on top of a slot waveguide design can improve the modulation efficiency and transmission penalty of a double-layer graphene modulator integrated on a 220 nm thick silicon-on-insulator platform. By changing the waveguide geometry the optical overlap of the mode with graphene can be tuned. An example of this is shown in this paper using TE slot waveguides which have an enhanced modulation efficiency. The transmission penalty, a figure of merit relating insertion loss and extinction ratio, did not improve for these devices, which is caused by a significant evanescent tail of the mode of a slot waveguide.

To further optimize the performance of the TE slot waveguide the silicon slab was introduced on top of the graphene slot modulator. This addition of this Si slab resulted in an optimized modulator mode-profile, which yields an improvement in both modulation efficiency and transmission penalty compared to the TE slot waveguide. Additionally, the optimization mentioned continues from previously experimentally demonstrated graphene slot modulator manufactured on the commercially available 220 nm imec platform. Thus showing a feasible way to enhance the performance of existing double-layer graphene modulators.

Introduction:

Graphene-based electro-optical modulators have received significant attention in recent years due to their potential applications in high-capacity optical communication and computation systems. These modulators possess several desirable features such as a large extinction ratio (ER), low insertion loss (IL) and compact footprint. They can also be modulated using low (CMOS compatible) driving voltages [1]. Conventional strip TE waveguides are limited in their modulation efficiency, caused by a low intensity of the evanescent E-fields within the graphene sheets placed on top. Recent research has shown that the E-field intensity within the graphene layer can be improved by switching to slot waveguides, resulting in a higher modulation efficiency, which allows for a reduction of the footprint of the graphene modulator. The transmission penalty (TP) of the device, a figure of merit relating both ER and IL [2], showed minimal improvement however [1]. This is caused by an increase in IL of the slot devices, which negates the benefits of the improved modulation efficiency.

Improving this TP, combined with an improved modulation efficiency remains an important research area to further advance the performance of graphene-based electro-optical modulators. In this paper, we demonstrate in simulations how the mode-profile of a double-layer graphene modulator can be optimized resulting in both an improvement in transmission penalty and modulation efficiency.

Simulation setup and optimization method:

The simulations and optimization presented in this paper build upon prior experimental work of double-layer graphene modulators, where silicon strip and slot waveguides were manufactured on imec's planarized 220 nm SOI platform [1]. This platform consists of a 220 nm Si layer on top of a 2 μm BOX patterned using DUV tools on 200 mm wafers. Graphene integration was performed using CVD grown graphene having an estimated scattering rate of 30 meV for enabling future scalability. A schematic cross-section of the strip DLG modulator considered is shown in figure 1.

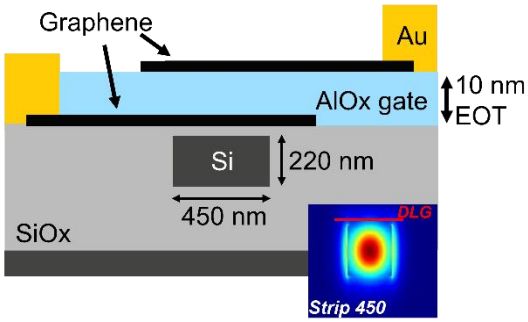

Figure 1 Double-layer graphene modulator on a strip waveguide

The modulator performance and optimization was simulated by first calculating the optical mode of the waveguide cross-section using the Lumerical MODE software [3]. The optical loss induced by the graphene layers was calculated using

$$\alpha(E_f) = \frac{1}{P_z}\int |E_{//}(x, y_{graph})|^2 Re\{\sigma_s(\omega, \Gamma, \mu, T)\}dx$$

where P_z is the Poynting vector along the propagation direction, $E_{//}(x, y_{graph})$ the tangential electric field of the optical mode at height y of the graphene layer, and $\sigma_s(\omega, \Gamma, \mu, T)$ the surface conductivity of graphene calculated using the Kubo equations with ω being the angular frequency, Γ the graphene scattering rate, T the temperature and μ the graphene Fermi level [4].

The Fermi level in graphene modulators is tuned through electro-static gating. The relation between the DC voltage applied between the graphene layers and the graphene Fermi level is calculated through

$$\mu(V) = \hbar v_f \sqrt{V \frac{C_{eq}\pi}{e}}$$

with e being the coulomb constant, C_{eq} the equivalent capacitance of the device and v_f the Fermi velocity of graphene at $9.5 \cdot 10^5$ m/s [5]. It should be noted that graphene only experiences modulation where the graphene sheets overlap, and in simulations the Fermi level in non-overlap regions are kept fixed at a chemical potential of 0 eV.

An example of a simulation where the voltage is swept is shown in figure 2. The figure shows the loss of the modulator per µm length in case of a 500 nm graphene overlap and a 10 nm AlOx thickness. The figure shows that the graphene devices do not reach the transparency regime in simulations for the given max voltage and oxide thickness used. In simulations an improved TP can be achieved by moving to higher voltages, or thinner oxide thicknesses. However since this is not feasible for experimental work this was not considered in the simulations.

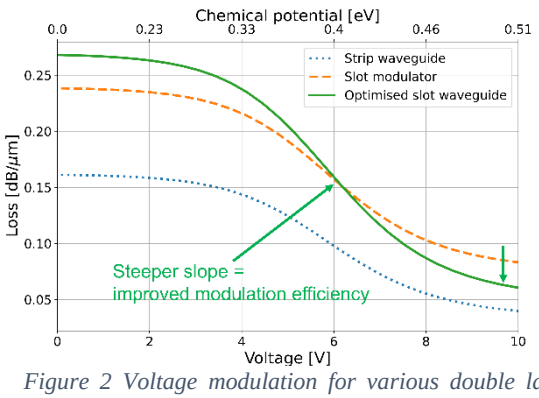

Figure 2 Voltage modulation for various double layer graphene modulators in case of a 10 nm EOT

The graphene modulator was optimized through a particle swarm optimization algorithm with two generations followed by a Nelder-Mead optimization on the

optimal point, where the width, height and graphene encapsulation thickness of a silicon slab on top of the graphene slot modulator is optimized. The optimizer was programmed to optimize the transmission penalty only, but can be modified to enable optimization of the modulation efficiency.

Simulation results and discussion

In this section simulation results for a graphene modulator having a 2 V_{pp} driving voltage and an AlOx thickness of 10 nm are presented. These parameters were chosen to stay in line with previous experimental results [1].
Simulations consider a TE strip waveguide, TE slot waveguide and the optimized TE slot waveguide which are schematically shown in Figure 3a), d) and g). The optical modes corresponding to these architectures are shown in Figure 3b), e) and h), with Figure 3c), f) and i) showing the normalized cross-section of the tangential E-field profile at the graphene layers.

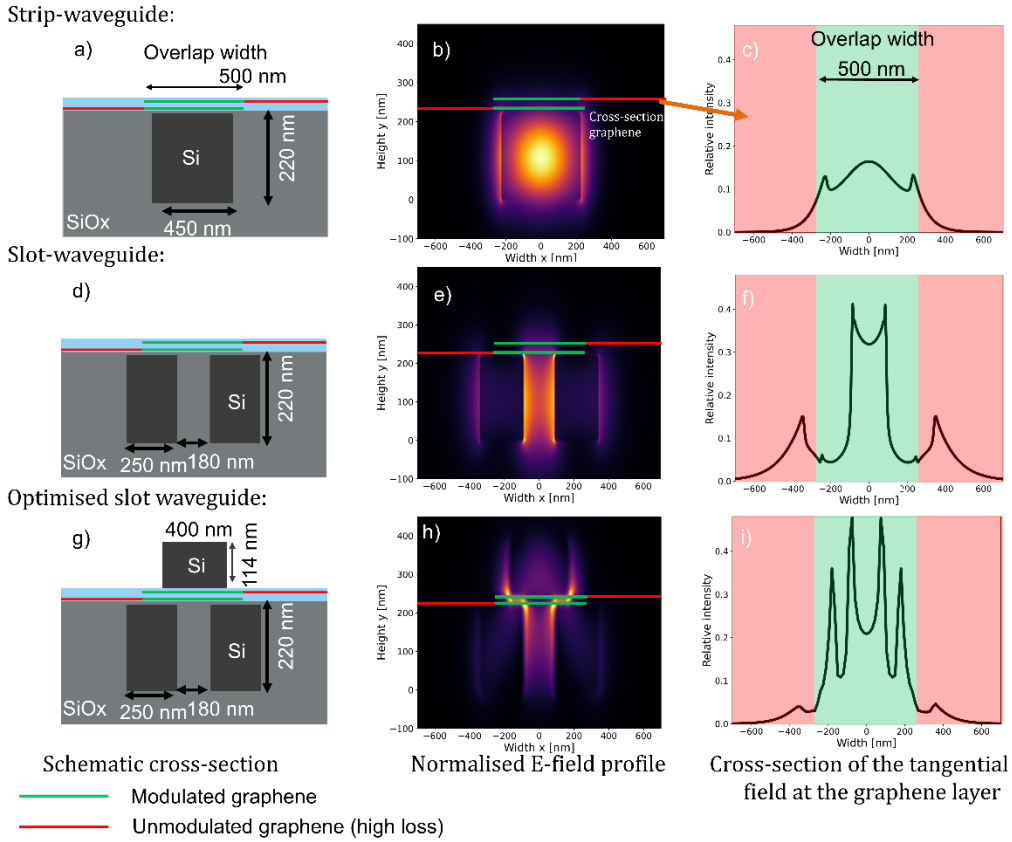

Figure 3 subfigures a), d), g) showing the schematic cross-section of the strip, slot and optimized slot waveguides. Subfigures b), e) and h) showing the mode profiles of the strip, slot and optimized slot waveguide. Subfigures c), f) and i) showing the tangential E-field profile 5 nm above the Si waveguide, with all three mode profiles being normalized to each other through the Poynting vector of the field profiles..

The overlap width of the two graphene layers is varied in simulations for which the results of the modulation efficiency and minimal transmission penalty, in case of a 20 µm long modulator, are shown in Figure 4.
The first conclusion that can be made from Figure 4 is that both the transmission penalty and modulation efficiency improve with an increase in overlap width. However by increasing this overlap the capacitance of the device increases. This has a negative

effect on the E/O bandwidth, thus when designing graphene modulators there will always be a trade-off between TP and the E/O bandwidth.
Comparing the slot to the strip modulator, the modulation efficiency improves for all overlap widths. This can be attributed to the increased E-field intensity at the graphene layer in the slot waveguide, as can be seen in Figures 3c) and f). The transmission penalty of the slot modulator improves for overlap widths below 500 nm since the peak E-field intensity width is concentrated at the center of the waveguide. Beyond 500 nm the slot modulator experiences higher insertion losses caused by the E-field 'horns' in the slot waveguide field profile.

The optimized slot modulator shows an enhanced modulation efficiency compared to both the slot and strip modulators. This improvement stems from the higher E-field intensity at the graphene layer as shown in Figure 4i). Additionally, the optimized modulator has a consistent improved transmission penalty for all overlap widths. This is a results of the enhanced modulation efficiency combined with the reduced insertion loss compared to the slot waveguide. This is achieved by suppressing the 'horns' present in the slot modulator's field profile which in turn reduces the insertion loss induced by the non-modulated part of the graphene modulator.

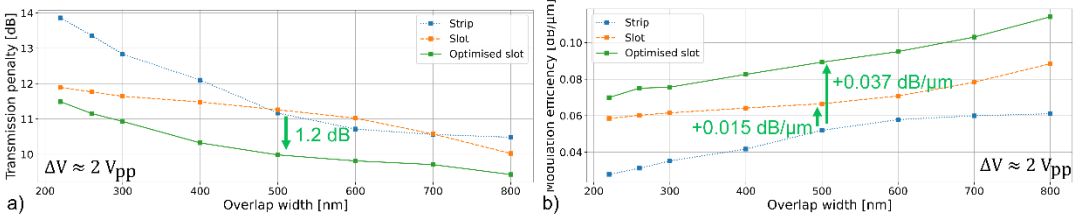

Figure 4 Simulation results with Figure a) showing the transmission penalty for a 20 µm modulator and Figure b) showing the modulation efficiency for the strip slot and optimised slot waveguide geometries

This optimization of the slot waveguide can be included in the double-layer graphene process flow by growing or transfer printing a silicon layer or slab on top of the double-layer graphene modulator. After this the silicon slab can be patterned and etched, where the existing encapsulation layer of graphene can be used as an etch-stop layer.

Conclusion

We have demonstrated in simulations that both the transmission penalty and modulation efficiency of a double-layer graphene modulator can be improved through optimization of the waveguide design. The best results are found for the optimized slot modulator, where for the case of a 500 nm graphene overlap the TP improved by 1.2 dB and the modulation efficiency increased by 0.037 dB/µm.

References

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