

# Generic Heterogeneous Integration Process Flow for Commercial Foundry Low-Index Photonic Platforms

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**Abstract:** We demonstrate a generic heterogeneous integration process flow for low-index photonic platforms, based on a two-step microtransfer printing approach. In this work, a silicon coupler is used for low-loss integration of III/V on silicon nitride. © 2021 The Author(s)

## 1. Introduction

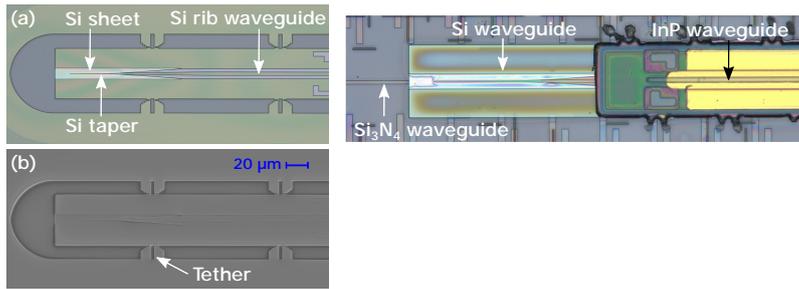
Silicon-nitride-on-insulator has been widely recognized as a promising passive photonic platform for telecommunication and life-science applications owing to the wide transparency window, limited mode confinement and ultra-low losses. However, due to the low refractive index of silicon nitride ( $\text{Si}_3\text{N}_4$ ), it is not straightforward to efficiently couple light between a III/V gain section and the passive  $\text{Si}_3\text{N}_4$  waveguide using evanescent coupling. In recent years, the heterogeneous integration of III/V semiconductor optical amplifiers (SOAs) on  $\text{Si}_3\text{N}_4$  therefore depended critically either on wafer bonding an intermittent Si layer [1] or the deposition of a hydrogenated amorphous silicon layer (a-Si:H) [2]. This intermediate layer allows for a better match in refractive index and consequently a higher coupling efficiency. Although these approaches have proven successful to develop integrated laser sources, the latter is likely to suffer from the material degradation of a-Si:H for high power pulses [3]. Moreover, both approaches depend on a considerable number of fabrication steps, increasing the overall processing time, proving fast prototyping elusive. Furthermore, the heterogeneous integration in a recess poses a significant challenge for existing integration methods, while being an essential technical requirement for compatibility with low-index photonic platforms with a thick oxide cladding.

## 2. Design and fabrication

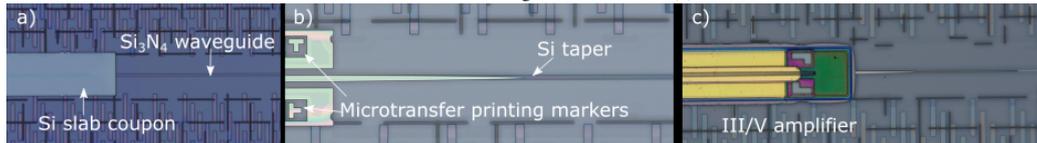
Here, we demonstrate a convenient heterogeneous integration process based on a two-step microtransfer printing approach and prove its viability on a commercially available silicon nitride platform, here fabricated by Ligentec SA. Two variations to this approach are demonstrated, each with specific benefits. In both cases a Si coupling structure is created on top of the  $\text{Si}_3\text{N}_4$  waveguide, to bridge the large refractive index mismatch between the  $\text{Si}_3\text{N}_4$  and the III/V SOA and enable efficient coupling.

In a first approach, a fully preprocessed Si coupling structure is microtransfer printed, enabling fast prototyping at the expense of limited alignment accuracy of the Si taper ( $\sim 500$  nm). A rib waveguide is employed to enable mechanical attachment of the waveguide core to the support structure of the coupon. This approach restricts most of the processing steps to the native source sample, which is a major benefit in terms of yield and fabrication time. The second approach starts from slab Si coupons, which are microtransfer printed onto the target sample. The waveguide and taper structures are then defined after the microtransfer printing step, using electron-beam lithography and RIE etching. Alignment is in this case done in the electron-beam lithography tool, using markers on the target sample, allowing for a high alignment accuracy (100 nm) and relaxed constraints on the coupler design. A 35 nm alumina etch stop layer on top of the  $\text{Si}_3\text{N}_4$  chip was used to pattern the Si coupler. This thin layer has no significant impact on the coupler performance. Moreover, if necessary the alumina can selectively be removed after microtransfer printing using an off-the-shelf photoresist developer.

For both approaches, the III/V SOA is subsequently printed on top of the Si coupler, hence limiting the heterogeneous integration process to merely two transfer printing cycles with minimal additional patterning or etching steps.



**Fig. 1** Approach 1: Microscope picture of a suspended preprocessed Si coupon on the source silicon-on-insulator wafer (a) and an optical shadow effect mode picture of the same structure (b). Microtransfer printed SOA on top of a printed Si coupon in the recess of a Ligentec  $\text{Si}_3\text{N}_4$  die (c).



**Fig. 2** Approach 2: Microscope picture of a microtransfer printed slab Si coupon (a) and the Si taper structure defined in this coupon with electron beam lithography (b). Microtransfer printed SOA on top of this patterned Si coupon (c).

Both the preprocessed coupons and slab coupons are fabricated on a 400 nm thick SOI wafer using electron-beam lithography (approach 1) or photolithography (approach 2) and dry etching. The Si taper design was optimized using coupled mode theory [4] to ensure robustness against lateral displacements (induced during microtransfer printing) as well as to ordinary fabrication tolerances. Moreover, for the first approach, a 20 nm thin Si sheet is left in the vicinity of the Si taper to warrant mechanical stability of the 150 nm wide taper tip during the microtransfer printing procedure (Fig. 1 (a)). As a final step, the sacrificial  $\text{SiO}_2$  layer underneath the Si coupons is underetched using hydrofluoric acid (HF) vapor (Fig. 1 (a), (b)). In contrast to liquid HF, vapor-phase HF provides a near 100% picking yield as it does not suffer from capillary forces which can lead to a collapse of the suspended Si layer. To ensure a high printing yield, a 80 nm adhesive BCB layer is spincoated on the target Ligentec die prior to microtransfer printing. Si coupons with a 1.6 mm and 2 mm length have been successfully printed on a 2  $\mu\text{m}$  wide and 800 nm thick  $\text{Si}_3\text{N}_4$  waveguide to accommodate a 1.3 mm InP SOA (Fig. 1 (c), Fig. 2 (c)). For approach 2, Si slab coupons are transferred onto the target die using microtransfer printing (Fig. 2 (a)). The tapers and waveguide structure are then created using electron-beam lithography and dry etching. In this case a fully-etched waveguide structure was used (Fig. 2 (b)), simplifying the processing to a single lithography and etching step. Using this approach, alignment offsets of  $\sim 100$  nm have been achieved. The two approaches we demonstrate have been successfully fabricated on the commercial low loss  $\text{Si}_3\text{N}_4$  platform of Ligentec SA. Measurements indicate a loss  $< 1$  dB per transition for a 1.6 mm Si coupon despite a 600 nm lateral offset using approach 1, and similar losses for a 2 mm Si coupon with a 100 nm lateral offset using approach 2. This is a strong indication that the taper design is very tolerant to lateral offsets. Further reduction of the coupling loss is likely limited by the sidewall roughness of the long and narrow tapers required for efficient mode coupling on this platform. This approach could also easily be extended to different platforms, with minor changes to the taper design and processing flow.

### 3. Conclusion

We have demonstrated two approaches for heterogeneous integration using two microtransfer printing steps. The presented approaches enable rapid prototyping and allow for low-loss III/V integration on generic commercially available low-index passive photonic platforms. In this work we show that this method strongly limits the required post-processing on target samples while enabling heterogeneous integration in a recess and competitive performance compared to existing integration methods.

### References

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