

Silicon-on-insulator nanophotonics

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ABSTRACT

Nanophotonics promise a dramatic scale reduction compared to contemporary photonic components. This allows the integration of many functions onto a chip. Silicon-on-insulator (SOI) is an ideal material for nanophotonics. It consists of a thin layer of silicon on top of an oxide buffer. In combination with high-resolution lithography, one can define a high refractive index contrast both in horizontally and vertically, resulting in a tight confinement of light. Moreover, SOI can be processed with industrial tools now used for silicon microelectronics. There are two candidates for nanophotonic waveguides. Photonic wires are basically conventional waveguides with reduced dimensions and a high refractive index contrast. These waveguides with submicron dimensions can have bend radii of only a few micrometers. The alternative is to use photonic crystals, which confine light by the photonic band gap effect. Introducing defects in a photonic crystal creates waveguides and other functional components. To make nanophotonics commercially viably, mass-manufacturing technology is needed. While e-beam lithography delivers the required accuracy for nanophotonic structures, it is too slow. We have used deep-UV lithography, used for advanced CMOS fabrication, to make nanophotonic waveguides. The fabrication quality is very good, which translates to low propagation losses. E.g. a $500nm$ (single-mode) photonic wire has a propagation loss of only $0.24dB/mm$. Using these low-loss waveguides, we have implemented a variety of nanophotonic components, including ring resonators and arrayed waveguide gratings.

Keywords: Nanophotonics, Silicon-on-Insulator, Photonic Crystals, Arrayed Waveguide Grating, Resonator

1. INTRODUCTION

To realize in photonics a similar increase in functionality as has been seen in electronics in the past decades, many photonic functions should be integrated onto a single chip. Large-scale integrated photonics have a number of distinct advantages: a serious reduction of costs through high-yield wafer-scale processes, increased performance, compact components with complex functionality, etc. Also, because of lithographic techniques, photonic integrated circuits (PICs) have the added benefit of automatically adhering to the strict alignment requirements of subcomponents. This dramatically reduces the need for costly active alignment procedures which are known to dominate the overall cost in discrete optoelectronics. However, in current commercial photonic components, many components have a length scale of several $100\mu m$ up to several millimeters, sometimes even centimeters. This not only holds for active functions, but also for simple passive elements such as filters, (de)multiplexers or even the bend radius of simple interconnecting waveguide.

Often, these large dimensions are needed because of the low refractive index contrast of the waveguides. Increasing the index contrast improves the confinement, but in parallel, the waveguide core should be shrunk to keep the waveguide single-mode. This results in waveguides which are not only very small but have to be fabricated with an accuracy in the range of 1 to $10nm$. Therefore these waveguides are often called *nanophotonic waveguides*. There are basically two types of nanophotonic waveguides: *Photonic wires*, which confine light with total internal reflection, and *Photonic Crystal* waveguides, which use the *Photonic Band Gap* (PBG) effect.^{1,2}

An unwanted side-effect of the higher index contrast is that the waveguides become more sensitive to perturbations, like scattering at roughness on the core-cladding interface.³ Or, in interferometric structures, the

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waveguides will be sensitive to phase noise due to small changes in waveguide shape and size along the propagation length. Therefore, high-quality, high-resolution fabrication tools are required. For research purposes, nanophotonic components are often fabricated using e-beam lithography. This is a very precise technique, but it is slow and not suitable for mass-production. Deep UV lithography, which is used for advanced CMOS fabrication, has both high resolution and large throughput. However, the technology development for this platform is largely dictated by the silicon electronics industry, which has very different requirements than those of photonic components. Direct transfer of processes is therefore not always straightforward.

Another problem of miniaturization is interfacing to the outside world. This is not different for nanophotonics, where the waveguide mode of a standard telecom fiber is orders of magnitude larger than the mode of a nanophotonic waveguide. Adiabatic tapers have been demonstrated,⁴ but they consume a large chip area. We have demonstrated a compact interface from a fiber to a photonic wire,⁵ using both a grating couplers, which can be combined with short multimode interferometric tapers.^{6,7}

In this paper we give an overview of our work in silicon-on-insulator (SOI) nanophotonic waveguide structures. First, we describe some basic properties of nanophotonic waveguides. The choice for the SOI material system becomes obvious then. In section 3 we describe the fabrication process, which is largely based on standard CMOS fabrication processes. Then we briefly describe basic waveguides, both photonic wires and photonic crystals in section 4. Section 5 covers wavelength selective functions implemented using photonic wire waveguides. These include resonators, cascaded Mach-Zehnder filters and Arrayed Waveguide Gratings (AWG). In section 6 we show a number of techniques to couple light to and from an optical fiber.

2. SOI NANOPHOTONIC INTEGRATED CIRCUITS

To keep the size of a nanophotonic circuit down, the various building blocks should all be as small as possible. As optical waveguides are a part of most functional elements, as well as the interconnection between the functional elements, they are an extremely crucial component. From a chip-layout point-of-view, the most important aspects of a waveguide are its core dimension, the minimum allowable spacing between waveguides and its bend radius. From an optical point-of-view, a waveguide should only have a single guided mode (at least for interconnection waveguides). Therefore, we could say that the ideal nanophotonic waveguide has a submicron core with a single mode that is mostly confined inside the core (to allow for small spacing and sharp bends). The confinement of a conventional waveguide is largely determined by the refractive index contrast between the waveguide core and the surrounding cladding. Semiconductors, which have a refractive index of 3 or larger, are very well suited for the fabrication of such waveguides. To get a single-mode waveguide with a high refractive index contrast, the waveguide's cross section must be of the order of $(\lambda/n_{core})^2$, with λ the wavelength of the light in vacuum, and n_{core} the refractive index of the waveguide core. For example, with a silicon core ($n = 3.45$) in air ($n = 1.0$) or glass ($n = 1.45$), waveguides are narrower than $500nm$ when operating at telecom wavelengths between $1.3\mu m$ and $1.6\mu m$. In functional building blocks, where interaction between multiple waveguides is needed, feature sizes can get down to $100nm$ or even less.

The tight confinement in such *photonic wires* allows for compact elements, like sharp bends, corner mirrors⁸ and ring resonators.⁹ However, as the performance is limited by sidewall roughness, these waveguides require very good processing.

For photonic crystal slab waveguides, there are similar constraints: the refractive index contrast should be sufficiently high (in order to have a full photonic band gap), and the feature sizes are of the order of the wavelength (inside the material). Photonic crystals are also sensitive to sidewall roughness, as well as to disorder in the periodic lattice.

2.1. Material Choice: Silicon-on-Insulator

A variety of materials is suited for photonic crystal slabs, but semiconductors are ideally suited. In this work, *silicon-on-insulator* (SOI) was used. SOI consists of a thin silicon layer on top of an oxide cladding layer carried on a bare silicon wafer. With its silicon core $n = 3.45$ and its oxide cladding ($n = 1.45$) it has a high vertical refractive index contrast (see figure 1. Also, both the silicon and the oxide are transparent at the telecom wavelengths of $1.3\mu m$ and $1.55\mu m$. its compatibility with CMOS fabrication processes, discussed in section 3.

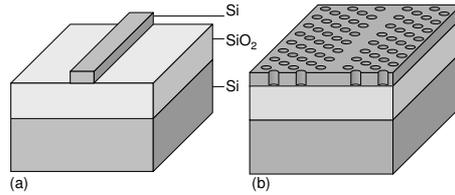


Figure 1. Nanophotonic waveguides in SOI. (a) Photonic wire, (b)W1 photonic crystal waveguide.

To reduce leakage of the guided mode in the top layer to the silicon substrate, we chose an oxide thickness of $1\mu\text{m}$.¹⁰ The thickness of the core was chosen to be 220nm , in order to keep the slab waveguide single-mode for the TE polarization.

2.2. Photonic Crystals

Photonic crystals are periodic structures with periods of the order of the wavelength of the light and a very high refractive index contrast within each period.^{2,11} For telecommunications, where infrared light with wavelengths in the range $1.3\mu\text{m} - 1.6\mu\text{m}$ are used, the photonic crystal period a is typically $0.45\mu\text{m}$ or less. The periodicity can extend in 1, 2 or 3 dimensions. Because of this high refractive index contrast, light will be scattered very strongly throughout the structure. For a well-chosen unit-cell geometry this scattering interferes in such a way that no propagation of light is possible within the crystal.¹ The wavelength range for which this occurs is the *photonic bandgap* (PBG).

When the regular lattice of a photonic crystal is disturbed, localized states are introduced in within the PBG. This binds light around the defect in the crystal. In a line defect, light must propagate along the defect, effectively creating a waveguide. The light cannot leak away through the surrounding photonic crystal because of the PBG. Therefore, when properly designed, bends in photonic crystal waveguides can be very abrupt.

3-D photonic crystals can control light omnidirectionally, but they are very difficult to fabricate for optical wavelengths, especially when well-controlled defects are needed. Alternatively one can use a *photonic crystal slab*. Here, a 2-D photonic crystal is created by etching a periodic lattice in a semiconductor slab waveguide, like the SOI layer structure. Horizontally, the photonic crystal controls the flow of light, while in the vertical direction the light is confined in the slab waveguide's core layer. This way, some 3-D control of the light can be achieved with structures that are much easier to fabricate using lithography and etching techniques. Figure 1b shows a W1 photonic crystal slab waveguide, consisting of a missing row of holes in a triangular lattice of etched holes in an SOI slab. However, unlike 3-D photonic crystals, the confinement in the vertical direction is not necessarily perfect, which can result in out-of-plane scattering losses of light.^{12,13}

Apart from pure waveguiding, photonic crystal slabs can also be used for other purposes. One significant aspect of periodic structures is the appearance of wavelength regions with a very flat dispersion curve, and therefore a low group velocity, especially near the band edges.¹⁴ In these regions, light is coupled strongly between the backward and forward propagating direction, and travels slowly through the waveguide. If the waveguide has active properties, like gain or nonlinear effects, the interaction time of the light with the material is significantly enhanced when using slow waves.

2.3. Photonic Wires

The principle of photonic wires is the same as of conventional optical waveguides: light is confined in a narrow core of high index material surrounded by a cladding of lower index material. For photonic wires, the index contrast is very high. This gives rise to very strong confinement, which makes it possible to make very sharp bends without radiation losses in the bend. However, there is no photonic bandgap to stop light from radiating away once it escapes the confinement of the wire.

Photonic wires are not periodic, and therefore their dispersion relation is far less exotic than photonic crystals. This makes them more predictable and easy to design. Moreover, they are broadband with a fairly linear dispersion, making them very well suited for waveguiding.

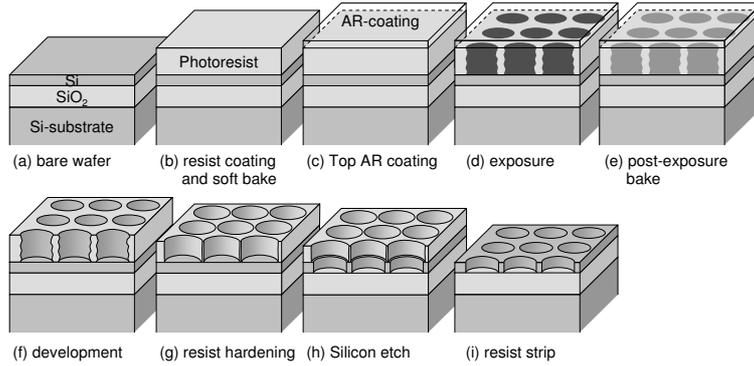


Figure 2. Fabrication process for photonic nanostructures in SOI using deep UV lithography and dry etching.

Still, because of their high refractive index contrast and their wavelength-scale features, photonic wires do have significantly more dispersion than conventional, low-contrast waveguides. The group index ($n_g = n_{eff} - \lambda dn_{eff}/d\lambda$), which dictates the propagation speed of a coherent pulse, is the relevant quantity when designing phase delays in interferometric structures. While the effective index of photonic wires varies between $n_{eff} = 2$ and $n_{eff} = 2.5$ for wires with a width between 400 and $600nm$, the group index has a value between $n_g = 4$ and $n_g = 4.7$. A waveguide height of $220nm$ is assumed. Therefore, when implementing wavelength-selective functions, there is still a significant size reduction possible with photonic wires compared to conventional waveguides. On the other hand, an optical on-chip link using photonic wires could have a considerable time delay compared to conventional (low-index) waveguides.

3. FABRICATION

For this work we used the advanced CMOS research environment of IMEC, Belgium. The fabrication process is illustrated in figure 2. First, photoresist with a top antireflective coating is spun on the bare wafer. After a pre-bake step, the patterns are illuminated into the photoresist. The resist is baked again, and then developed. Before etching, a resist hardening plasma treatment is applied to the resist. Then, the pattern is transferred into the silicon using an ICP-RIE etch. This fabrication process is described in more detail in.¹⁵

The substrate material was commercial SOI wafers from SOITEC fabricated with the UNIBOND[®] process¹⁶ with a silicon thickness of $220nm$ and an oxide layer of $1\mu m$.

3.1. Deep UV Lithography

Photonic nanostructures typically consist of a variety of structures and for accurate alignment all nanostructures should be printed in the same lithography step. Not all structures print on target for the same illumination setup and exposure dose.^{10, 17} E.g. for higher doses, illuminated areas, like the holes of a photonic crystal or the trenches next to photonic wires, will grow. The dose-to-target for photonic crystals and photonic wires can therefore differ significantly. To fabricate both together, a bias needs to be applied to some structures. Isolated features, such as photonic wires, are easier to correct than dense features. In photonic crystals, which are densely packed structures with periods close to the illumination wavelength, the proximity of the holes causes interference between the images neighboring holes. This can cause aberrations in the features near to defects in the photonic crystals. These *optical proximity effects* (OPE) should also be corrected on the mask in advance. The optical proximity corrections that are needed to print these holes on target have been described elsewhere.¹⁵

3.2. Etching

After lithography, the photoresist patterns are etched into the underlying SOI. We can choose between etching only the top silicon, or the underlying oxide as well. For a nanophotonic waveguide, etching the oxide is better, as it increases the lateral and the vertical index contrast. However, this resulted in significant sidewall roughness,

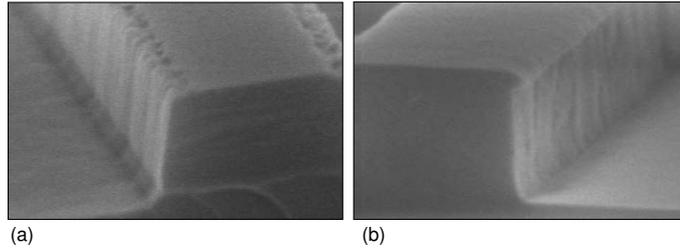


Figure 3. Scanning Electron Micrograph of photonic wire waveguides. (a) etched with the standard etch process for Silicon, using the photoresist as an etch mask, and (b) using a 40nm thin SiO_2 hard mask.

leading to high waveguide losses.¹⁰ Although the sidewall roughness can be reduced by thermal oxidation of the top silicon layer¹⁸ this technique only reduces roughness in the top layer, not in the underlying oxide.

We therefore opted not to etch the buried oxide altogether. Instead, we applied a plasma treatment of the photoresist, which smoothens irregularities present in the photoresist patterns. Then the top Silicon is etched, using the resist as an etch mask. Very low propagation losses for photonic wires fabricated with this process have been demonstrated.^{6,19}

Still, after detailed SEM inspection, there is still significant sidewall roughness (Figure 3a). Also, from the same image we can see that there is also additional roughness at the top edges of the waveguides. This can be attributed to resist etch-through.

To improve both the sidewall roughness and avoid resist etch-through, a thin SiO_2 layer (40nm) was applied as a hard etch mask. This layer is applied prior to the photoresist using TEOS deposition. After lithography, the pattern is first transferred into the oxide, which is then used as a hard mask for etching. Afterward, the photoresist is stripped. At this stage, no attempts have been made to remove the oxide hard mask, which becomes an integral part of the waveguide. Any chemical process for the removal of this oxide top layer would also affect the exposed buried oxide which serves as the bottom cladding.

SEM inspection (Figure 3b) shows a considerable reduction in sidewall roughness. Note that the SiO_2 hard mask is clearly visible, giving the waveguide cross-section a T-top profile.

4. WAVEGUIDES

The waveguide is the most basic component of a photonic integrated circuit. As already mentioned, we can use either photonic crystal waveguides or photonic wires.

Experiments have shown that, for a given level of fabrication technology, photonic wires outperform photonic crystal waveguides in terms of propagation losses.^{6,20}

4.1. Straight Waveguides

Using our fabrication technology, we have demonstrated propagation losses as low as $2.4dB/cm$ in photonic wires.^{15,19} Similar results have been reported by other groups.^{21,22} This is in strong contrast with the propagation losses of our photonic crystal waveguides, which are of the order of $70dB/cm$.^{6,15} Lower propagation losses, of the order of $20dB/cm$ in SOI photonic crystal losses have been reported.^{22,23} However, all these results are on structures fabricated with e-beam lithography. To reduce propagation losses even further, the oxide buffer of the SOI stack can be removed, something which is only possible in photonic crystal waveguides, as it is obvious that a free-standing photonic wire is mechanically very difficult to make. Using so-called air-bridge photonic crystal waveguides, propagation losses of $6 - 7dB/cm$ have been reported.^{21,22}

As mentioned in section 2.2, photonic crystal waveguides can support modes with a very high group index. These slow light modes have been experimentally observed in SOI waveguides.²⁴ However, as the propagation losses of these modes increase with lower group velocity, these slow modes are therefore very lossy.

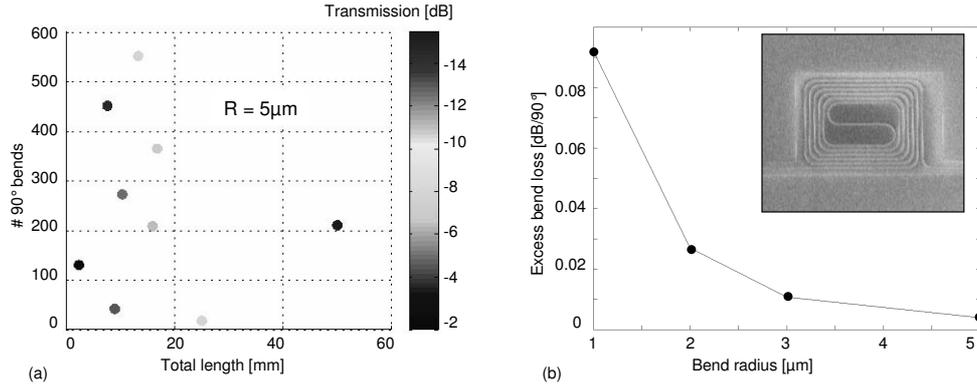


Figure 4. Bend losses in photonic wires. (a) Total transmission for a spiral waveguide with $5\mu\text{m}$ bend radius as a function of the number of 90° bends and the total waveguide length. (b) Excess bend loss (compared to a straight waveguide of equal length) per 90° bend, as a function of bend radius.

4.2. Bends in Photonic Wires

In photonic wires, bend losses increase when the bend radius decreases. To characterize these bend losses, we fabricated a large number of spiral waveguides with various bend radii (see inset in figure 4b). We cascaded such spirals to obtain a statistically significant spread in both waveguide length (from $100\mu\text{m}$ up to 5cm) and number of bends (from 0 up to 550 bends).

Figure 4a show the total transmission for different spiral waveguides with $5\mu\text{m}$ bend radius, plotted as a function of both the total waveguide length and the number of 90° bends. A bilinear fit on these data gives us both the propagation loss of the straight waveguide, as well as the excess loss per 90° bend. As expected, the bend losses increase dramatically for shorter bend radii. This is shown in figure 4b. For a bend radius of $1\mu\text{m}$, the excess bend loss is $0.92\text{dB}/90^\circ$, while for a $5\mu\text{m}$ bend radius, the losses drop an order of magnitude to $0.01\text{dB}/90^\circ$ bend. Similar number for bend losses have been reported in literature.²⁵

5. PHOTONIC WIRE-BASED WAVELENGTH SELECTIVE COMPONENTS

Wavelength Division Multiplexing (WDM) allows to transport a number of information channels over a single waveguide (or fiber) using various carrier wavelengths. Multiplexing and demultiplexing these signals requires wavelength selective filters. We demonstrate such components in SOI based on resonators, Mach-Zehnder interferometers and Arrayed Waveguide Gratings (AWG).

5.1. Ring and Racetrack Resonators

Micro-ring resonators can be a building block for densely integrated wavelength selective filters. The small bend radii with low radiation loss allows for very compact rings, which in turn allows for a very large *free spectral range* (FSR) needed for add-drop filters. Also important are a large finesse and high extinction ratio. Reliable fabrication of such devices is challenging however. Our ring resonators have radii from $1\mu\text{m}$ up to $8\mu\text{m}$ and are laterally coupled to two waveguides for in and outcoupling. We studied different coupling alternatives in order to achieve low crosstalk and high finesse while maintaining a large free spectral range.

5.1.1. Single Resonators

In figure 5a, we show a circular ring resonator coupled to two straight waveguides. The gap between the ring and the straight waveguide is limited to approximately 200nm due to lithographic limitations. This could be dramatically improved using shorter illumination wavelengths, and resolution enhancement techniques assist features and phase shift masks. As the length of the coupling section quite is short, the large gap makes coupling between the ring and waveguides difficult. Figure 6a shows the transmission spectrum of a ring with $5\mu\text{m}$ radius. At the resonant frequencies, the power in the drop port is still much lower than the power in the pass port.

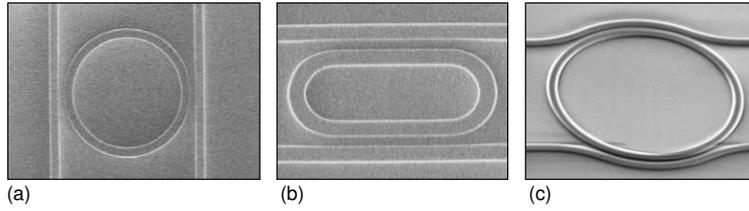


Figure 5. Ring and racetrack resonators. (a) Circular ring resonator; (b) racetrack resonator with a straight coupling section; (c) bend-coupled ring resonator.

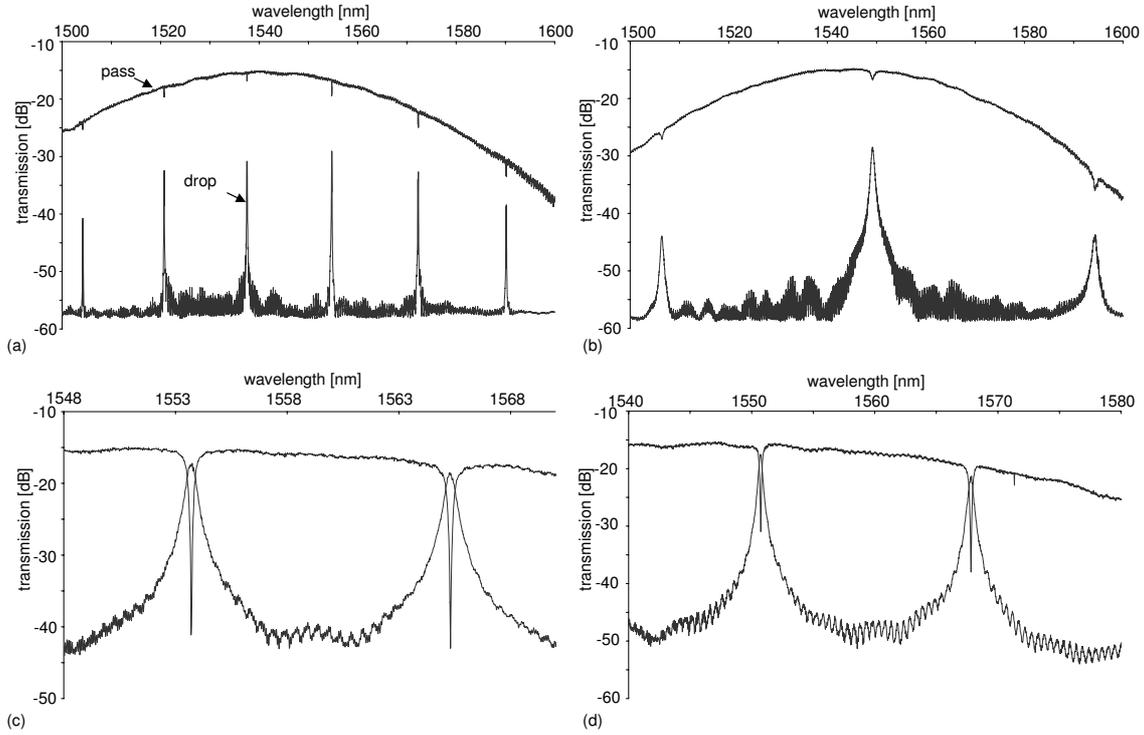


Figure 6. Transmission spectra of drop and pass ports for resonators. (a) Ring with $5\mu\text{m}$ radius; (b) Racetrack with $1\mu\text{m}$ bend radius, $3\mu\text{m}$ coupling section; (c) Racetrack with $5\mu\text{m}$ bend radius and $6.28\mu\text{m}$ coupling section; (d) Ring with bent coupling section and a radius of $5\mu\text{m}$

Therefore, we looked at other ring resonator configurations to enhance coupling between the cavity and the waveguides.

One option to improve the coupling efficiency is to include a straight coupling section, resulting in a racetrack-shaped resonator (Figure 5b). We have fabricated racetracks with radii of the bend section between 1 and $6\mu\text{m}$. Figure 6b shows transmission spectra of a racetrack with $1\mu\text{m}$ radius. With a $1\mu\text{m}$ radius (Figure 6a), a Q of around 2100 is obtained and a FSR in excess of 40nm , but the drop efficiency is low. The low Q can be attributed to bend losses in the photonic wire. For larger radii, the ring losses decrease quickly. With a $2\mu\text{m}$ radius, the drop efficiency is already much larger and Q factors in the range 5000 – 9000 are obtained. We have also fabricated racetracks with $5\mu\text{m}$ radius and larger coupling section. The larger coupling leads to a high add-drop extinction ratio of -20dB and 50-70% drop efficiency at Q factors still larger than 3000. This is illustrated in figure 6b. Due to the larger resonator, the FSR is reduced to approximately 12nm .

Racetrack resonators clearly improve coupling, but because of the required straight section the FSR is limited. Alternatively, one can use a bent waveguide for coupling.²⁶ An example is shown in figure 5c. By carefully choosing the widths of cavity and the access waveguides waveguides, a good phase matching can be obtained

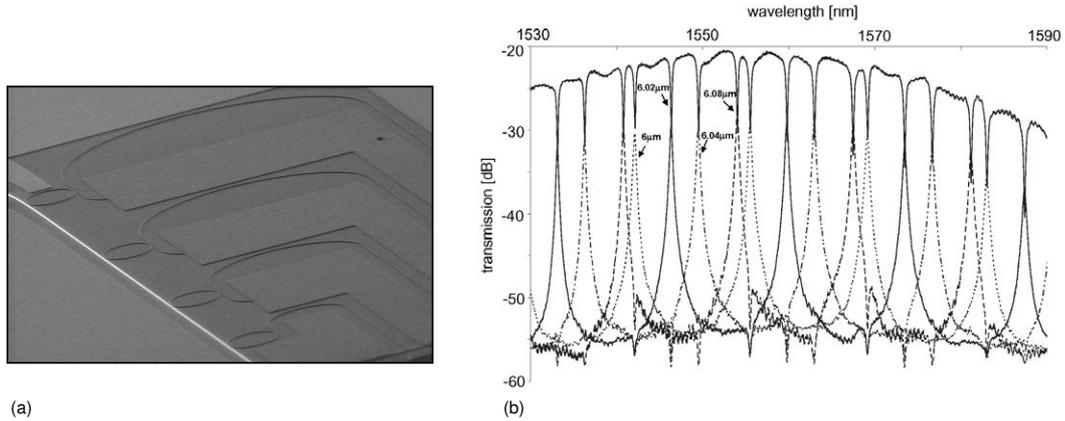


Figure 7. (a) 4-channel demultiplexer using first-order racetrack resonators with different bend radius. (b) overlaid transmission characteristics in the pass port and drop ports for the 4 output channels.

and coupling can be high without lowering the FSR as in the case of the racetrack resonator. We fabricated bend-coupled resonators with $5\mu\text{m}$ and $8\mu\text{m}$ radius. The amount of coupling is varied by varying the angular range over which both waveguides are aligned. As shown in figure 6, coupling is sufficient to obtain a quite high extinction ratio (-10dB to -15dB) and high drop efficiency. Further optimizations should improve these devices.

The dimensions of these ring resonators are critical. The gap of the directional coupler is typically $200-250\text{nm}$ wide and the coupling strength depends strongly on this value. The width of the waveguide in the ring has a strong influence on the resonance wavelength: a width change of 5nm leads to a shift of about 15nm . This sensitivity calls for a thorough optimization of the design and fabrication process including line bias effects and proximity corrections.

5.1.2. 4-Channel, Racetrack-Resonator-Based Demultiplexer

We have combined racetrack resonators to make a 4-channel add-drop filter by using racetrack resonators with different radius.²⁷ The device is shown in figure 7a. By varying the radius, the resonance wavelength is changed and each cavity is tuned to another set of dropped wavelengths. Note that with this approach the FSR also varies. Figure 7b shows the transmission spectra for the 4 resonators with bend radius 6 , 6.02 , 6.04 and $6.08\mu\text{m}$. We see that a large part of the FSR can be reached by changing the radius over only 80nm . However, the resonance wavelength doesn't increase linearly with the radius. We believe this is largely due the discretization on the mask, but other configurations will be studied to avoid this problem and achieve better control of the wavelength spacing.

5.2. Cascaded Mach Zehnder Filters (CMZ)

To implement filters, a Mach-Zehnder interferometer is an alternative to resonators. SOI-wire based Cascaded Mach-Zehnder interferometers have been demonstrated by several authors.^{28,29} As shown in figure 11, such filters consist of a series of Mach-Zehnder interferometers with constant path-length difference but with varying coupling ratio. The coupling ratios are optimized to obtain the desired wavelength dependent transmittance. A CMZ filter can be designed for Chebychev-type filter behavior with low sidelobe levels. Figure 8 shows an example of a 5-stage CMZ, consisting of 6 directional couplers and 5 delay sections. The isolated waveguides have a width of 565nm while the waveguides in the coupling sections are only 535nm wide due to optical proximity effects. The gap width itself is 220nm .

Figure 8c shows the transmission characteristic of this component in both the pass and the drop port, normalized to the transmission of a simple straight waveguide. We can see a well-defined filter characteristic with a bandwidth of 2.6nm , a free spectral range of 17nm and a coupling efficiency of almost 100%. The crosstalk of 10dB is still relatively high and caused by a non optimized choice of the coupling ratios and by phase errors in the interferometers.

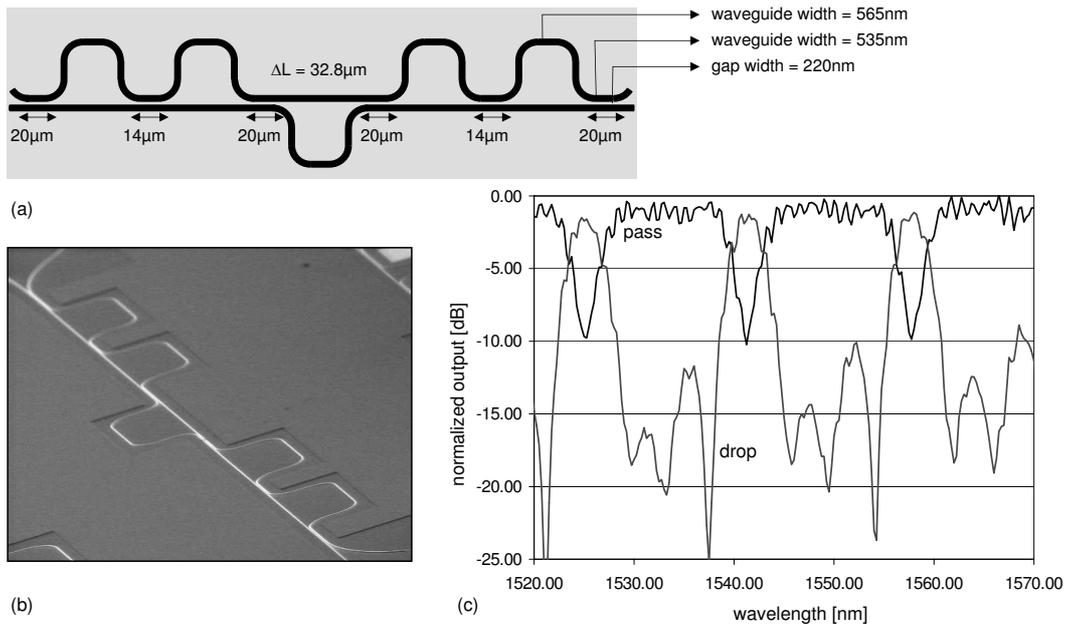


Figure 8. Design of a 5-stage cascaded mach zehnder filter. (a) Design parameters, (b) fabricated device, (c) transmission spectrum of pass and drop port

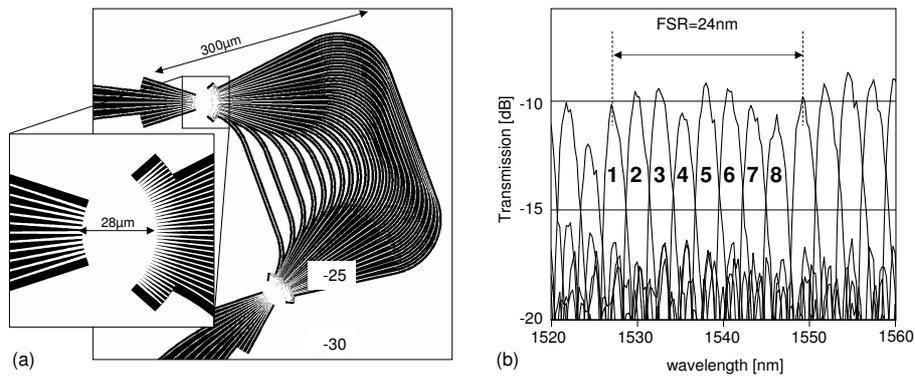


Figure 9. An arrayed waveguide grating. (a) Layout; (b) Overlaid transmission spectrum from the 8 output ports.

5.3. Arrayed Waveguide Gratings (AWG)

Silica-on-Silicon AWGs (*Arrayed Waveguide Grating*) are currently the most popular integrated device for multiplexing and demultiplexing multiple wavelength channels. However, these consume chip areas of tens of cm^2 . Figure 9a shows a an 8-channel AWG in SOI, which has a footprint of only $380\mu m \times 290\mu m$ or about $0.1mm^2$. The transfer from the input port to the 8 output waveguides is plotted in Figure 9b. The small ripple is caused by residual reflections in the grating couplers. The channel spacing is $3nm$, with a free spectral range of $24nm$. The on-chip insertion loss was approximately $8dB$. We believe this loss is mainly caused by reflections in the star coupler and can be reduced by adapting the transition zone between the grating arms and the star coupler. The main problem however is the high crosstalk level, limited to values around $-7dB$, which is clearly not sufficient for practical applications. Also in³⁰ an AWG fabricated using SOI-wires was presented. The authors optimized the devices for compactness and demonstrated a $110 \times 93m^2$ device with a $6nm$ channel spacing and a $90nm$ FSR. However, also in this case, the crosstalk was limited to a few dB.

The high crosstalk is caused by a combination of factors, the most important being overspill in the star coupler. Also, phase errors in the grating arms, introduced by very small irregularities in the high-index-contrast

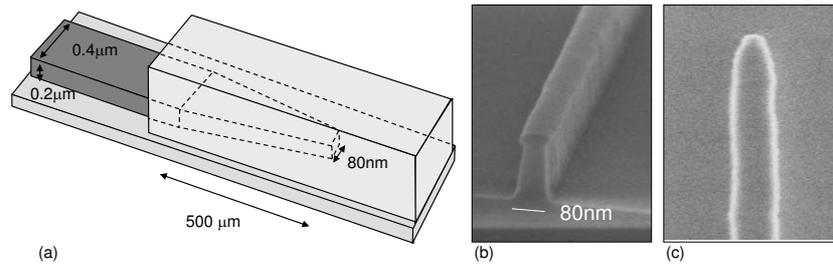


Figure 10. An inverse polymer taper for fiber-to-photonic-wire coupling (a) principle, (b, c) waveguide tip fabricated with deep UV lithography.

wires, can lead to random phase fluctuations over the array arms.

6. INTERFACING TO FIBER

Coupling light efficiently between an SOI nanophotonic waveguide and an optical fiber is an important issue. Some kind of spot-size converter is needed to adapt the mode of a sub-micrometer sized waveguide to the mode of a single-mode fiber.

In some material systems, such as polymer or silica-on-silicon, the size of the basic optical waveguide mode is identical to that of the optical fiber and the coupling is straightforward, with losses as low as $0.1dB$. In nanophotonics there is a large mode mismatch resulting in large coupling losses if no mode adapters are used. In general there are two approaches to enhance the coupling. One can either use external elements e.g. small ball lenses or a lensed fibers, or implementing the mode converter on the chip itself. Using external components doesn't require additional processing on the chip, but introduces costly packaging steps. On-chip mode converters relaxes the alignment requirements, which results in lower packaging cost. The extremely large mismatch makes external mode adaptation almost impossible for SOI nanophotonic circuits and on-chip mode adapters are needed.

There a number of requirements for a good mode converter. It should be broadband (which excludes long, weak diffraction gratings) and have a low insertion loss (including reflection). To reduce the packaging costs, the couplers should have sufficient alignment tolerances. It should also be easy to fabricate, with a limited number of (CMOS compatible) processing steps, and reasonable fabrication tolerances. Because these mode converters are included on the nanophotonic circuit, the footprint per connection should also be kept within bounds, as large mode converters can easily cancel out the reduction in size gained from the use of nanophotonic circuits.

Different solutions possible, two of which are described below.

6.1. Adiabatic (Inverse) Tapers

The inverse taper approach shown in figure 10a has been demonstrated by several groups. Over a length of a few hundreds of micrometers the photonic wire is narrowed down, expelling the optical field upwards into a lower-index top cladding. In most cases this overlay is patterned to form a low-contrast, single mode waveguide, which transports the optical mode to the edge of the chip, coupling into a small-core, high-NA single mode fiber. Low-loss, broad-band operation was demonstrated ($< 0.5dB$ per connection between $1250nm$ and $1750nm^4$,²¹). The loss is strongly dependent on the silicon taper tip width and the taper length. A compromise between acceptable loss and size has to be found. All of the demonstrated devices until now used e-beam lithography for defining the narrow taper tips. Figure 10b shows a similar taper point fabricated using a combination of $248nm$ DUV lithography and trimming, demonstrating that these couplers are also compatible with standard CMOS processing techniques.

6.2. Grating Fiber Couplers

An alternative to adiabatic tapers is the use of a diffraction grating to couple light to and from a fiber. This idea is not new, but often a long, weak grating is used, which results in a narrow bandwidth. Moreover, such a solution may require an additional lens because the Gaussian beam exiting the grating is not adapted to the

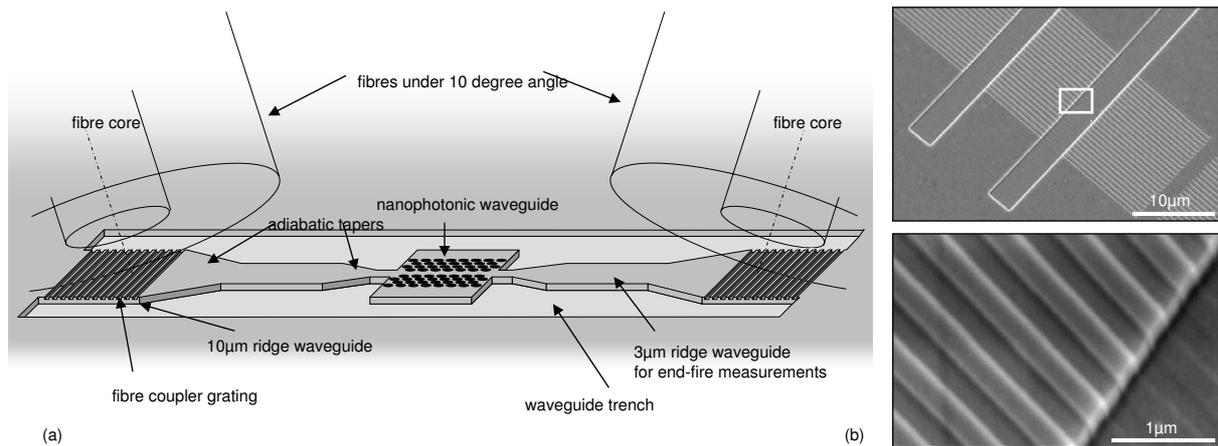


Figure 11. A vertical grating-based fiber coupler used for coupling light into nanophotonic waveguide structures and back into fibers. (a) principle, (b) fabricated structure.

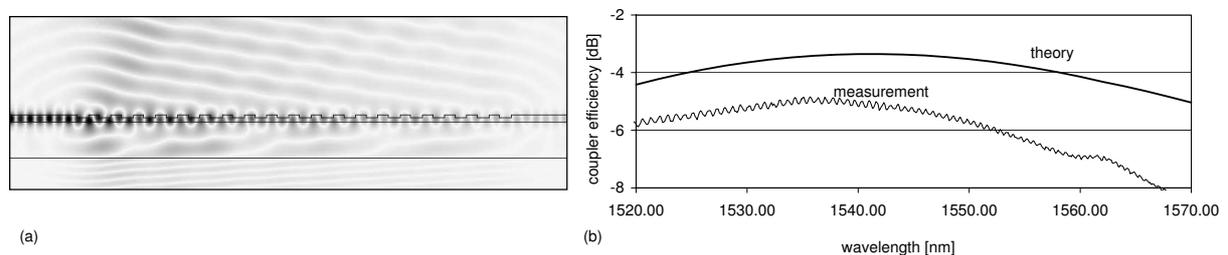


Figure 12. A vertical fiber coupler. (a) Simulation of the field distribution; (b) simulated coupling efficiency as a function of wavelength, and measured coupling efficiency.

fiber mode. Instead, we used a short but strong grating as shown schematically in Figure 11. The mode exiting this grating has the same dimensions as the single mode fiber and therefore direct butt-coupling between the fiber and the chip is possible.

There are a number of advantages to using such a grating coupler: This grating has only a footprint of $10\mu\text{m} \times 10\mu\text{m}$ ensures a large bandwidth, of the order of 50nm . If the fiber is slanted with respect to the top surface, there is only very little backreflection into the fiber. However, the main advantage is that such a coupler allows for in and outcoupling without the need for cleaving and polishing facets, which makes wafer-scale testing of photonic circuits possible.

We designed and optimized a grating for coupling between an SOI waveguide, with a 220nm thin *Si* core layer, and a single-mode optical fiber.⁵ For a uniform grating, the maximum coupling efficiency that can be achieved is approximately 55% and the 1dB bandwidth for that structure is 43nm . The parameters that were optimized are the etch depth, grating period and duty cycle and the thickness of the buried oxide layer of the SOI. Also an index matching layer is used between the grating and the fiber. The thickness of the buried oxide is very crucial, and our SOI wafers with $1\mu\text{m}$ oxide are not optimal, reducing the coupling efficiency. Figure 12 shows both the simulation and experimental results for a deep-UV fabricated fabricated grating coupler. As can be seen from this picture a maximum coupling efficiency of 32% was measured. The 1dB -bandwidth is 35nm . The theoretical calculations for the same structure are also shown. The maximum coupling efficiency was calculated to be 46%.

The gratings can be optimized further by modifying the fill factor of each grating period. Both the width of the grating teeth and the spacing between the grating teeth is optimized.³¹ On an SOI substrate the coupling efficiency is 63%.

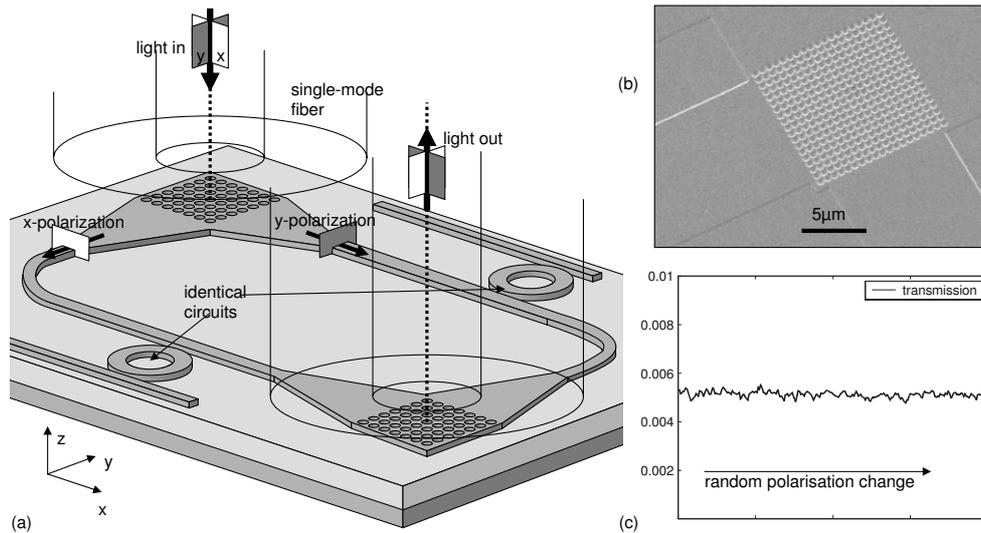


Figure 13. (a) Polarization diversity scheme using 2-D grating couplers. (b) Fabricated 2-D grating coupler. (c) Transmission (fiber to fiber) of a polarization diversity circuit when the polarization at the input is changed randomly.

6.3. Polarization Splitter

The 1-D grating only couples TE-polarized light into the circuits and TM-polarized light is lost. However, with a 2-D grating both polarizations can couple to different directions perpendicular with respect to each other. Such a 2-D grating coupler can be used as a polarization splitter³² for implementing a polarization diversity scheme as presented in Figure 13a. The two fiber polarizations are split up and each is processed in its own circuit. Of course, both circuits should be identical. At the end, both circuits are merged using another 2-D fiber coupler.

A fabricated fiber coupler is shown in figure 13b. As with the 1-D fiber coupler, the grating itself is roughly the same size as a single-mode fiber core. Figure 13c proves the validity of a polarization diversity scheme using the 2-D fiber couplers. The graph shows the transmission of a polarization diversity circuit while the polarization in the input fiber is rotated randomly. The output power of the circuit remains constant.

6.4. Interference-based Spot-Size Converters

While the actual coupling section of a grating coupler is only $10\mu m$ long, it is only coupled to a $10\mu m$ wide waveguide, not to a single-mode submicron photonic wire. For this transition, an adiabatic taper should be several hundred micrometers long. A non-adiabatic taper based on multi-mode interference can couple a broad and narrow waveguide over a much shorter length.³³ An example with a field plot is shown in figure 14a. The coupler consists of a non-periodic segmented waveguide, where each segment is actual a multi-mode waveguide. In this sense, the structure is a generalized multi-mode interferometer (MMI). After optimization of the segments' width and length using genetic algorithms and a steepest-descent method, the interference pattern of at the end of the structure is matched to the mode in the photonic wire. The design process is discussed in detail in.⁷ As this optimization is purely numerical, it is not straightforward to gain insight into the design of these structures. With this technique we have calculated transmissions over 90%.

Figure 14b shows a picture of a number of spot-size converters in SOI with 5 and 10 sections. As a comparison, we also fabricated linear and parabolic tapers. In figure 14c we plotted the coupling efficiency of the optimized tapers as a function of total taper length. For the 10-section tapers, both transmission measurements with a single taper and with two tapers were performed. The transmission of parabolic and linear tapers of similar lengths is also plotted. We can see that the interference tapers have high coupling efficiencies at much shorter length than the linear and parabolic tapers.

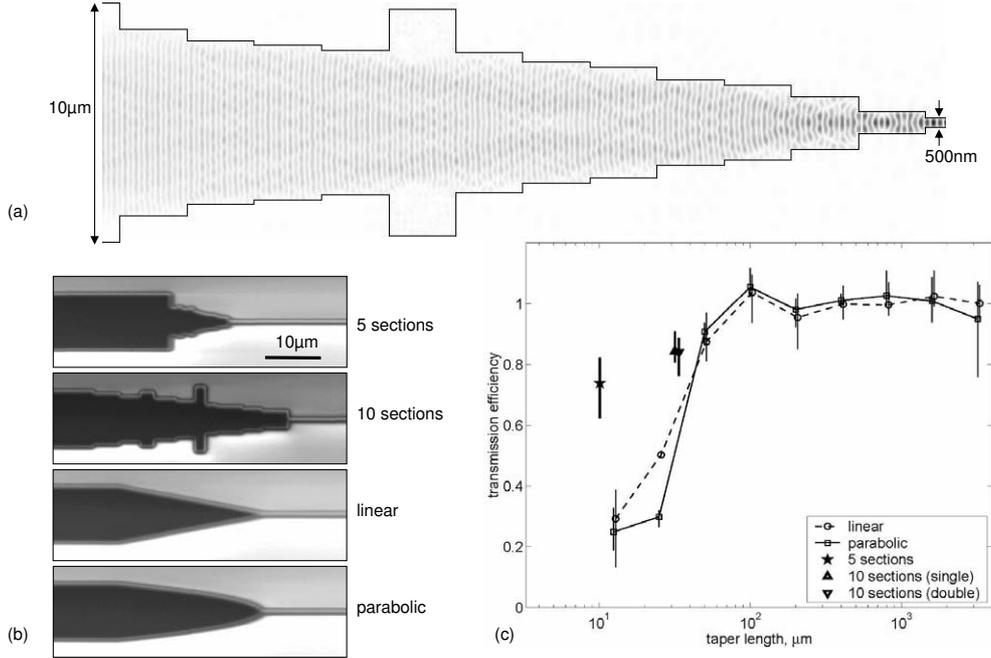


Figure 14. Short spot-size converter between a $10\mu\text{m}$ wide ridge waveguide and a 500nm wide photonic wire. (a) Simulation result of a 10-section coupler, (b) fabricated structures with 5 sections and 10 sections, as well as short linear and parabolic tapers. (c) Coupling efficiency as function of length for linear tapers, parabolic tapers and optimized interference tapers.

7. CONCLUSION

We have developed a fabrication process for nanophotonic waveguides in SOI using deep UV lithography as a pattern-definition technique. We used this process to fabricate a large variety of structures. In this paper, we have presented a number of wavelength-selective functions, including ring resonators, cascaded Mach-Zehnder filters and arrayed waveguide gratings (AWGs). All these devices show promising results. We have also discussed the issue of interfacing nanophotonic waveguides with single-mode fibers. For this, we presented grating fiber couplers, which can also act as polarization splitters, allowing for a polarization diversity approach. In combination with these grating couplers, we showed that interference-based couplers can greatly reduce the footprint of a fiber-chip interface.

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