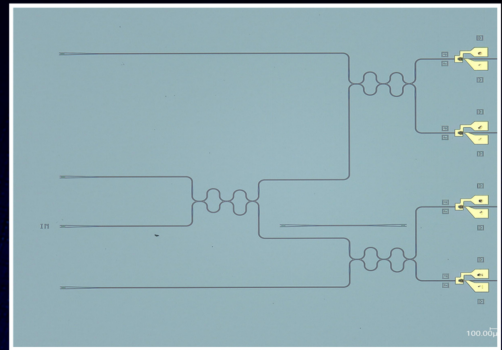
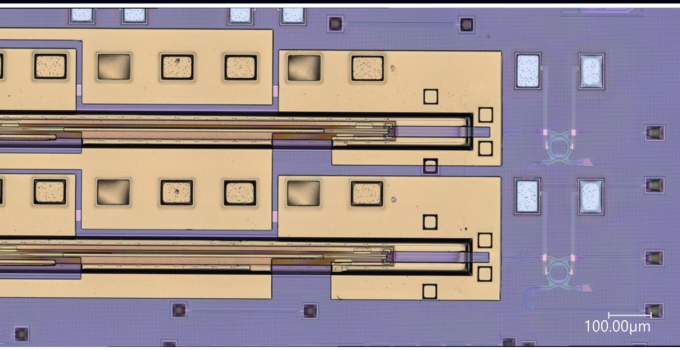




Heterogeneous Integration of Optical Receivers on Silicon and Silicon Nitride Platforms

Senbiao Qin

Doctoral dissertation submitted to obtain the academic degree of
Doctor of Photonics Engineering

Supervisors

Prof. Günther Roelkens, PhD - Prof. Johan Bauwelinck, PhD
Department of Information Technology
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Supervisors

Prof. Günther Roelkens, PhD, Ghent University

Prof. Johan Bauwelinck, PhD, Ghent University

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The past five years of my PhD journey have been filled with a wide range of emotions—struggle, anxiety, disappointment, but also joy and excitement. It has been an intense and unforgettable experience that has profoundly shaped who I am today. I believe this journey will continue to influence my life and career in meaningful ways.

Looking back, I still clearly remember the period when I was applying for PhD positions. It was April 2021, and I was about to graduate with my master's degree. I applied for numerous positions across North America and Europe and faced many rejections along the way. Eventually, I was fortunate to receive several interview invitations. Feeling both relieved and grateful, I ultimately chose PRG as my next destination. Five years later, I remain convinced that this was one of the best decisions I have ever made.

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and introduced me to everyone. Standing beside him, I recall noticing how tall he was. What impressed me most, and what has had the greatest impact on me, is not only his exceptional ability to manage and oversee a large volume of work, but also his genuine passion for research.

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*Gent, April 2026
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List of Acronyms

AI	Artificial Intelligence
APD	Avalanche Photodiode
ART	Aspect-Ratio Trapping
ASE	Amplified Spontaneous Emission
Au	Gold
AWG	Arbitrary Waveform Generator; Arrayed Waveguide Grating
BCB	Benzocyclobutene
BER	Bit Error Rate
BEOL	Back-End-Of-Line
BOE	Buffered Oxide Etching
BOX	Buried Oxide
CMOS	Complementary Metal-Oxide-Semiconductor
Co-D2W	Collective Die-to-Wafer
CWDM	Coarse Wavelength Division Multiplexing
DI	Deionized
DMRR	Dual Micro-Ring Resonator
DUT	Device Under Test
DWDM	Dense Wavelength Division Multiplexing
EBL	Electron-Beam Lithography
EDFA	Erbium-Doped Fiber Amplifier
EME	Eigenmode Expansion
EO	Electro-Optic
FBMS	Fixed-Beam Moving-Stage
FDTD	Finite-Difference Time-Domain
FDE	Finite Difference Eigenmode
FIB	Focused Ion Beam
FIR	Finite Impulse Response
FSR	Free Spectral Range

Ge	Germanium
HPC	High-Performance Computing
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IIR	Infinite Impulse Response
IMDD	Intensity Modulation Direct Detection
InP	Indium Phosphide
InGaAs	Indium Gallium Arsenide
IPA	Isopropanol
ISI	Inter-Symbol Interference
LPCVD	Low-Pressure Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy
MQW	Multi-Quantum-Well
μ TP	Micro-Transfer Printing
MUTC	Modified Uni-Traveling-Carrier
MZI	Mach-Zehnder Interferometer
MZM	Mach-Zehnder Modulator
NRE	Nano-Ridge Engineering
NRZ	Non-Return-to-Zero
NoW	Network-on-Wafer
OSM	Open-Short-Match
OSNR	Optical Signal-to-Noise Ratio
PC	Polarization Controller
PCB	Printed Circuit Board
PD	Photodiode
PDFA	Praseodymium-Doped Fiber Amplifier
PDK	Process Design Kit
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapor Deposition
PIC	Photonic Integrated Circuit
PRBS	Pseudo-Random Binary Sequence
RC	Resistance-Capacitance
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SCH	Separate Confinement Heterostructure

Si	Silicon
SiN	Silicon Nitride
SiPh	Silicon Photonics
SNR	Signal-to-Noise Ratio
SOA	Semiconductor Optical Amplifier
SOI	Silicon-On-Insulator
SWIR	Short-Wave Infrared
TEC	Thermoelectric Cooler
TIA	Transimpedance Amplifier
TMM	Transfer Matrix Method
VNA	Vector Network Analyzer
VOA	Variable Optical Attenuator
WDM	Wavelength Division Multiplexing
WPE	Wall-Plug Efficiency

Samenvatting

Inleiding

De voortdurende groei van dataverkeer in high-performance computing, kunstmatige intelligentie, cloudinfrastructuur en telecommunicatie heeft de vraag naar optische communicatiesystemen met hoge bandbreedte en energie-efficiëntie aanzienlijk doen toenemen. Optische ontvangers vormen fundamentele bouwstenen in deze systemen, waarbij gemoduleerde optische signalen worden omgezet in elektrische signalen voor verdere elektronische verwerking. De prestaties van de ontvanger hebben een directe invloed op de gevoeligheid van de verbinding, de bandbreedtedichtheid en de algehele energie-efficiëntie van het systeem.

Moderne optische communicatie bestrijkt meerdere toepassingsdomeinen, waaronder optische interconnecties met ultrakorte afstand, datacentercommunicatie (datacom) en langeafstandstelecommunicatie (telecom). Hoewel deze domeinen verschillen in transmissieafstand en systeemvereisten, delen zij een gemeenschappelijke behoefte aan compacte, hogesnelheids- en schaalbare ontvangerarchitecturen. Het realiseren van een dergelijke integratie vereist de combinatie van passieve fotonische platformen met lage verliezen en actieve componenten met hoge prestaties op basis van directe bandkloof III–V-halfgeleiders.

Dit proefschrift onderzoekt micro-transfer printing (μ TP) als een veelzijdige heterogene integratiestrategie voor het realiseren van optische ontvangers met hoge prestaties over meerdere golflengtebanden en fotonische platformen. Het werk richt zich op de integratie van III–V-fotodiodes (PD's) en halfgeleidergebaseerde optische versterkers (SOA's) op silicium-nitride (SiN) en siliciumfotonica (SiPh) platformen, met een vooruitblik op elektronisch-fotonische co-integratie.

Resultaten

Micro-transfer printing van O-band InGaAs/InP fotodiodes op een silicium-nitride fotonisch platform

Hogesnelheid InGaAs/InP gemodificeerde 'uni-traveling-carrier' (MUTC) fotodiodes werden ontworpen en heterogeen geïntegreerd op LPCVD SiN-golfsgeleiders met behulp van μ TP. Een volledige μ TP-integratieproces werd ontwikkeld [Fig. 1(a)], inclusief de fabricage van transfer-printbare PD-coupons op de III-V-bronwafer, hun transfer naar de SiN fotonisch geïntegreerde schakeling (PIC), en daaropvolgende nabewerkingsstappen na het printen.

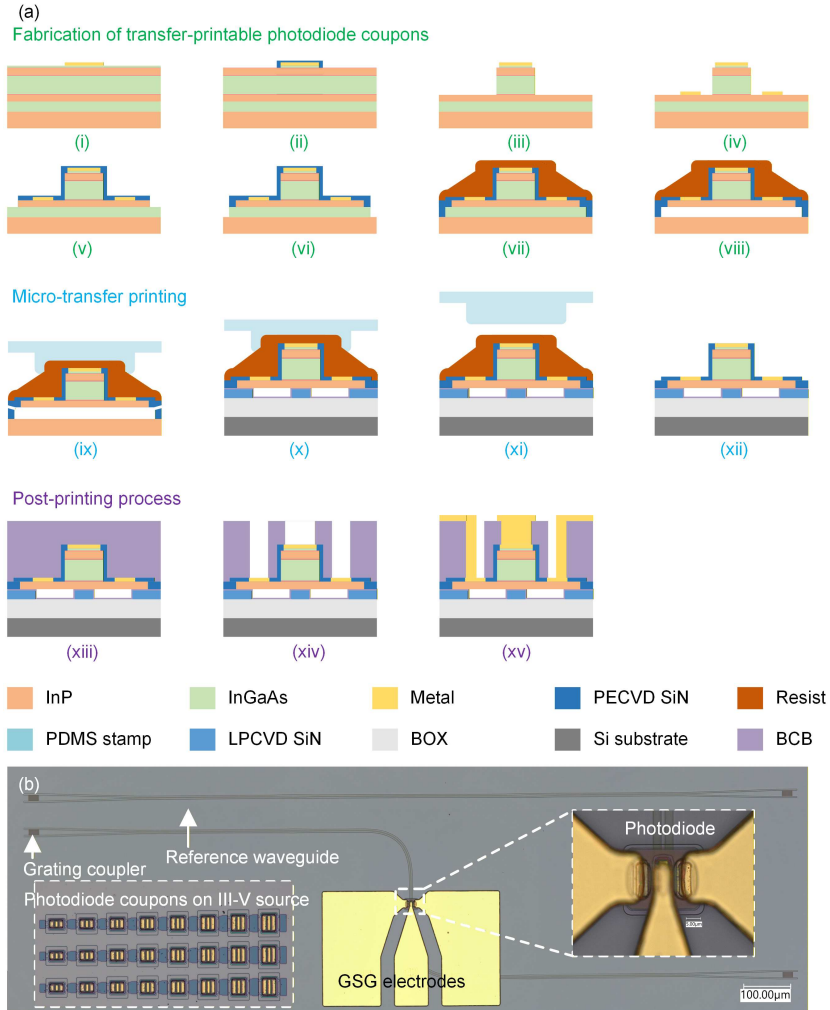
De gefabriceerde componenten [Fig. 1(b)] vertonen een lage donkerstroom van minder dan 38 nA bij een bias-spanning van -2 V [Fig. 2(a)]. Een responsiviteit van 1 A/W, overeenkomend met een kwantumefficiëntie van 95%, werd bereikt bij een golflengte van 1310 nm [Fig. 2(b)]. Bovendien werd een 3-dB bandbreedte van 37 GHz verkregen, wat 12 GHz hoger is dan die van een referentie PIN-PD, toegeschreven aan het gedeeltelijk gedopeerde absorberontwerp [Fig. 2(c)].

Grootsignaalmetingen tonen duidelijke open oogdiagrammen tot 40 Gbit/s voor non-return-to-zero (NRZ) modulatie [Fig. 2(d)]. Deze resultaten tonen aan dat μ TP de integratie van hogesnelheidsfotodetectie op SiN-fotonische schakelingen mogelijk maakt.

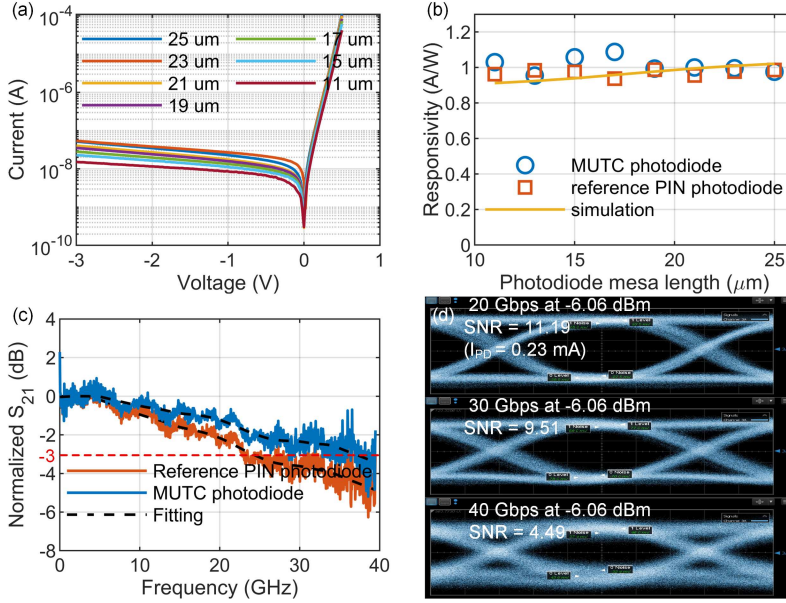
O-band 4×32 Gbit/s CWDM-ontvanger op silicium-nitride met micro-transfer-geprinte InGaAs/InP-fotodiodes

Voortbouwend op de demonstratie op componentniveau werd een 4×32 Gbit/s O-band 'coarse wavelength-division multiplexed' (CWDM) ontvanger gerealiseerd op een SiN-fotonisch platform, door middel van micro-transfer-geprinte InGaAs/InP PD's. De ontvanger integreert een gecascadeerde Mach-Zehnder-interferometer (MZI) roosterfilter-demultiplexer met vier hogesnelheids-PD's [Fig. 3], en behaalt een laag verlies (1.7–2.4 dB) en een overspraak minder dan -14 dB over het 1270–1330 nm golflengtebereik [Fig. 4(a)]. Hogesnelheid 'back-to-back' ontvangst van 32 Gbit/s NRZ-signalen wordt gedemonstreerd op alle kanalen, met duidelijke oogdiagrammen en bitfoutkansen (BER's) onder 10^{-4} bij ontvangen optische vermogens boven -11 dBm, gerealiseerd zonder gebruik van een transimpedantie-versterker [Fig. 4(b) en (c)].

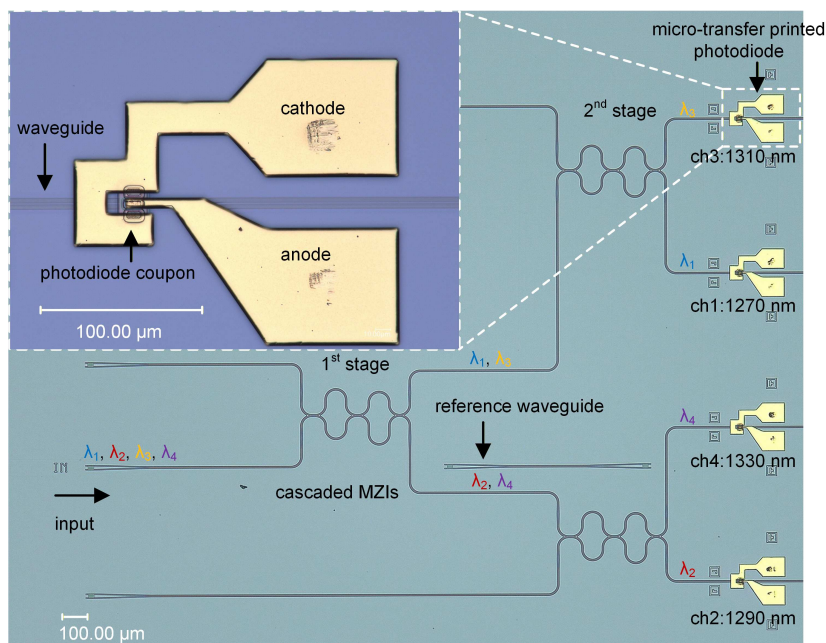
Deze systeemniveau-demonstratie bevestigt de schaalbaarheid van μ TP voor meerkanaals datacom-ontvangerarchitecturen. Daarnaast biedt de combinatie van het SiN-platform en de roosterfilterarchitectuur een breedbandige en fabricagetolerante demultiplexeringsrespons, en wordt verwacht dat deze een verbeterde robuustheid tegen temperatuurvariaties zal bieden dankzij de relatief lage thermo-optische



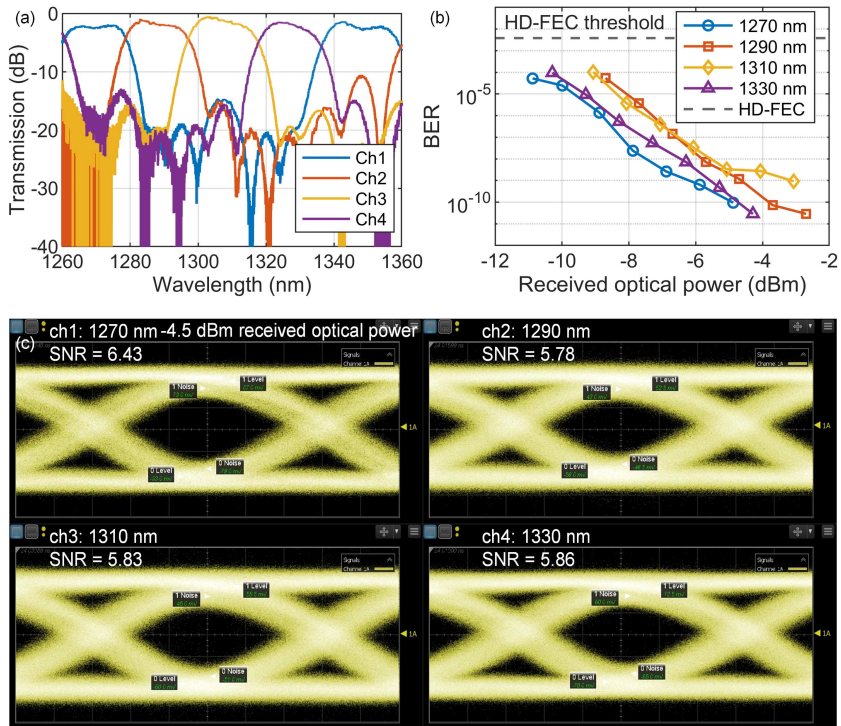
Figuur 1: Fabricage en integratie van InGaAs/InP MUTC-fotodiodes op een SiN-fotonisch platform. (a) Schematische weergave van het proces, inclusief de fabricage van transfer-printbare fotodiode (PD)-coupons op de III-V-bronwafer, micro-transfer printing (μ TP) op de SiN-fotonisch geïntegreerde schakeling (PIC), en daaropvolgende nabewerkingsstappen na het printen. (b) Optische microscoopbeelden van de gefabriceerde PD-coupons op het III-V-bronsubstraat en een representatieve golfgeleider-geïntegreerde PD na transfer printing op de SiN PIC. De inzet toont een ingezoomde weergave van de geïntegreerde fotodiode.



Figuur 2: Prestaties van de gefabriceerde micro-transfer-geprinte InGaAs/InP-fotodiodes geïntegreerd op een SiN-fotonisch platform. (a) Stroom–spanningskarakteristieken (I–V) van fotodiodes (PD's) met verschillende mesa-lengtes. (b) Gemeten responsiviteit van MUTC-PD's en referentie PIN-PD's als functie van de mesa-lengte bij een bias-spanning van -2 V en een golflengte van 1310 nm. (c) Genormaliseerde S_{21} -frequentierespons van een 11- μm lange MUTC-PD en een referentie PIN-PD met dezelfde mesa-lengte, gemeten bij een bias-spanning van -2 V. De stippellijn geeft de gefitte respons aan. (d) Gemeten oogdiagrammen die NRZ-werking tot 40 Gbit/s aantonen bij een optisch ingangsvermogen van -6.06 dBm.



Figuur 3: Microscoopbeeld van de O-band vierkanaals CWDM-ontvanger PIC, met de inzet die een vergrote weergave toont van een micro-transfer-geprinte fotodiode.

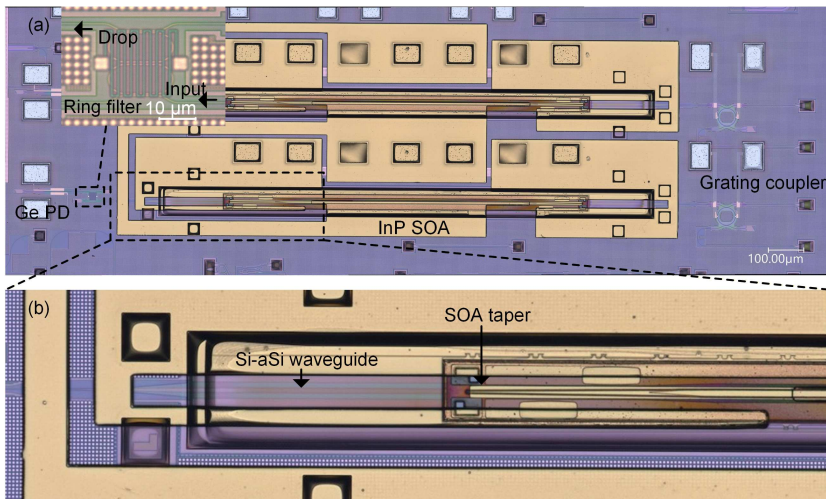


Figuur 4: Prestaties van de O-band vierkanaals CWDM-ontvanger. (a) Gemeten transmissiespectra van de vierkanaals demultiplexer, die kanaalscheiding tonen over het 1270–1330 nm golflengtegebied. (b) Bitfoutkans (BER) als functie van het ontvangen optisch vermogen voor alle kanalen, wat werking onder de HD-FEC-drempel aangeeft. (c) Back-to-back oogdiagrammen bij 32 Gbit/s NRZ voor de vier golflengtekanalen, die duidelijke oogopeningen en consistente hogesnelheidsontvangstprestaties over alle kanalen aantonen.

gevoeligheid van SiN.

Micro-transfer printing van InP SOA's voor C-band voorversterkte ontvangers

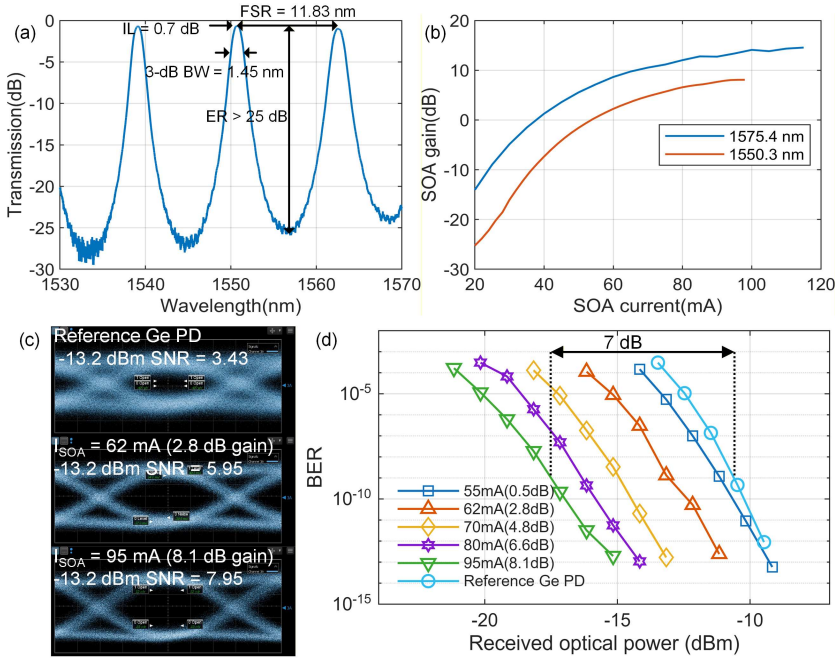
Om de veelzijdigheid van μ TP en de compatibiliteit met back-end-of-line (BEOL) processen aan te tonen, werd een C-band voorversterkte ontvanger gerealiseerd op een geavanceerd siliciumfotonica-platform door een InP SOA vóór een hogesnelheids germanium (Ge) fotodiode te integreren. De ontvanger werd gerealiseerd op imec's iSiPP200-platform, waarbij een micro-transfer-geprinte InP-gebaseerde quantum-well SOA, een 50 GHz Ge-fotodiode en een thermisch afstembare dubbele micro-ringresonator (DMRR)-filter werden gecombineerd om versterkte spontane emissie (ASE)-ruis buiten de signaalband te onderdrukken [Fig. 5].



Figuur 5: Microscoopbeelden van de gefabriceerde voorversterkte ontvanger. (a) Overzicht van de layout, inclusief de InP SOA, Ge-fotodiode en roosterkoppelaars; de inzet toont een ingezoomde weergave van het dubbele micro-ringresonator (DMRR)-filter. (b) Detailweergave van de SOA-taperregio.

De DMRR-filter vertoonde een drop-port verlies van 0.7 dB, een 3-dB bandbreedte van 1.45 nm en een extinctieverhouding van meer dan 25 dB [Fig. 6(a)]. De geïntegreerde SOA vertoonde on-chip kleinsignaalversterkingen tot 14.6 dB bij 1575.4 nm, terwijl de SOA een on-chip versterking van 8.1 dB leverde bij 1550.3 nm (golflengte gebruikt in het hoge-snelheidsexperiment) [Fig. 6(b)]. Hogesnelheidsmetingen toonden verder 30 Gbit/s NRZ-ontvangst aan, met een verbetering van de ontvangergevoeligheid van ongeveer 7 dB bij een bitfoutkans (BER) van 10^{-9} ten opzichte van een referentie Ge-fotodiode zonder SOA-voorversterking [Fig. 6(c) en

(d)]. Micro-transfer printing maakt de heterogene integratie van III–V SOA's op een CMOS-compatibel siliciumfotonica-platform mogelijk en biedt een praktische route naar compacte en zeer gevoelige voorversterkte ontvangers voor toekomstige optische communicatie in de C-band.



Figuur 6: Prestaties van de voorversterkte ontvanger. (a) Gemeten transmissiespectrum van de dubbele micro-ringresonator (DMRR)-filter, met een 3-dB bandbreedte van 1.45 nm, een vrije spectrale afstand (FSR) van 11.83 nm en een extinctieverhouding van meer dan 25 dB. (b) Gemeten on-chip SOA-versterking als functie van de injectiestroom bij golflengtes van 1575.4 nm en 1550.3 nm. (c) Gemeten 30 Gbit/s NRZ-oogdiagrammen bij een ontvangen optisch vermogen van -13.2 dBm voor verschillende SOA-biasstromen, vergeleken met een referentie Ge-fotodiode. (d) Bitfoutkans (BER) als functie van het ontvangen optisch vermogen voor verschillende SOA-biasstromen, die een verbetering van de ontvangergevoeligheid van ongeveer 7 dB tonen ten opzichte van de referentie Ge-fotodiode.

Conclusie

Dit proefschrift heeft micro-transfer printing (μ TP) aangetoond als een veelzijdige en schaalbare heterogene integratiestrategie voor het realiseren van optische ontvangers met hoge prestaties over meerdere fotonische platformen en golflengtebanden. Op componentniveau werden hogesnelheids InGaAs/InP-fotodiodes

succesvol geïntegreerd op een silicium-nitride (SiN) platform, met hoge responsiviteit, lage donkerstroom en bandbreedtes boven 37 GHz. Hierop voortbouwend werd een 4×32 Gbit/s O-band CWDM-ontvanger gerealiseerd op SiN, wat de schaalbaarheid van μ TP voor meerkanaalsontvangerarchitecturen bevestigt. Op systeemniveau maakte de integratie van InP halfgeleider optische versterkers (SOA's) op een silicium fotonica-platform een C-band voorversterkte ontvanger mogelijk, met een verbetering van de ontvangergevoeligheid van ongeveer 7 dB.

Samen tonen deze resultaten aan dat μ TP zowel fotodetectie- als optische versterkingsfunctionaliteiten heterogeen kan integreren op passieve fotonische schakelingen zonder aanpassing van de front-end fabricageprocessen. Door de fabricage van actieve III–V componenten los te koppelen van het passieve fotonische platform en integratie in de back-end-of-line (BEOL) mogelijk te maken, biedt μ TP een flexibel en platformonafhankelijk pad naar compacte, hoogpresterende en energie-efficiënte optische ontvangers. Dit werk legt een basis voor toekomstige heterogene fotonische systemen en opent de weg naar meer geavanceerde elektronisch–fotonische co-integratie in volgende generatie optische interconnects.

Summary

Introduction

The continuous growth of data traffic in high-performance computing, artificial intelligence, cloud infrastructure, and telecommunications has significantly increased the demand for high-bandwidth and energy-efficient optical communication systems. Optical receivers are fundamental building blocks in these systems, converting modulated optical signals into electrical signals for subsequent electronic processing. The performance of the receiver directly impacts link sensitivity, bandwidth density, and overall system energy efficiency.

Modern optical communication spans multiple application domains, including ultra-short-reach optical interconnects, data center communication (datacom), and long-haul telecommunications (telecom). While these domains differ in transmission distance and system requirements, they share a common need for compact, high-speed, and scalable receiver architectures. Achieving such integration requires combining low-loss passive photonic platforms with high-performance active devices based on direct-bandgap III–V semiconductors.

This thesis investigates micro-transfer printing (μ TP) as a versatile heterogeneous integration strategy for realizing high-performance optical receivers across multiple wavelength regimes and photonic platforms. The work focuses on integrating III–V photodiodes (PDs) and semiconductor optical amplifiers (SOAs) onto silicon nitride (SiN) and silicon photonics (SiPh) platforms, with an outlook toward electronic–photonic co-integration.

Results

Micro-transfer printing of O-band InGaAs/InP photodiodes on a silicon nitride photonic platform

High-speed InGaAs/InP modified uni-traveling-carrier (MUTC) PDs were designed and heterogeneously integrated onto LPCVD SiN waveguides using μ TP. A com-

plete μ TP integration process flow was developed [Fig. 7(a)], including the fabrication of transfer-printable PD coupons on the III–V source wafer, their transfer onto the SiN photonic integrated circuit (PIC), and subsequent post-printing processing steps.

The fabricated devices [Fig. 7(b)] exhibit a low dark current below 38 nA at a bias voltage of -2 V [Fig. 8(a)]. A responsivity of 1 A/W, corresponding to a quantum efficiency of 95%, was achieved at a wavelength of 1310 nm [Fig. 8(b)]. Furthermore, a 3-dB bandwidth of 37 GHz was obtained, which is 12 GHz higher than that of a reference PIN PD, attributed to the partially doped absorber design [Fig. 8(c)].

Large-signal measurements show clear open eye diagrams up to 40 Gbit/s using non-return-to-zero (NRZ) modulation [Fig. 8(d)]. These results demonstrate that μ TP enables the integration of high-speed photodetection functionality onto SiN photonic circuits.

O-band 4×32 Gbit/s CWDM receiver on silicon nitride with micro-transfer-printed InGaAs/InP photodiodes

Building upon the device-level demonstration, a 4×32 Gbit/s O-band coarse wavelength-division multiplexed (CWDM) receiver was implemented on a SiN photonic platform, enabled by micro-transfer printed InGaAs/InP PDs. The receiver integrates a cascaded Mach–Zehnder interferometer (MZI) lattice filter demultiplexer with four high-speed PDs [Fig. 9], achieving low insertion loss (1.7–2.4 dB) and crosstalk below -14 dB across the 1270–1330 nm wavelength grid [Fig. 10(a)]. High-speed back-to-back reception of 32 Gbit/s NRZ signals is demonstrated on all channels, with clear eye diagrams and bit-error rates (BERs) below 10^{-4} at received optical powers above -11 dBm, achieved without the use of a transimpedance amplifier [Fig. 10(b) and (c)].

This system-level demonstration confirms the scalability of μ TP for multi-channel datacom receiver architectures. In addition, the combination of the SiN platform and the lattice filter architecture provides a broadband and fabrication-tolerant wavelength demultiplexing response, and is expected to offer improved robustness to temperature variations due to the relatively low thermo-optic sensitivity of SiN.

Micro-transfer printing of InP SOAs on an advanced silicon photonics platform for C-band pre-amplified receivers

To demonstrate the versatility of μ TP and its compatibility with back-end-of-line (BEOL) processes, a C-band pre-amplified receiver was implemented on an advanced silicon photonics platform by integrating an InP SOA in front of a high-

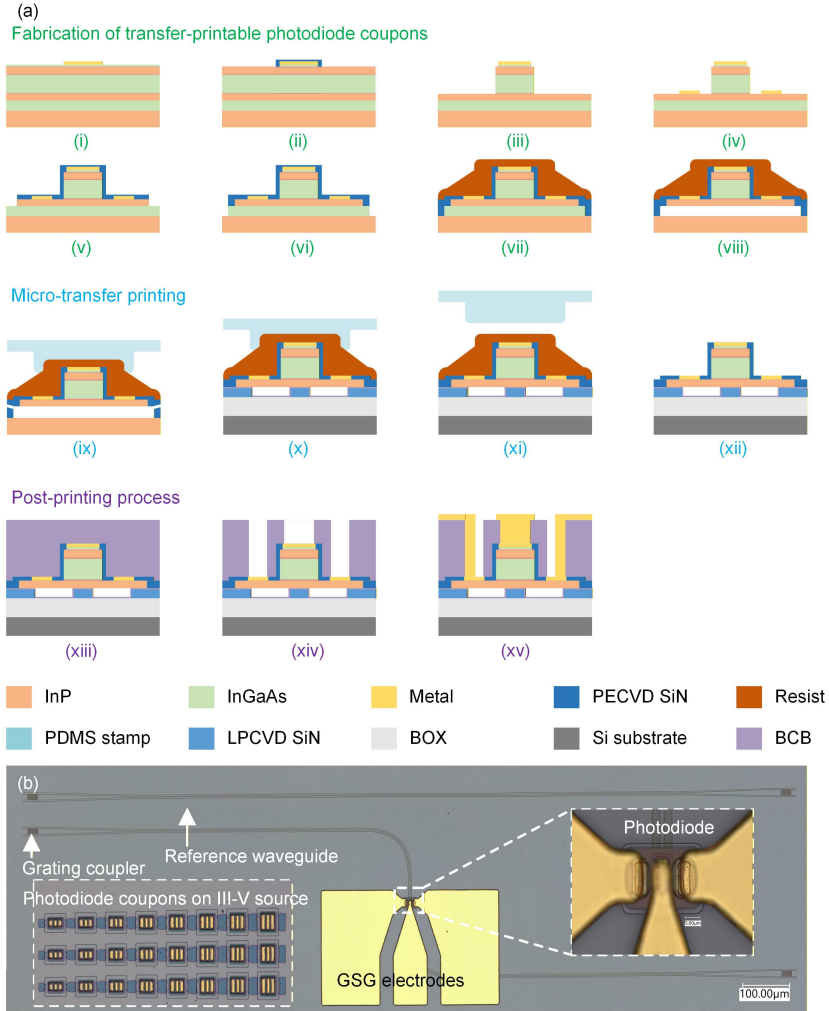


Figure 7: Fabrication and integration of InGaAs/InP MUTC photodiodes on a SiN photonic platform. (a) Schematic illustration of the process flow, including the fabrication of transfer-printable photodiode (PD) coupons on the III-V source wafer, micro-transfer printing (μ TP) onto the SiN photonic integrated circuit (PIC), and subsequent post-printing processing steps. (b) Optical microscope images of the fabricated PD coupons on the III-V source substrate and a representative waveguide-integrated PD after transfer printing onto the SiN PIC. The inset shows a zoomed-in view of the integrated photodiode.

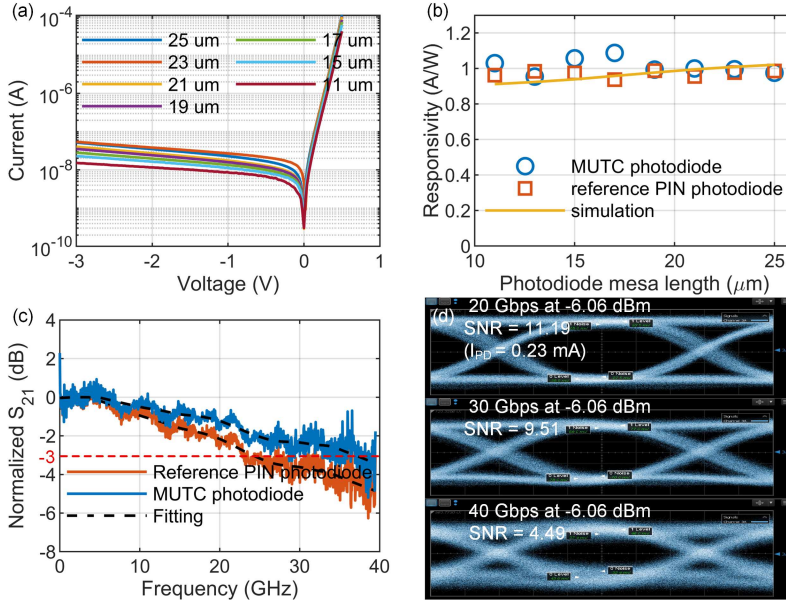


Figure 8: Performance of the fabricated micro-transfer-printed InGaAs/InP photodiodes integrated on a SiN photonic platform. (a) Current-voltage (I - V) characteristics of photodiodes (PDs) with different mesa lengths. (b) Measured responsivity of MUTC PDs and reference PIN PDs as a function of mesa length at a bias voltage of -2 V and a wavelength of 1310 nm. (c) Normalized S_{21} frequency response of an 11- μm -long MUTC PD and a reference PIN PD with the same mesa length, measured at a bias voltage of -2 V. The dashed line indicates the fitted response. (d) Measured eye diagrams demonstrating NRZ operation up to 40 Gbit/s at an input optical power of -6.06 dBm.

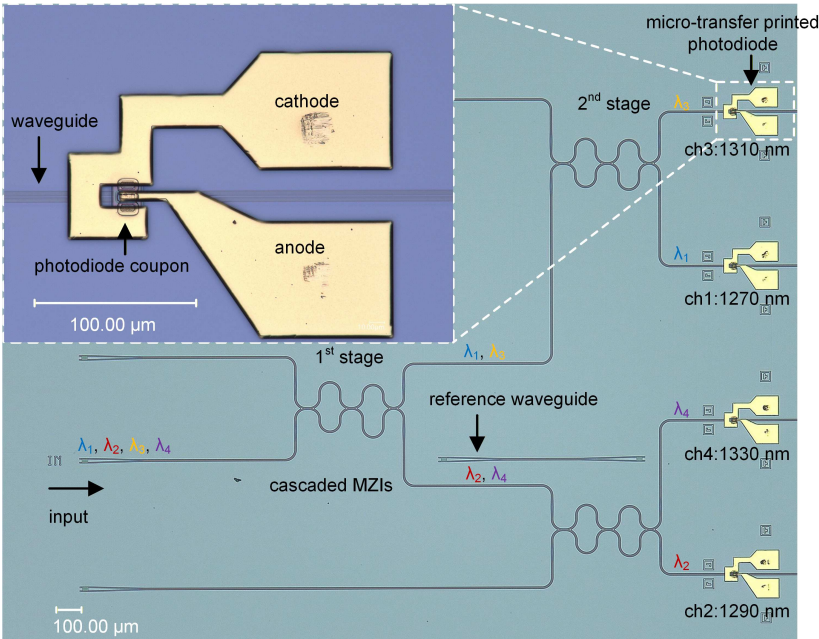


Figure 9: Microscope image of the O-band four-channel CWDM receiver PIC, with the inset showing a magnified view of a micro-transfer printed photodiode.

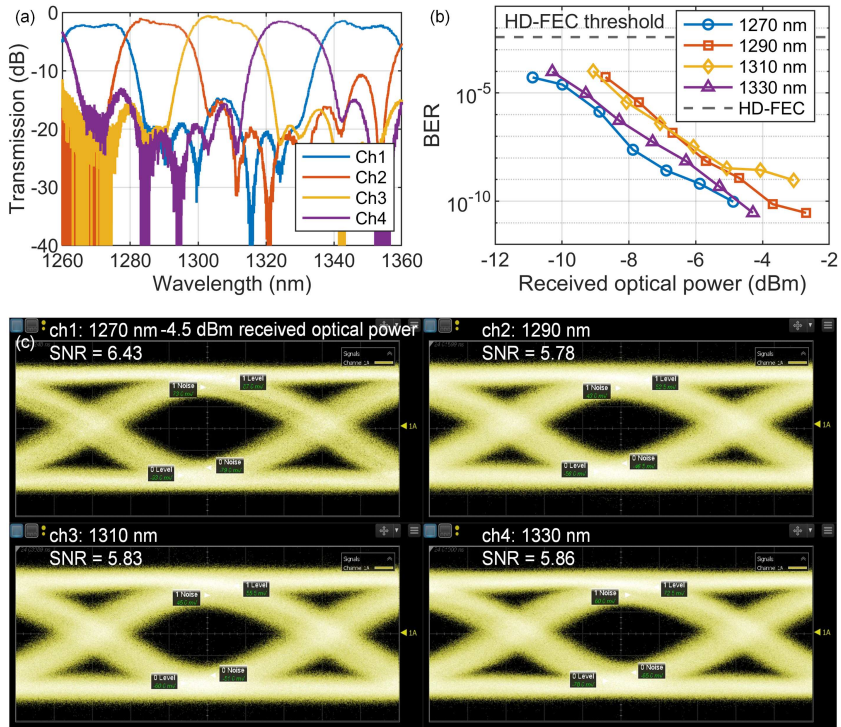


Figure 10: Performance of the O-band four-channel CWDM receiver. (a) Measured transmission spectra of the four-channel demultiplexer, showing channel separation over the 1270–1330 nm wavelength grid. (b) Bit-error rate (BER) as a function of received optical power for all channels, indicating operation below the HD-FEC threshold. (c) Back-to-back eye diagrams at 32 Gbit/s NRZ for the four wavelength channels, demonstrating clear eye openings and consistent high-speed reception performance across all channels.

speed germanium (Ge) PD. The receiver was realized on imec's iSiPP200 platform, combining a transfer-printed InP-based quantum-well SOA, a 50 GHz Ge PD, and a thermally tunable dual micro-ring resonator (DMRR) filter for suppressing out-of-band amplified spontaneous emission (ASE) noise [Fig. 11].

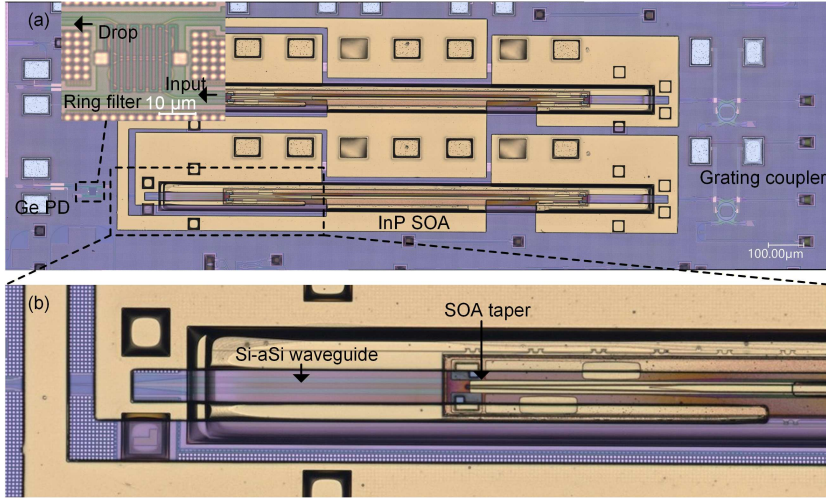


Figure 11: Microscope images of the fabricated pre-amplified receiver. (a) Overview of the device layout, including the InP SOA, Ge photodiode, and grating couplers; the inset shows a zoomed-in view of the dual micro-ring resonator (DMRR) filter. (b) Close-up view of the SOA taper region.

The DMRR filter showed a drop-port insertion loss of 0.7 dB, a 3-dB bandwidth of 1.45 nm, and an extinction ratio exceeding 25 dB [Fig. 12(a)]. The integrated SOA exhibited on-chip small-signal gains up to 14.6 dB at 1575.4 nm, while the device used in the high-speed experiment provided 8.1 dB on-chip gain at 1550.3 nm [Fig. 12(b)]. High-speed measurements further demonstrated 30 Gbit/s NRZ reception, with a receiver sensitivity improvement of approximately 7 dB at a bit-error rate (BER) of 10^{-9} compared with a reference Ge PD without SOA pre-amplification [Fig. 12(c) and (d)]. Micro-transfer printing enables the heterogeneous integration of III-V SOAs on a CMOS-compatible silicon photonics platform, providing a practical route toward compact and high-sensitivity pre-amplified receivers for future C-band optical communication.

Conclusion

This thesis has demonstrated micro-transfer printing (μ TP) as a versatile and scalable heterogeneous integration strategy for realizing high-performance optical

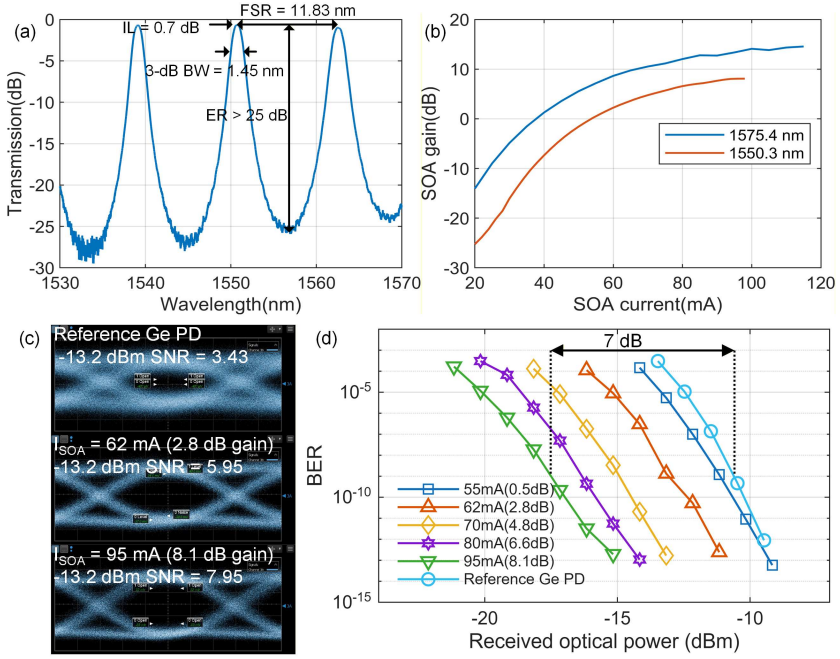


Figure 12: Performance of the pre-amplified receiver. (a) Measured transmission spectrum of the dual micro-ring resonator (DMRR) filter, indicating a 3-dB bandwidth of 1.45 nm, a free spectral range (FSR) of 11.83 nm, and an extinction ratio exceeding 25 dB. (b) Measured on-chip SOA gain as a function of injection current at wavelengths of 1575.4 nm and 1550.3 nm. (c) Measured 30 Gbit/s NRZ eye diagrams at a received optical power of -13.2 dBm for different SOA bias currents, compared with a reference Ge photodiode. (d) Bit-error rate (BER) as a function of received optical power for different SOA bias currents, showing a receiver sensitivity improvement of approximately 7 dB compared with the reference Ge photodiode.

receivers across multiple photonic platforms and wavelength regimes. At the device level, high-speed InGaAs/InP photodiodes were successfully integrated onto a silicon nitride (SiN) platform, achieving high responsivity, low dark current, and bandwidths exceeding 37 GHz. Building upon this, a 4×32 Gbit/s O-band CWDM receiver was realized on SiN, confirming the scalability of μ TP for multi-channel receiver architectures. At the system level, the integration of InP semiconductor optical amplifiers (SOAs) onto a silicon photonics platform enabled a C-band pre-amplified receiver, demonstrating a receiver sensitivity improvement of approximately 7 dB.

Together, these results highlight the capability of μ TP to heterogeneously integrate both photodetection and optical gain functionalities onto passive photonic circuits without modification of the front-end fabrication processes. By decoupling the fabrication of active III–V devices from the passive photonic platform and enabling deterministic integration at the back-end-of-line (BEOL), μ TP provides a flexible and platform-agnostic pathway toward compact, high-performance, and energy-efficient optical receivers. This work establishes a foundation for future heterogeneous photonic systems and paves the way toward more complex electronic–photonic co-integration in next-generation optical interconnects.

1

Introduction

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1.1 Evolution of optical receivers across communication scales

The rapid growth of artificial intelligence (AI), high-performance computing (HPC), cloud infrastructure, and global telecommunications has driven an unprecedented demand for bandwidth density and energy efficiency in communication systems. As computing architectures transition from monolithic scaling to chiplet-based and heterogeneous integration paradigms, communication increasingly becomes a primary bottleneck in terms of both system performance and power consumption [1–3]. Optical technologies, long established in long-haul fiber networks, are now penetrating progressively shorter communication scales — from metro links to data centers, and ultimately to chip-to-chip and wafer-scale interconnects.

Across these regimes, optical receivers serve as fundamental building blocks. They convert modulated optical signals into electrical signals for subsequent electronic processing, and their performance directly impacts bandwidth, sensitivity, energy consumption, and integration density. While communication distances and system constraints differ significantly across application domains, a common trend emerges: the need for compact, high-speed, energy-efficient, and heterogeneously integrated optical receivers.

This section examines the evolution of optical receiver requirements across three communication scales — ultra-short-reach interconnects, short-reach datacom systems, and metro/long-haul telecom links — before identifying the common integration challenges that motivate the research presented in this thesis. The shift in dominant system constraints across these distance regimes is conceptually illustrated in Fig. 1.1.

1.1.1 Ultra-short-reach optical interconnect

Ultra-short-reach optical interconnect encompasses communication distances ranging from millimeters to several meters, including chip-to-chip communication within a package [4], co-packaged optics adjacent to switching ASICs [5, 6], board-level optical links [7, 8], and emerging wafer-scale optical interposers [9, 10].

At these scales, the dominant constraint is no longer fiber loss or chromatic dispersion, but rather *energy per transmitted bit* and *bandwidth density*. As multi-chiplet architectures replace monolithic scaling, inter-chip communication must support aggregate bandwidths in the terabit-per-second regime while maintaining stringent power budgets.

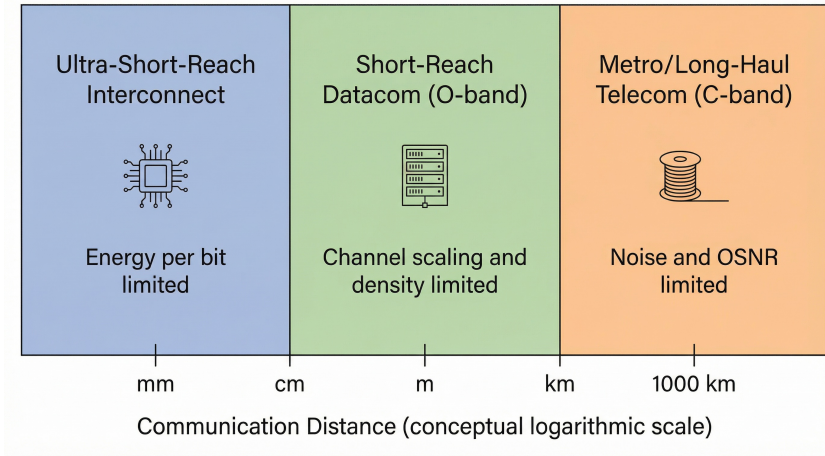


Figure 1.1: Conceptual illustration of optical communication regimes across distance scales, highlighting the shift in dominant system constraints from energy-per-bit limitations in ultra-short-reach interconnects, to channel density constraints in short-reach datacom (O-band) systems, and to noise and OSNR limitations in metro and long-haul telecom (C-band) systems.

Electrical interconnects perform well over short on-chip distances; however, their bandwidth density and energy efficiency degrade rapidly as interconnect length increases due to the scaling of resistive–capacitive (RC) effects, signal integrity degradation, and the increased power required for equalization. These limitations become particularly severe in wafer-scale systems, where communication distances can reach tens of centimeters.

A representative system-level example of this challenge is the photonic Network-on-Wafer (NoW) GPU architecture proposed in [10], which employs a wafer-scale optical interposer to implement an inter-GPU communication fabric. The bandwidth-density–energy scaling trends reported in [10] are reproduced in Fig. 1.2, comparing between conventional chip-scale electrical interconnects and projected wafer-scale photonic approaches.

In this architecture, multiple GPU chiplets are mounted on a common substrate and interconnected through optical I/O interfaces, photonic switching elements, and optical waveguides. A key observation is that electrical interconnects exhibit a steep degradation in bandwidth density per unit energy as the interconnect length increases into the centimeter regime, whereas optical interconnects can sustain high bandwidth density with comparatively weak dependence on transmission distance. This scaling behavior motivates the exploration of photonic interconnect fabrics for

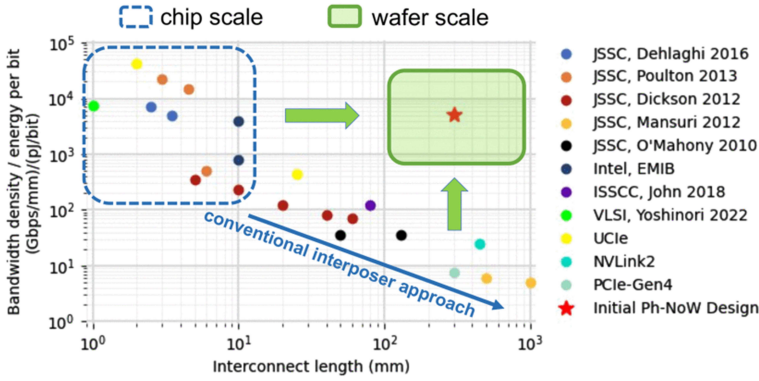


Figure 1.2: Bandwidth density per energy per bit as a function of interconnect length, reproduced from [10]. The figure highlights the efficiency limitations of conventional chip-scale electrical interconnects and the projected advantages of wafer-scale photonic approaches.

wafer-scale computing systems.

This extreme-case scenario highlights several key requirements for ultra-short-reach optical receivers:

- Per-wavelength data rates in the tens of gigabits per second, supported by sufficient electrical bandwidth to enable energy-efficient NRZ operation,
- Low device capacitance and minimized parasitic resistance and inductance to preserve signal integrity at high speed,
- Dense integration compatible with electronic co-packaging and short electrical interconnects,
- Extremely low energy per transmitted bit to meet system-level power constraints,
- Scalability to multi-channel wavelength-division multiplexed (WDM) architectures for achieving high aggregate bandwidth.

This motivates the use of low-loss waveguide platforms, such as LPCVD SiN, for wafer-scale optical routing, where the link length can extend from chip-scale distances to tens of centimeters or even the meter scale. However, a scalable wafer-scale photonic interconnect requires more than only low-loss passive waveguides. In addition to the SiN routing layer, efficient electro-optic modulators are required,

for example based on LiNbO_3 or III–V electro-absorption modulators. Photonic switching can be implemented using thermally tuned SiN/SOI interferometric circuits or, for faster and lower-energy reconfiguration, LiNbO_3 -based switching elements. On the receiver side, high-speed and low-capacitance photodetectors must be integrated close to TIAs to minimize parasitic capacitance and preserve sensitivity at high data rates. For longer or more complex routing paths, where waveguide, coupler, and switching losses accumulate, integrated optical gain may also be required to maintain sufficient link margin.

The receiver designs proposed in this thesis contribute to this scaling challenge at several levels. First, the use of a low-loss SiN platform supports longer on-interposer or wafer-scale optical routing, where propagation loss must remain small over long paths. This is particularly important for the longer-distance links in Fig. 1.2, where the main advantage of photonics comes from its weak energy scaling with distance. Second, the demonstrated O-band CWDM receiver shows how multiple wavelength channels can be demultiplexed and detected on the same SiN platform, thereby increasing the aggregate bandwidth. The low thermo-optic coefficient of SiN also improves the thermal stability of wavelength-selective filters, reducing the need for active temperature control and therefore lowering system-level power consumption. Third, the co-integration of III–V photodetectors with front-end electronic circuits is being investigated in parallel by collaborators within the group [11]. Although this co-integration is not demonstrated in this thesis, it represents a complementary route toward compact receiver implementations with reduced electrical interconnect parasitics, improved sensitivity, and high-speed operation for short chip-to-chip and chip-to-interposer links. Finally, the integration of SOAs provides a possible route to compensate accumulated routing and switching losses in more complex wafer-scale photonic fabrics.

Therefore, the proposed receivers support the scaling of the different links shown in Fig. 1.2 by combining three key elements: low-loss SiN routing for longer interconnect distances, WDM receiver architectures for higher aggregate bandwidth density, and heterogeneous integration of active III–V/electronic components for compact, sensitive, and energy-efficient optical I/O. These features directly address the bandwidth-density–energy bottleneck that limits conventional electrical interconnects as the communication distance increases.

1.1.2 Short-reach datacom (O-band)

Short-reach optical communication systems operate over distances ranging from several meters to a few kilometers, typically within and between data centers. In this regime, cost, energy efficiency, and integration density are the primary design

drivers, and links are predominantly implemented using intensity-modulation and direct-detection (IMDD) architectures. Aggregate link capacities have evolved from early 100 Gb/s interfaces to 400 Gb/s and 800 Gb/s deployments, and continue to scale through parallelism across multiple electrical lanes and wavelength-division multiplexing (WDM) [12, 13]. These trends reflect the increasing bandwidth demands of cloud computing and hyperscale data center networks, where optical interconnects progressively replace electrical links as data rates and reach requirements increase [14].

The O-band (1260–1360 nm), centered near 1310 nm, is widely adopted for short-reach datacom due to the near-zero chromatic dispersion of standard single-mode fiber. This property simplifies link design and eliminates the need for dispersion compensation over typical data center distances. Although C-band devices are also investigated in this thesis to verify the heterogeneous SOA integration concept, the O-band is particularly attractive for practical data center interconnects. In addition, O-band quantum-dot (QD) SOAs are promising for such applications because the stronger carrier confinement in QD active regions can provide improved temperature stability and a lower noise figure compared with conventional quantum-well SOAs. These properties are beneficial for low-noise optical pre-amplification in compact and energy-efficient datacom receivers. Architectures such as CWDM4 employ multiple wavelength channels to scale total throughput while maintaining manageable per-lane data rates. A conceptual O-band WDM receiver architecture is illustrated in Fig. 1.3.

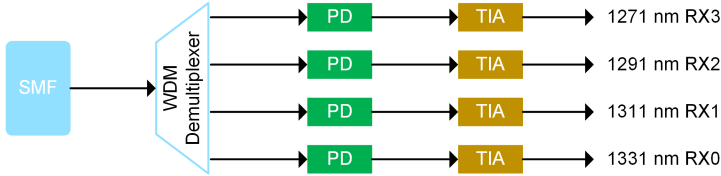


Figure 1.3: Conceptual O-band WDM receiver architecture. An incoming multi-wavelength optical signal in the O-band (1271–1331 nm) is demultiplexed into four wavelength channels and detected by parallel photodiodes with dedicated transimpedance amplifiers (TIAs).

The receiver requirements in this regime include:

- High responsivity to relax transmitter power requirements and improve link energy efficiency,
- Electrical bandwidth sufficient to support tens of gigabits per second per lane

(typically 20–40 GHz depending on the modulation format),

- Compact integration of wavelength demultiplexers and photodetector arrays to enable scalable WDM receiver architectures,
- Cost-effective, CMOS-compatible manufacturing suitable for high-volume deployment.

As aggregate bandwidth increases, the integration of wavelength filtering and high-speed photodetection on a single photonic integrated circuit becomes essential. Silicon photonics has emerged as a dominant platform for high-volume datacom applications due to its CMOS compatibility and mature ecosystem, enabling monolithic integration of germanium photodiodes for O-band detection. In contrast, silicon nitride (SiN) platforms offer ultra-low propagation loss and broadband operation but lack intrinsic optical absorption at near-infrared communication wavelengths, thereby requiring heterogeneous integration of direct-bandgap semiconductors for photodetection.

Chapters 2 and 3 of this thesis address these challenges through the micro-transfer printing integration of high-speed InGaAs/InP photodiodes onto low-loss silicon nitride photonic circuits, and demonstrate a multi-channel O-band CWDM receiver.

1.1.3 Metro and long-haul telecom (C-band)

Telecommunication systems operating over metro, regional, and long-haul distances — spanning tens to thousands of kilometers — present a fundamentally different set of constraints. These systems predominantly operate in the C-band (1530–1565 nm), where fiber attenuation is minimal and erbium-doped fiber amplifiers (EDFAs) are well established.

In contrast to interconnect and datacom systems, telecom links are typically *noise-limited* rather than bandwidth-limited. Optical amplification compensates fiber attenuation but introduces amplified spontaneous emission (ASE) noise, placing stringent requirements on receiver sensitivity and optical signal-to-noise ratio (OSNR) tolerance.

The receiver requirements in this regime therefore include:

- High sensitivity under amplified noise conditions,
- Compatibility with optical pre-amplification,
- Wide dynamic range and tolerance to amplified optical power levels,

- Support for advanced modulation formats.

Pre-amplified receiver architectures place a semiconductor optical amplifier (SOA) in front of the photodetector to boost the optical signal prior to detection and thereby enhance receiver sensitivity. Integrating optical gain monolithically or through heterogeneous approaches can reduce fiber coupling losses and packaging complexity compared to discrete amplification schemes. At the same time, the incorporation of SOAs introduces system-level considerations, including thermal management, gain saturation, and the control of amplified spontaneous emission (ASE) noise.

Chapter 4 of this thesis demonstrates the heterogeneous integration of InP-based SOAs onto a silicon photonics platform using micro-transfer printing, enabling the realization of a compact C-band pre-amplified receiver architecture and the experimental evaluation of its performance.

1.1.4 Common integration challenges across domains

Despite the wide variation in communication distance, system architecture, and wavelength regime, ultra-short-reach interconnect, datacom, and telecom systems share a common technological requirement: the scalable integration of low-loss photonic routing with high-performance active optoelectronic functionalities, including high-speed modulation, photodetection, and, in some cases, optical gain. Realizing such multifunctional photonic integrated circuits often requires combining complementary material platforms within a unified and scalable integration framework.

The dominant constraints and integration needs across domains are summarized in Table 1.1.

Table 1.1: Comparison of integration drivers across communication domains.

Domain	Main Constraint	Integration Need
Interconnect	Energy per bit	Co-integration with electronics
Datacom	Channel scaling	WDM + compact filtering
Telecom	Sensitivity	Integrated gain + low noise

In all cases, silicon and silicon nitride provide excellent low-loss waveguide platforms with strong CMOS compatibility and mature fabrication ecosystems. Silicon photonics additionally supports the monolithic integration of germanium photodiodes for efficient O- and C-band detection. However, both silicon and silicon nitride are indirect-bandgap materials and therefore cannot provide efficient light emission

or optical gain. Furthermore, silicon nitride lacks intrinsic optical absorption at telecom wavelengths, necessitating heterogeneous integration for photodetection.

Direct-bandgap III–V semiconductors, such as InGaAs and InP, provide efficient light emission, optical amplification, and high-performance photodetection across O-band and C-band wavelengths. Their integration onto silicon-based or silicon-nitride-based platforms therefore enables the realization of fully functional photonic integrated circuits.

Despite differences in communication scale and wavelength regime, all domains require compact, high-speed integration of low-loss photonic routing with high-performance active optoelectronic devices. This shared requirement motivates the exploration of scalable heterogeneous integration technologies, such as micro-transfer printing, which forms the central theme of this thesis and is discussed in detail in the following sections.

1.2 Photonic integration platforms

The realization of high-performance integrated optical receivers critically depends on the underlying photonic integration platform. Among the most prominent platforms are silicon photonics and silicon nitride photonics, both compatible with CMOS fabrication infrastructure.

1.2.1 Silicon photonics

Silicon photonics, typically implemented on silicon-on-insulator (SOI) substrates, has become a leading platform for integrated optical communication systems. Its success is largely driven by compatibility with CMOS fabrication infrastructure, enabling wafer-scale manufacturing and high-yield production. These advantages have enabled the development of highly integrated photonic transceivers for data center networks, metro communication systems, and emerging optical interconnect architectures.

A key feature of silicon photonics is the high refractive index contrast between silicon and silicon dioxide, which enables strong optical confinement within submicron-scale waveguides. This strong confinement allows compact passive components such as directional couplers, Mach–Zehnder interferometers, wavelength filters, and arrayed waveguide gratings to be implemented with small footprints. As a result, complex photonic integrated circuits (PICs) containing large numbers of optical components can be realized on a single chip, supporting wavelength-division

multiplexed (WDM) architectures that scale link capacity through parallel optical channels.

Silicon photonics also supports high-speed electro-optic modulation through the plasma dispersion effect in carrier-based p–n junction devices (e.g., carrier-depletion and carrier-injection modulators). This mechanism enables energy-efficient modulators operating at tens of gigabits per second and forms the basis of many commercial silicon photonics transmitters. In addition, germanium photodiodes can be monolithically integrated on silicon waveguides, enabling efficient photodetection in both the O-band and C-band communication windows.

Despite these advantages, silicon photonics also exhibits several intrinsic limitations. Silicon is an indirect-bandgap semiconductor and therefore cannot provide efficient optical gain or light emission. Consequently, active functions such as lasers and semiconductor optical amplifiers must be implemented using direct-bandgap III–V materials. Furthermore, certain applications — such as low-loss photonic routing or high-performance passive filtering — may benefit from alternative material platforms with lower propagation loss.

These limitations motivate the development of heterogeneous integration approaches that combine the scalability and manufacturability of silicon photonics with the superior optoelectronic properties of III–V semiconductors. Such integration strategies enable the realization of fully functional photonic systems incorporating light sources, amplifiers, modulators, and photodetectors on a common platform.

1.2.2 Silicon nitride photonics

Silicon nitride (SiN) photonics has emerged as an important complementary platform to silicon photonics, particularly for applications requiring ultra-low optical loss and operation across a wide wavelength range. SiN waveguides are typically formed by a silicon nitride core embedded within a silicon dioxide cladding, resulting in a dielectric waveguide structure with moderate refractive index contrast. Compared with silicon-on-insulator platforms, silicon nitride offers superior passive optical performance, including significantly lower propagation loss, wide transparency windows, and high optical power handling capability [15].

One of the most distinctive advantages of SiN photonics is the realization of ultra-low-loss waveguides and ultra-high-Q resonators. Advances in fabrication processes such as LPCVD deposition, photonic Damascene processing, and optimized annealing techniques have enabled propagation losses well below 1 dB/m in optimized structures, whereas typical SOI and InP waveguides exhibit propagation losses at the dB/cm level [16, 17]. These ultra-low-loss waveguides support high-quality

resonant devices and long optical delay lines, making SiN particularly attractive for applications such as microwave photonics, frequency comb generation, precision metrology, and optical sensing [15]. In addition, the wide transparency window of silicon nitride, extending from the visible to the mid-infrared, allows SiN photonic circuits to operate across a broad wavelength range.

Another important advantage of SiN is its high optical power handling capability. Unlike silicon waveguides, SiN does not suffer from two-photon absorption at typical telecommunication wavelengths, which enables stable operation at higher optical powers. This property is especially beneficial in nonlinear photonics applications, where strong optical fields are required to generate effects such as Kerr frequency combs and supercontinuum generation.

Despite these advantages, silicon nitride is fundamentally a passive dielectric material and lacks intrinsic electro-optic or optoelectronic functionality. Efficient optical modulation, photodetection, and optical gain therefore require integration with additional materials. As a result, SiN photonic circuits are frequently combined with silicon, III–V semiconductors, or other functional materials such as lithium niobate through hybrid or heterogeneous integration approaches in order to realize complete photonic systems.

Consequently, while silicon nitride provides an excellent low-loss photonic routing platform, the realization of fully integrated transmitters and receivers on SiN requires the incorporation of active optoelectronic components. This requirement motivates the heterogeneous integration strategies discussed in the following section.

1.3 Heterogeneous integration techniques and micro-transfer printing

Efficient optical gain and certain optoelectronic functions require direct-bandgap III–V compound semiconductors such as InP and InGaAs. While silicon photonics platforms can integrate germanium photodiodes for near-infrared detection, silicon and silicon nitride are both indirect-bandgap materials and therefore cannot provide efficient optical gain. As a result, heterogeneous integration is essential for combining passive photonic platforms with active optoelectronic devices. Over the past two decades, several heterogeneous integration strategies have been developed, including bonding-based integration, flip-chip integration, direct epitaxial growth, and micro-transfer printing (μ TP).

1.3.1 Bonding-based integration

Bonding is one of the most mature heterogeneous integration approaches and enables the permanent attachment of III–V materials onto silicon-based photonic platforms. In this approach, a III–V epitaxial layer or die is bonded onto a processed silicon photonic wafer, after which the III–V substrate is typically removed and optoelectronic devices are fabricated in the bonded layer. Bonding-based heterogeneous integration has enabled a wide range of hybrid silicon photonic devices, including lasers, semiconductor optical amplifiers, and photodetectors.

Depending on the integration scale and bonding mechanism, bonding techniques can be classified along two dimensions: bonding scale and bonding interface type.

Bonding scale: wafer-to-wafer and die-to-wafer

Wafer-to-wafer (W2W) bonding involves bonding a full III–V wafer to a silicon or silicon photonics wafer. After bonding, the III–V substrate is removed and devices are fabricated in the bonded layer. W2W bonding offers high throughput and good alignment uniformity across the wafer. However, it requires strict surface flatness and cleanliness and typically results in relatively high consumption of III–V material, since the entire III–V wafer is bonded even if only localized active regions are required.

Die-to-wafer (D2W) bonding attaches III–V dies onto selected regions of a target wafer. The dies may consist of III–V epitaxial material or partially processed device layers, which are subsequently processed after bonding. This approach improves material utilization and allows selective placement of active devices only

in predefined locations of the photonic circuit. As a result, D2W bonding provides greater design flexibility compared with W2W bonding, although it may face challenges in alignment accuracy and throughput for large-scale manufacturing.

One widely used implementation of D2W bonding is collective die-to-wafer (Co-D2W) bonding, in which singulated dies are first transferred to a carrier wafer and subsequently bonded to the target wafer in a single bonding step. A schematic illustration of the Co-D2W process is shown in Fig. 1.4. The process typically includes carrier preparation, die population on the carrier wafer, wafer bonding, and carrier separation, enabling wafer-scale heterogeneous integration while maintaining selective placement of III–V devices.

Bonding interface types

Bonding techniques can further be classified based on the bonding interface:

- **Direct (molecular) bonding:** Also referred to as fusion bonding, this technique relies on atomic-level bonding between ultra-clean and flat surfaces. It enables very thin bonding interfaces and good thermal conductivity but requires stringent surface preparation and high surface quality.
- **Adhesive bonding:** A polymer layer, such as benzocyclobutene (BCB), is used as an intermediate adhesive layer. Adhesive bonding relaxes surface roughness requirements and improves process tolerance but introduces a thicker bonding layer and reduced thermal conductivity.
- **Hybrid bonding:** Hybrid bonding combines dielectric bonding with simultaneous metal interconnect formation, enabling both mechanical attachment and electrical interconnection between bonded layers. This approach is increasingly adopted in advanced packaging and high-density heterogeneous integration.

Bonding-based approaches have enabled many early demonstrations of III–V-on-silicon lasers and photodetectors and remain widely used in silicon photonics platforms. However, these approaches typically involve bonding continuous III–V films over relatively large areas, even when only localized active regions are required.

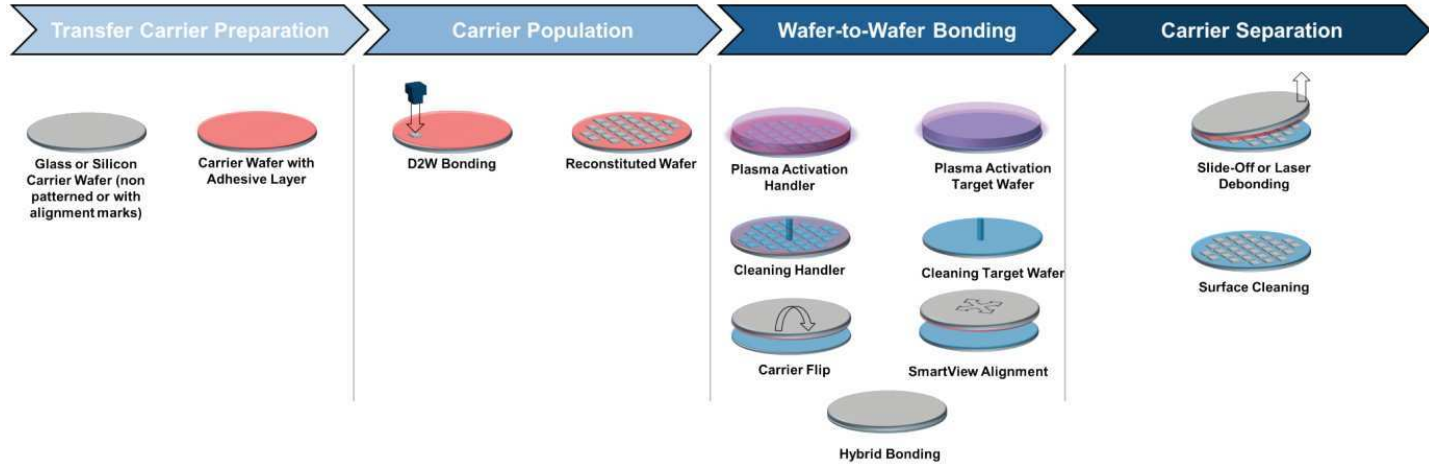


Figure 1.4: Schematic illustration of collective die-to-wafer (Co-D2W) bonding. Singulated III–V dies are first transferred to a carrier wafer and then bonded collectively to the target wafer, followed by carrier separation. Reproduced from [18].

1.3.2 Flip-chip integration

Flip-chip integration is a heterogeneous integration approach in which pre-fabricated optoelectronic devices are inverted and electrically connected to a target photonic or electronic substrate using solder bumps, metal pillars, or conductive adhesives. In contrast to bonding-based integration, where III–V material layers are transferred and processed together with the silicon platform, flip-chip integration typically combines fully processed chips from different material platforms in a packaging or assembly step.

This approach allows the independent fabrication and optimization of III–V devices and silicon-based photonic circuits. As a result, only known-good dies need to be assembled, which can improve yield and reduce material waste. Flip-chip assembly also enables short electrical interconnects and good thermal contact between the active device and the substrate, which is beneficial for high-speed and high-power optoelectronic devices.

In photonic integrated circuits, flip-chip integration is frequently used to attach III–V lasers, semiconductor optical amplifiers, or detectors onto passive silicon or silicon nitride waveguide platforms. A schematic illustration is shown in Fig. 1.5.

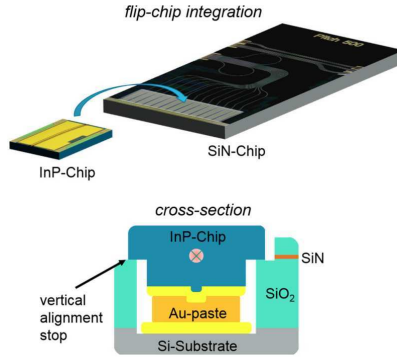


Figure 1.5: Example of hybrid flip-chip integration of an InP device onto a silicon nitride photonic chip. Reproduced from [19].

A typical implementation places the III–V chip into an etched recess on the photonic chip and uses mechanical alignment structures to simplify the positioning process. For example, hybrid integration of InP laser chips onto silicon nitride photonic circuits has been demonstrated using flip-chip bonding combined with passive mechanical alignment structures and optical feedback alignment techniques.

Despite its advantages, flip-chip integration presents several challenges. Precise optical alignment between the III–V device and the underlying waveguide is required

to achieve efficient optical coupling. In addition, optical coupling is often realized through butt-coupling or tapered mode converters, which impose strict alignment tolerances. Compared with wafer-scale bonding approaches, flip-chip integration is typically performed at the die level and therefore may offer lower throughput for large-scale manufacturing.

Nevertheless, flip-chip integration remains an important technique for hybrid photonic integration, particularly in applications where fully processed active devices must be integrated onto passive photonic platforms.

1.3.3 Direct epitaxial growth

Direct epitaxial growth aims to achieve monolithic integration by growing III–V semiconductor materials directly on silicon substrates. In contrast to bonding-based or assembly-based approaches, this technique eliminates intermediate bonding interfaces and enables the fabrication of active devices directly within a silicon photonic platform. In principle, monolithic integration offers advantages in terms of scalability, thermal management, and compatibility with high-volume CMOS manufacturing.

However, direct heteroepitaxy of III–V materials on silicon is technically challenging due to fundamental material incompatibilities. The lattice constant mismatch between typical III–V materials and silicon can exceed several percent, which leads to the formation of misfit dislocations and threading defects during crystal growth. Additionally, differences in thermal expansion coefficients between III–V compounds and silicon can introduce strain during cooling from the growth temperature, further increasing defect densities and affecting device reliability.

To mitigate these issues, several defect reduction techniques have been developed, including the use of thick buffer layers, strained superlattices, and selective-area growth structures that confine defects near the silicon interface. For example, aspect-ratio trapping (ART) structures can localize threading dislocations within narrow trenches, preventing them from propagating into the active device region.

Recent work has demonstrated significant progress toward practical monolithic integration. In particular, nano-ridge engineering (NRE) combined with selective-area epitaxy has enabled the growth of high-quality GaAs structures on large silicon wafers.

Figure 1.6 illustrates an example of a GaAs nano-ridge structure grown on a silicon wafer using selective-area epitaxy.

Using this approach, electrically driven GaAs-based laser diodes have been demon-

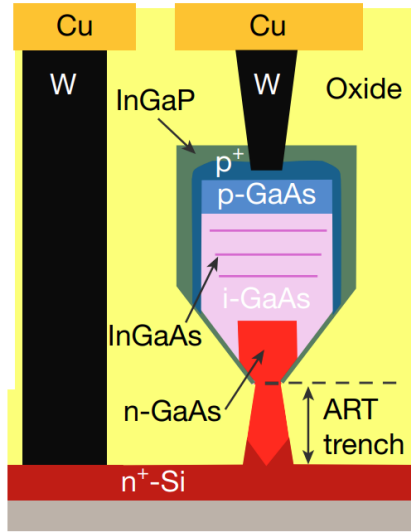


Figure 1.6: Example of monolithic III–V integration on silicon using selective-area epitaxial growth of GaAs nano-ridge structures. Reproduced from [20].

strated on 300-mm silicon wafers fabricated entirely within a CMOS pilot manufacturing line, illustrating the potential of monolithic III–V integration for scalable photonic systems [20].

Despite these advances, direct epitaxial growth remains an active research area. Achieving sufficiently low defect densities and long-term device reliability remains challenging, particularly for quantum-well lasers and other defect-sensitive optoelectronic devices. As a result, heterogeneous integration approaches such as bonding and micro-transfer printing continue to play an important role in current photonic integration platforms.

1.3.4 Micro-transfer printing

Micro-transfer printing (μ TP) is a heterogeneous integration technique that enables the deterministic placement of prefabricated device coupons or thin-film structures from a source wafer onto a target photonic platform. The process relies on elastomeric stamps, typically fabricated from polydimethylsiloxane (PDMS), to retrieve and transfer microstructures with high spatial precision. As illustrated in Fig. 1.7, arrays of prefabricated device coupons can be selectively picked up from a source wafer and transfer-printed onto predefined locations of a target photonic integrated circuit (PIC). Although laser coupons are shown as an example in the schematic, the same concept applies to a wide range of devices and thin-film materials, including photodetectors, semiconductor optical amplifiers, and functional films such as lithium niobate.

Originally developed for the transfer of discrete microscale devices, μ TP has evolved into a versatile heterogeneous integration platform capable of transferring structures ranging from micrometer-scale devices to millimeter- and centimeter-scale thin films [21]. Recent demonstrations have further extended the technique toward wafer-level transfer printing, enabling scalable integration of heterogeneous materials on large photonic wafers [22, 23].

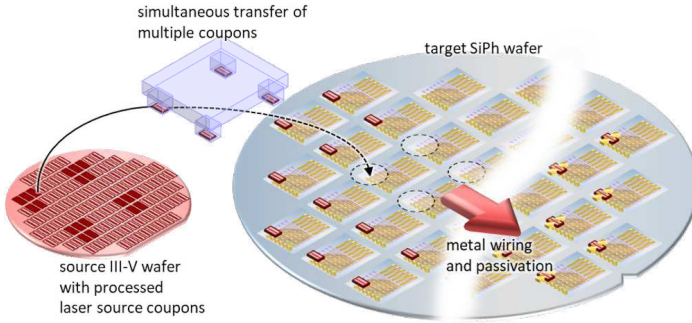


Figure 1.7: Conceptual illustration of micro-transfer printing (μ TP) for heterogeneous photonic integration. Prefabricated device coupons fabricated on a source wafer are retrieved using an elastomeric stamp and transfer-printed onto predefined locations of a target silicon photonic wafer. Although laser coupons are illustrated here as an example, the technique can be applied to a wide range of device types and thin-film materials.

For photonic integrated circuits, μ TP provides an attractive approach for integrating materials that are not natively available in silicon-based platforms. By transferring active or functional materials onto passive silicon or silicon nitride waveguide circuits, the technique enables the realization of complex photonic systems that

combine multiple material platforms within a single integrated circuit.

The basic working principle of μ TP is illustrated in Fig. 1.8. In a typical process, devices such as lasers, photodetectors, or semiconductor optical amplifiers are first fabricated on their native source wafer. A sacrificial release layer is incorporated in the epitaxial stack to enable the detachment of the devices from the substrate. After device fabrication, selective under-etching of the release layer forms suspended device coupons supported by temporary tether structures.

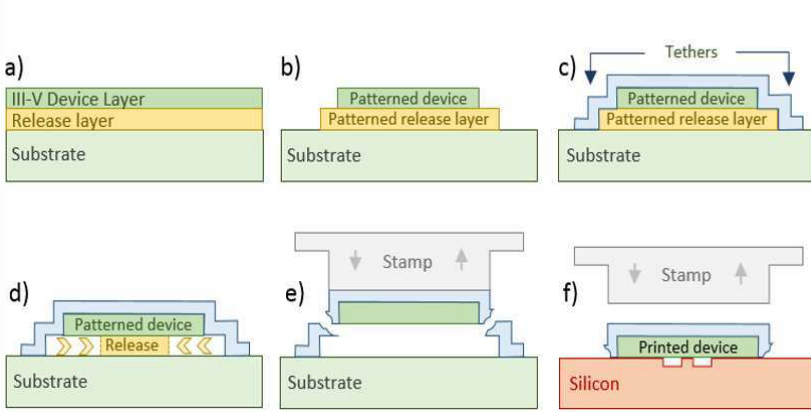


Figure 1.8: Schematic illustration of the micro-transfer printing process. (a) Epitaxial device layer grown on a substrate with a sacrificial release layer. (b) Definition of device coupons and patterned release layer. (c) Formation of suspended coupons supported by tether structures. (d) Selective release of the device coupons. (e) Pickup of the coupon using a PDMS elastomeric stamp. (f) Printing of the device onto the target silicon photonic substrate. Reproduced from [24].

A PDMS stamp is laminated onto the released devices and rapidly retracted, allowing the coupons to be picked up due to the viscoelastic adhesion of the elastomeric stamp. The devices are subsequently aligned with predefined locations on the target photonic circuit and printed by slowly retracting the stamp, which reduces the adhesion force and releases the coupons onto the target substrate. After transfer printing, additional processing steps such as adhesive bonding, planarization, and metallization are typically performed to complete the integration.

The overall μ TP integration process can be summarized as follows:

1. Fabrication of device coupons on a source wafer,
2. Definition of sacrificial release layers and tether structures,
3. Selective under-etching to release the coupons,

4. Pickup using a patterned PDMS elastomeric stamp,
5. Alignment and printing onto the target photonic platform,
6. Post-printing processing such as bonding and metallization.

Compared with conventional heterogeneous integration approaches such as wafer bonding or flip-chip assembly, μ TP offers several distinctive advantages. Since devices can be fabricated in dense arrays on the source wafer (70 μ m device pitch is a typical value), μ TP enables more efficient utilization of source materials than assembly approaches that require larger die footprints and spacing (approximately 300 μ m for flip-chip integrated devices) [24]. The transfer process can also be performed after completion of the photonic back-end-of-line (BEOL) processing, making the technique compatible with standard photonic fabrication flows [25, 26]. In addition, patterned elastomeric stamps enable the parallel transfer of multiple devices, which improves integration throughput and scalability.

Another important advantage of μ TP is its versatility in terms of transferable material systems and device dimensions. Beyond optoelectronic devices, recent work has demonstrated the transfer printing of larger thin-film structures and functional materials, including lithium niobate, magneto-optic materials [27], and nonlinear optical films [28–30]. These developments highlight the potential of μ TP as a flexible platform for multi-material photonic integration.

In this thesis, micro-transfer printing is investigated as a heterogeneous integration strategy for implementing high-performance integrated optical receivers operating in both the O-band and C-band on silicon nitride and advanced silicon photonics platforms.

1.4 Research objectives and contributions

The objective of this thesis is to investigate micro-transfer printing as a versatile heterogeneous integration strategy for realizing high-performance integrated optical receivers across multiple photonic platforms and wavelength bands.

The specific objectives are:

1. Demonstration of high-responsivity, high-speed O-band InGaAs/InP photodiodes integrated onto LPCVD silicon nitride waveguides.
2. Realization of multi-channel O-band CWDM receivers on SiN using μ TP-integrated photodiodes.

3. Integration of InP semiconductor optical amplifiers onto an advanced silicon photonics platform for C-band pre-amplified receivers.
4. Analysis of device- and system-level performance trade-offs, including responsivity, bandwidth, and noise.

The main contributions include:

- 1 A/W responsivity (95% quantum efficiency) O-band MUTC photodiodes integrated on SiN, with 37 GHz 3-dB bandwidth supporting 40 Gbit/s NRZ large-signal reception.
- Demonstration of a 4×32 Gbit/s O-band CWDM receiver on SiN.
- μ TP integration of InP SOAs on an advanced silicon photonics platform and validation of a C-band pre-amplified receiver.

Since this thesis was carried out in a collaborative research environment, the author's own contribution is clarified here. In Chapter 2, the photodiode epitaxial wafers were grown by collaborators at TU/e. In Chapter 3, the passive SiN photonic integrated circuit was designed by Laurens Bogaert and fabricated by Jasper De Witte in our group. In Chapter 4, the InP SOA coupons were fabricated by collaborators at III–V Lab and by Emadreza Soltanian in our group. The silicon photonics tape-out used in Chapter 4 was performed by Jing Zhang in our group. Except for these specific contributions, all other work presented in this thesis was performed by the author, including device and system design, simulations, layout preparation where applicable, micro-transfer-printing process development and/or implementation, experimental characterization, data analysis, interpretation of the results, and thesis writing.

The novelty of this thesis is demonstrated at both the device and receiver-system levels. First, since SiN is an intrinsically passive platform, the μ TP integration of InGaAs/InP photodiodes enables high-performance active receiver functionality on SiN. The demonstrated O-band MUTC photodiodes combine high responsivity with competitive high-speed operation compared with reported SiN-integrated photodetectors.

Second, this work extends μ TP-based photodiode integration from individual devices to a 4×32 Gbit/s O-band CWDM receiver on SiN. This bridges the gap between passive SiN wavelength-selective circuits and receiver-level WDM implementations, which are typically realized on silicon platforms using integrated Ge photodiodes or APDs.

Third, this thesis demonstrates μ TP integration of InP SOAs on an advanced silicon photonics platform, enabling a C-band pre-amplified receiver concept that combines III–V optical gain with the scalability of silicon photonics. Detailed comparisons with representative state-of-the-art works are provided in the corresponding chapters.

Collectively, this work establishes micro-transfer printing as a scalable and platform-agnostic heterogeneous integration approach for next-generation photonic integrated receivers.

1.5 Thesis organization

The remainder of this thesis is organized as follows:

Chapter 2 presents the design, fabrication, and characterization of O-band InGaAs/InP photodiodes integrated onto LPCVD silicon nitride photonic circuits using micro-transfer printing.

Chapter 3 demonstrates a 4×32 Gbit/s O-band CWDM receiver implemented on silicon nitride with μ TP-integrated photodiodes.

Chapter 4 describes the integration of InP semiconductor optical amplifiers onto an advanced silicon photonics platform and the experimental validation of a C-band pre-amplified receiver architecture.

Chapter 5 summarizes the conclusions of this work and outlines future research directions.

1.6 Publications

1.6.1 Publications in international journals

1. **S. Qin**, L. Bogaert, J. De Witte, S. Reniers, Y. Jiao, J. Zhang, J. Bauwelinck, G. Roelkens, “O-band 4×32 Gbit/s CWDM receiver on a silicon nitride photonic platform with micro-transfer printed InGaAs/InP photodiodes”, *Optics Express*, 34(8), pp. 15532–15542 (2026).
2. **S. Qin**, L. Bogaert, S. Reniers, Y. Jiao, J. Zhang, J. Bauwelinck, G. Roelkens, “Micro-transfer printing of O-band InGaAs/InP photodiodes on a silicon nitride photonic platform”, *Optics Express*, 33(16), pp. 34153–34169 (2025).

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1.6.2 Publications in international conferences

1. **S. Qin**, E. Soltanian, J. Ramirez, D. Neel, N. Vaissiere, J. Decobert, J. Zhang, G. Roelkens, “Microtransfer printing of InP SOAs on advanced silicon photonics platform for C-band preamplified receivers”, *SPIE Photonics West*, 13371, United States, (2025).
2. Y.Chen, **S. Qin**, E. Soltanian, L. Bogaert, J. Zhang, G. Roelkens, “Heterogeneous Silicon Photonics Switch Fabric Integrated with SOAs and PDs enabled by Micro-Transfer Printing”, *IEEE Photonics Benelux Annual Symposium 2024*, Netherlands, (2024).
3. **S. Qin**, L. Bogaert, J. Zhang, G. Roelkens, “Micro-transfer printing of O-band InP-InGaAs photodiodes on a silicon nitride photonic platform”, *IEEE Silicon Photonics Conference (SiPhotonics)*, Japan, (2024).

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9. **S. Qin**, L. Bogaert, G. Roelkens, "Design of a 32Gbit/s O-band high sensitivity receiver", *IEEE Benelux Photonics Chapter - Annual Symposium 2022*, Netherlands, pp. poster 17 (2022).

2

Micro-transfer printing of O-band InGaAs/InP photodiodes on a silicon nitride photonic platform

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2.1 Introduction

Silicon nitride (SiN) has long been employed in CMOS manufacturing as a diffusion barrier and passivation layer in electronic integrated circuits (ICs) [31]. In integrated photonics, *low-pressure chemical vapor deposition (LPCVD) SiN*—the workhorse SiN variant for low-loss photonic waveguides—is increasingly viewed as a complementary platform to silicon-on-insulator (SOI) owing to its favorable optical properties. Its broad transparency window (roughly 400–4000 nm) supports applications ranging from atomic physics [32] and biophotonics [33] to LiDAR [34], telecom/datacom, and molecular spectroscopy [35]. Crucially, the negligible two-photon absorption enables watt-level on-chip power, which has been leveraged for Kerr frequency-comb formation [36–38] and supercontinuum generation [39–41]. Compared with SOI, the moderate index contrast of SiN waveguides mitigates sidewall-scattering losses; state-of-the-art propagation losses below 1 dB/m have been reported [42], improving laser noise via longer photon lifetimes [43–45].

However, the lack of native active functionality remains the primary limitation of this platform. This challenge is being addressed through hybrid and heterogeneous integration with III–V semiconductors [46–53] and lithium niobate (LiNbO₃) [54, 55], which have enabled the realization of sub-Hz-linewidth lasers [48] and electro-optic modulators with bandwidths exceeding 50 GHz [54].

Within this context, integrated PDs are equally essential. Table 2.1 summarizes recent efforts to realize photodiodes (PDs) on SiN photonic integrated circuits (PICs). Most demonstrations to date target C-band operation, including a micro-transfer printing (μ TP) integrated uni-traveling-carrier (UTC) PD with a 3-dB bandwidth of 155 GHz aimed at THz links [56], die-to-wafer bonded balanced receivers [57], and emerging graphene devices [58]. For near-visible operation—relevant to sensing, imaging, and quantum photonics—silicon PIN PDs [59] and MoSe₂/WS₂ heterojunctions [60] have been explored.

The O-band (1260–1360 nm) is particularly attractive for short-reach interconnects due to the minimal chromatic dispersion of standard single-mode fiber. Yu *et al.* demonstrated an O-band InGaAsP MUTC waveguide PD on SiN via μ TP with a 54 GHz 3-dB bandwidth; however, the employed butt-coupling resulted in a modest responsivity of 0.42 A/W at 1310 nm (40% quantum efficiency) [61]. PbS colloidal quantum-dot PDs at 1275 nm offer low-cost processing but are limited to a 1.7 ns

response (100 MHz 3-dB bandwidth), restricting high-speed applications [62].

In this chapter, we report O-band InGaAs/InP PDs integrated on an LPCVD SiN platform using μ TP. By employing an efficient waveguide-coupled geometry, we realize 1 A/W responsivity at 1310 nm (95% quantum efficiency). To enhance high-speed performance, we introduce a partially doped absorber to implement a modified UTC (MUTC) design and fabricate a strictly matched PIN reference (identical thickness, geometry, and process, but with an undoped absorber) to isolate the impact of the absorber. The MUTC device attains a 3-dB bandwidth of 37 GHz—12 GHz higher than the PIN reference with the same absorber thickness. We further demonstrate non-return-to-zero (NRZ) data reception up to 40 Gbit/s with open eyes, meeting O-band short-reach requirements for datacom and interconnects while benefiting system power through high responsivity. Finally, because μ TP is Back end of line (BEOL)-compatible [63, 64], this approach enables dense co-integration of SOAs [49], lasers [49–53], modulators [54], and PDs [56, 59] on foundry SiN platforms, providing a scalable path toward multifunctional SiN PICs.

2.2 Device concept and epitaxial layer stack design

2.2.1 MUTC absorber engineering

The PDs developed in this work were fabricated on InGaAs/InP epitaxial wafers. The epitaxial layer stack of the MUTC-type PD is presented in Table 2.2. To achieve both high responsivity and large bandwidth, a partially doped absorber composed of a 350 nm p-doped InGaAs layer (neutral region) and a 500 nm intrinsic InGaAs layer (depleted region) is employed. The carrier transit time in such a structure is jointly determined by the diffusion velocity of electrons in the neutral region and the drift velocity of holes in the depleted region. By optimizing the ratio between the p-doped and intrinsic InGaAs layers, the total transit time is effectively reduced while maintaining the same total absorber thickness and optical absorption efficiency as in a conventional PIN PD. To evaluate the specific impact of absorber-layer doping, a reference PIN PD was also fabricated, with the epitaxial layer stack as shown in Table 2.3. The main similarities and difference between the MUTC and reference PIN PDs are summarized in Table 2.4. This reference device has an identical epitaxial structure, mesa geometry, and fabrication process to the MUTC device, but features an undoped 850 nm intrinsic InGaAs absorber. Both types of PDs were integrated onto LPCVD SiN PICs using μ TP, ensuring a consistent comparison of performance under identical fabrication and integration conditions.

Table 2.1: Recent progress on PD integration on SiN PICs

PD	Wavelength (nm)	Quantum efficiency	Bandwidth (GHz)	Dark current	Ref.
III-V UTC (μ TP)	1550	24%	155	10 nA @ -1 V	[56]
InGaAs/InP PD (die-to-wafer bonding)	1550	58%	30	100 nA @ -3 V	[57]
h-BN/MoS ₂ /graphene	1550	19%	28	10 nA @ 10 V	[58]
Si PIN (μ TP)	800	30%	6	107 pA @ -3 V	[59]
MoSe ₂ /WS ₂ heterojunction	780	159% ^a	0.02	50 pA	[60]
InGaAsP MUTC (μ TP)	1310	40%	54	6 nA @ -3 V	[61]
PbS colloidal quantum dot	1275	68%	0.1	70 nA @ -1 V	[62]
InGaAs/InP MUTC (μ TP)	1310	95%	37	below 38 nA @ -2 V	This work

^aThis PD has internal gain.

Table 2.2: Epitaxial layer stack of MUTC PD

Feature	Material	Thickness (nm)	Doping level (cm^{-3})
Cap	InP	100	$p = 1 \times 10^{18}$
Contact	InGaAs	40	$p = 2 \times 10^{19}$
Band smoothing	Q1.4	10	$p = 8 \times 10^{18}$
Band smoothing	Q1.25	10	$p = 4 \times 10^{18}$
P-contact	InP	300	$p = 3 \times 10^{18}$
Band smoothing	Q1.15	10	$p = 3 \times 10^{18}$
Band smoothing	Q1.26	10	$p = 3 \times 10^{18}$
Band smoothing	Q1.46	10	$p = 3 \times 10^{18}$
Neutral absorber	InGaAs	350	$p = 3 \times 10^{18}$ (top) to 2.5×10^{17} (bottom)
Depleted absorber	InGaAs	500	n.i.d.
Band smoothing	Q1.46	10	$n = 3 \times 10^{18}$
Band smoothing	Q1.26	10	$n = 3 \times 10^{18}$
Band smoothing	Q1.15	10	$n = 3 \times 10^{18}$
N-contact	InP	300	$n = 3 \times 10^{18}$
Release	InGaAs	550	$n = 1 \times 10^{18}$
Buffer	InP	100	$n = 1 \times 10^{18}$
Substrate	InP	N.A.	n type

Table 2.3: Epitaxial layer stack of reference PIN PD

Feature	Material	Thickness (nm)	Doping level (cm^{-3})
Cap	InP	100	$p = 1 \times 10^{18}$
Contact	InGaAs	40	$p = 2 \times 10^{19}$
Band smoothing	Q1.4	10	$p = 8 \times 10^{18}$
Band smoothing	Q1.25	10	$p = 4 \times 10^{18}$
P-contact	InP	300	$p = 3 \times 10^{18}$
Band smoothing	Q1.15	10	$p = 3 \times 10^{18}$
Band smoothing	Q1.26	10	$p = 3 \times 10^{18}$
Band smoothing	Q1.46	10	$p = 3 \times 10^{18}$
Absorber	InGaAs	850	n.i.d.
Band smoothing	Q1.46	10	$n = 3 \times 10^{18}$
Band smoothing	Q1.26	10	$n = 3 \times 10^{18}$
Band smoothing	Q1.15	10	$n = 3 \times 10^{18}$
N-contact	InP	300	$n = 3 \times 10^{18}$
Release	InGaAs	550	$n = 1 \times 10^{18}$
Buffer	InP	100	$n = 1 \times 10^{18}$
Substrate	InP	N.A.	n type

Table 2.4: Comparison between MUTC and reference PIN PDs used in this work

Aspect	MUTC PD	Reference PIN PD
Absorber layer	350 nm p-doped InGaAs + 500 nm intrinsic InGaAs	850 nm intrinsic InGaAs
Total absorber thickness	850 nm	850 nm
Other epitaxial layers	Identical	Identical
Mesa geometry	Identical	Identical
Integration method	μ TP on SiN PICs	μ TP on SiN PICs
Availability	Custom-fabricated for this study	Custom-fabricated for this study
Intended role	Bandwidth-optimized design	Baseline for comparison

2.2.2 Theoretical analysis of the transit-time-limited bandwidth

The electron diffusion time in the neutral region τ_N is approximated to

$$\tau_N \simeq \frac{W_N}{v_N} \quad (2.1)$$

, and the hole drift time in the depleted region τ_D is approximated to

$$\tau_D \simeq \frac{W_D}{v_D} \quad (2.2)$$

where W_N and W_D are thicknesses of the neutral p-type InGaAs absorber and the depleted intrinsic InGaAs absorber layer respectively. v_N is the effective minority electron velocity in the neutral layer, which is determined by the electron diffusion coefficient D_e ($v_N \simeq 3D_e/W_N$). v_D is the hole drift velocity. Here, values from Ref. [65] are adopted ($D_e = 2.0 \times 10^2 \text{ cm}^2/\text{s}$, $v_D = 5.0 \times 10^6 \text{ cm/s}$). The effective carrier transit time τ_{tr} is defined by these two parts, but it is not a simple sum.

Theoretical analysis of the transit-time-limited bandwidth was performed using a charge-control model, which was investigated in Ref. [66]. By assuming a uniform carrier generation at a rate of G , τ_N and τ_D can be defined as

$$\tau_N = \frac{\Delta Q_1}{\Delta J_1} = \frac{\Delta Q_1}{q\Delta G W_N} \quad (2.3)$$

$$\tau_D = \frac{\Delta Q_2}{\Delta J_2} = \frac{\Delta Q_2}{q\Delta G W_D} \quad (2.4)$$

where ΔQ_1 and ΔQ_2 are increments of charges distributing over the device induced by carrier generation in the neutral and depletion layers, respectively. ΔJ_1 and ΔJ_2 are corresponding current increments. The effective transit time then can be expressed as

$$\tau_{tr} = \frac{\Delta Q_1 + \Delta Q_2}{\Delta J_1 + \Delta J_2} = \frac{W_N \tau_N + W_D \tau_D}{W} \simeq \frac{W_N^2/v_N + W_D^2/v_D}{W} \quad (2.5)$$

where W is the total InGaAs absorber thickness. The transit-time bandwidth then is given by

$$BW_{tr} = \frac{0.445}{\tau_{tr}} \quad (2.6)$$

The calculation of the transit-time bandwidth as a function of the ratio of p-InGaAs layer when considering a total absorber thickness of 850 nm is shown in Fig. 2.1. For the MUTC design used in this study, where the p-doped layer constitutes 40% of the total 850 nm absorber, the theoretical transit-time-limited bandwidth reaches 65 GHz. In contrast, the fully intrinsic absorber of the reference PIN PD corresponds

to a bandwidth of about 25 GHz. These results indicate that partial absorber doping can substantially enhance the intrinsic speed limit of the device by reducing carrier transit time, thereby enabling higher-frequency operation without compromising optical absorption.

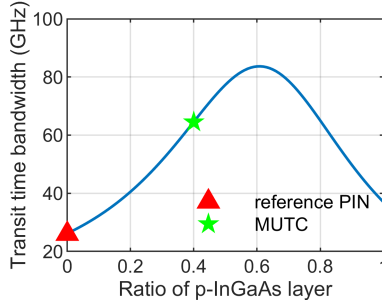


Figure 2.1: Calculated transit time bandwidth for an epitaxial layer stack with 850 nm total absorber layer as a function of the ratio of the p-InGaAs layer to total absorber layer thickness.

2.3 SiN photonic circuits design

2.3.1 LPCVD SiN stripe waveguide

SiN thin films for optical waveguides are typically deposited using either low-pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD). While PECVD SiN offers better CMOS compatibility owing to its low deposition temperature, the incorporation of hydrogen-related bonds leads to higher optical absorption, particularly at C-band wavelengths. In contrast, LPCVD forms a high-quality SiN film with minimal hydrogen bonds after post-annealing at around 1000 °C, resulting in significantly lower propagation loss. At O-band wavelengths, the absorption associated with hydrogen bonds is less pronounced; however, LPCVD SiN still exhibits lower loss compared to PECVD SiN. For instance, the propagation losses of 400 nm-thick LPCVD and PECVD SiN waveguides at 1270 nm were reported as 0.32 dB/cm and 0.45 dB/cm, respectively [67]. In this work, the passive photonic circuits were fabricated on an LPCVD SiN wafer.

Commercial SiN wafers were used for the fabrication of passive photonic circuits. Each wafer consists of a 300-nm-thick SiN layer on top of a 3.3- μ m-thick buried oxide layer. The cross section of the SiN strip waveguide used in this study is shown

in Fig. 2.2(a). The waveguide width is $1.1\ \mu\text{m}$, and a $2\text{-}\mu\text{m}$ -thick benzocyclobutene (BCB) layer is employed as the upper cladding. The simulated electric field intensity profile of the fundamental TE mode at a wavelength of $1310\ \text{nm}$ is shown in Fig. 2.2(b).

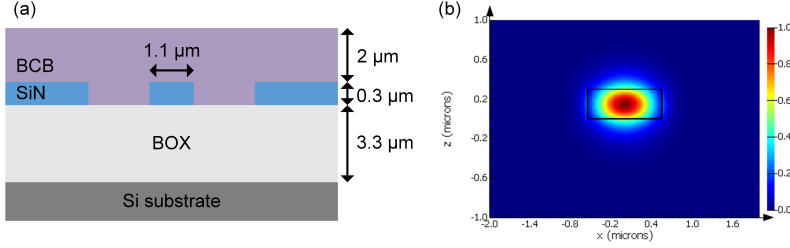


Figure 2.2: Waveguide structure of the passive SiN PICs. (a) Cross section of the SiN strip waveguide. (b) Simulated electric field intensity of the fundamental TE mode at a wavelength of $1310\ \text{nm}$.

The dispersion curves of the SiN waveguide were obtained by calculating the effective index of the TE_0 , TM_0 , and TE_1 modes as a function of the waveguide width, as shown in Fig. 2.3. For TE polarization, the SiN strip waveguide exhibits single-mode operation when the width is below $1.1\ \mu\text{m}$. For the $1.1\text{-}\mu\text{m}$ -wide SiN waveguide used in this work, the effective index of the fundamental TE mode equals to 1.66.

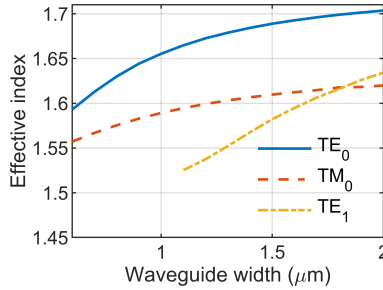


Figure 2.3: Dispersion diagram of the SiN strip waveguide at a wavelength of $1310\ \text{nm}$. The calculated effective indices of the TE_0 , TM_0 , and TE_1 modes are shown.

2.3.2 Waveguide-to-PD coupling design

A waveguide-coupled device structure is employed in this work to enable efficient optical coupling between the SiN waveguide and the III–V PD. As illustrated in

Fig. 2.4, the III–V PD coupon is integrated onto a strip SiN waveguide (300 nm SiN layer thickness, 1.1 μm waveguide width), supported by the SiN layer outside the etched trenches. The 850 nm thick InGaAs absorber is patterned into a 6 μm -wide mesa to provide sufficient alignment tolerance during μTP . The PD is passivated by a PECVD SiN layer and further encapsulated with a 2 μm -thick BCB layer serving as the upper cladding. Metal electrodes are deposited on the top and both sides of the mesa, forming the anode and cathode contacts. The InP n-contact layer and the BCB bonding layer between the InGaAs absorber and the SiN waveguide have thicknesses of 300 nm and approximately 30 nm, respectively, both sufficiently thin to avoid significant degradation of optical absorption.

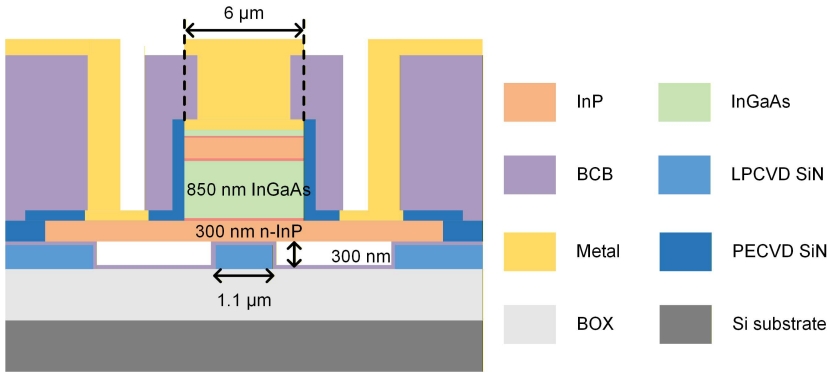


Figure 2.4: Schematic of the waveguide-coupled PD structure.

Figure 2.5(a) shows the simulated optical power distribution of the fundamental TE mode launched into a PD with a 10 μm -long mesa. The optical power is evanescently coupled from the SiN waveguide into the PD mesa and is almost completely absorbed within the first 5 μm of propagation. Figure 2.5(b) summarizes the simulated absorption efficiency as a function of mesa length. As the mesa length increases from 11 μm to 25 μm , the absorption efficiency improves from 87% to 97%. This efficient coupling scheme enables high responsivity in the fabricated PDs. Although increasing the mesa length provides a few-percent improvement in absorption efficiency, it also increases the junction capacitance due to the larger device area. Therefore, simply extending the mesa is not necessarily beneficial for high-speed operation. A higher absorption efficiency could instead be pursued by optimizing the mesa geometry, for example by using a narrower mesa to partially compensate for the capacitance increase.

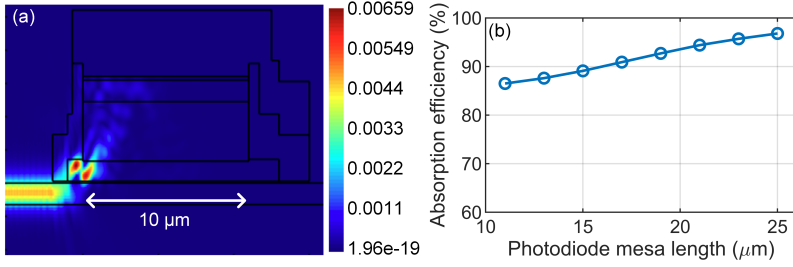


Figure 2.5: Simulated waveguide-to-PD coupling. (a) Optical power distribution of the fundamental TE mode in a PD with a 10 μm mesa. (b) Simulated absorption efficiency versus mesa length.

2.3.3 Grating coupler design

Grating couplers are employed in this work to couple optical signals from an optical fiber into the SiN PICs. A fully etched, uniform SiN grating coupler is designed for fiber coupling at an incident angle of 10° . The schematic cross-section of the grating coupler is illustrated in Fig. 2.6(a). The grating comprises 24 periods with a pitch of 915 nm and a duty cycle of 57%. The corresponding GDS layout is shown in Fig. 2.6(b). The grating region has a width of 12 μm and is connected to a 200 μm -long adiabatic taper, which efficiently transfers optical power from the wide grating section into the narrow SiN waveguide with minimal loss.

The measured transmission spectrum of the SiN grating coupler is shown in Fig. 2.7. The device exhibits a coupling loss below 10 dB over the wavelength range from 1285 nm to 1340 nm. A minimum coupling loss of 7 dB is achieved at 1310 nm.

2.3.4 PIC layout design

The GDS layout of the SiN PIC is shown in Fig. 2.8(a). The PIC incorporates an 8×3 array of waveguide-coupled PDs. Alignment markers are placed at the four corners of the chip for the post-printing process. A unit cell of the PD array is illustrated in Fig. 2.8(b). Each PD is micro-transfer printed onto a SiN waveguide with a pair of grating couplers. Dedicated alignment markers for the μTP process are positioned on both sides of each PD.

Ground-signal-ground (GSG) electrodes are implemented for high-speed electrical probing. A reference waveguide is placed adjacent to each waveguide-coupled PD to enable grating coupler de-embedding during optical characterization. The SiN waveguides and grating couplers are defined by electron-beam lithography

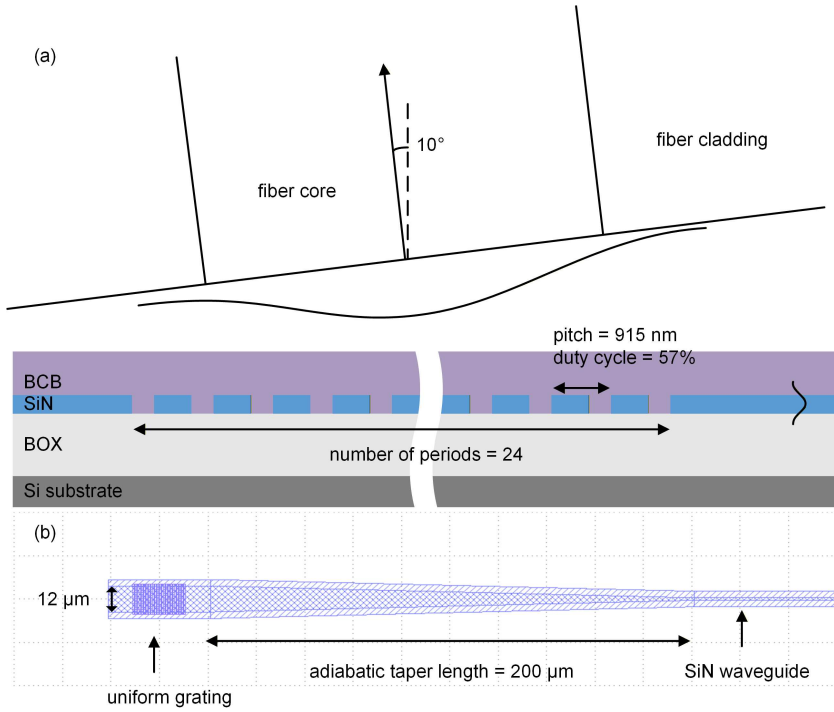


Figure 2.6: Design of a fully etched SiN uniform grating coupler operating in the O-band. (a) Schematic cross-section of the grating coupler. (b) GDS layout of the grating coupler.

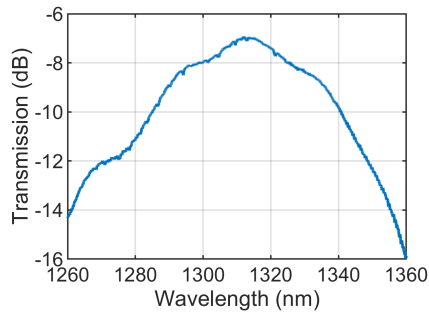


Figure 2.7: Measured transmission spectrum of the SiN grating coupler.

(EBL) using a writing field of $500\ \mu\text{m} \times 500\ \mu\text{m}$. To minimize optical loss induced by stitching errors, a taper structure is introduced where the waveguide crosses a stitching boundary. The waveguide width is adiabatically expanded from $1.1\ \mu\text{m}$ to $2.5\ \mu\text{m}$ and then reduced back to $1.1\ \mu\text{m}$ over a length of $100\ \mu\text{m}$.

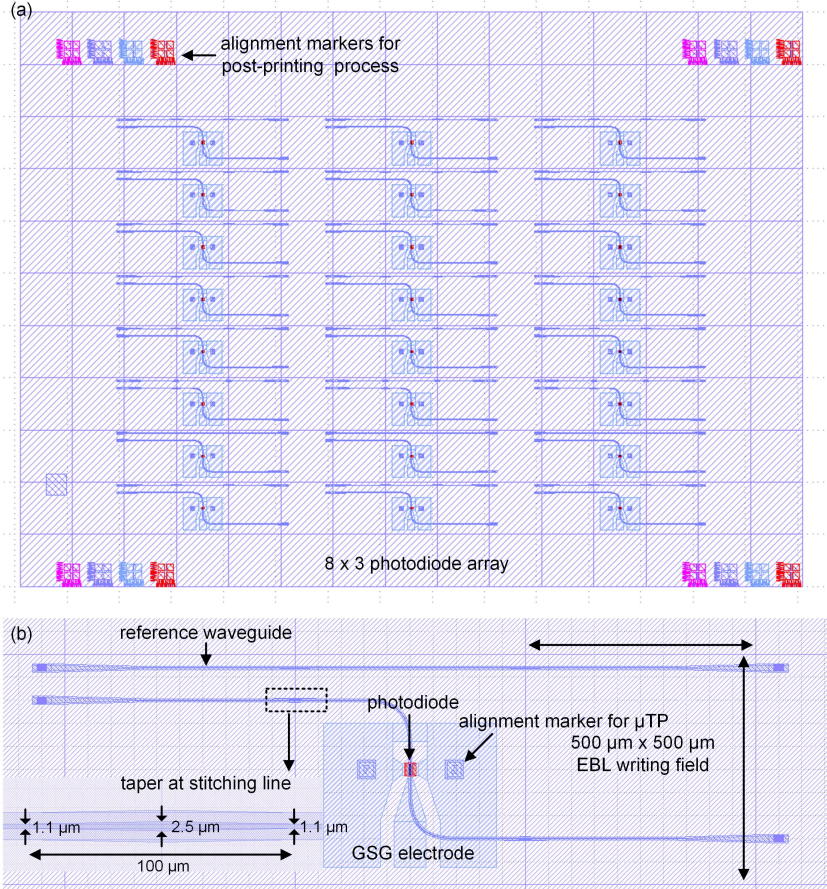


Figure 2.8: PIC layout design. (a) SiN PIC GDS layout with an 8×3 PD array. (b) Unit cell of the PD array, consisting of a waveguide-coupled PD and an adjacent reference waveguide.

2.4 Fabrication process

2.4.1 Overview of the process flow

Fig. 2.9 gives an overview of the process flow. The overall fabrication process can be divided into three parts: (1) fabrication of transfer-printable PD coupons, (2) μ TP integration, and (3) post-printing processing.

The PD mesa, as well as the anode and cathode metal layers, are first fabricated on the InGaAs/InP wafer [Fig. 2.9(a)–(d)]. A SiN layer is then deposited and patterned to provide device passivation and form tether structures that anchor the PDs to the substrate, after which the devices are released [Fig. 2.9(e)–(h)]. During the pick-up step, the PDMS stamp is laminated onto the fabricated coupons, breaking the SiN tethers and allowing the devices to be lifted from the source wafer [Fig. 2.9(i)]. Subsequently, the PDs are transfer-printed onto a pre-patterned SiN PIC [Fig. 2.9(j)–(l)]. The post-printing process includes spin-coating a BCB cladding layer, followed by metallization to form the GSG electrodes [Fig. 2.9(m)–(o)].

2.4.2 Fabrication of PD coupons

Figure 2.10 shows the layout design of the PD coupon. The GDS layout of a single PD coupon with an 11 μm mesa length is illustrated in Fig. 2.10(a). The mesa width is 6 μm . The PD incorporates an n-InP island with dimensions of 24 $\mu\text{m} \times 15 \mu\text{m}$. A SiN encapsulation layer is deposited over the PD, leaving a margin for photolithography alignment tolerance, which makes the overall coupon slightly larger than the PD itself. Four narrow tethers connect the coupon to anchor points located outside the release layer etch window. Figure 2.10(b) presents the GDS layout of a PD array, where the devices are arranged with a 50 μm pitch. Eight different mesa lengths, ranging from 11 μm to 25 μm , are implemented within the array.

We obtained the InGaAs/InP wafers from TU/e, with the anode metal already patterned. A small sample of 1 cm $\times$ 0.6 cm was cleaved from the wafer for subsequent processing. Prior to cleaving, a thin photoresist layer was spin-coated on the wafer to prevent particle contamination. The sample was then cleaned sequentially with acetone, isopropanol (IPA), deionized water, and oxygen plasma (Tepla).

The next step is defining the mesa structure using a combination of ICP dry etching and wet etching. However, during the mesa wet etching, the edge of the 40 nm InGaAs contact layer beneath the anode metal was exposed to the etchant and

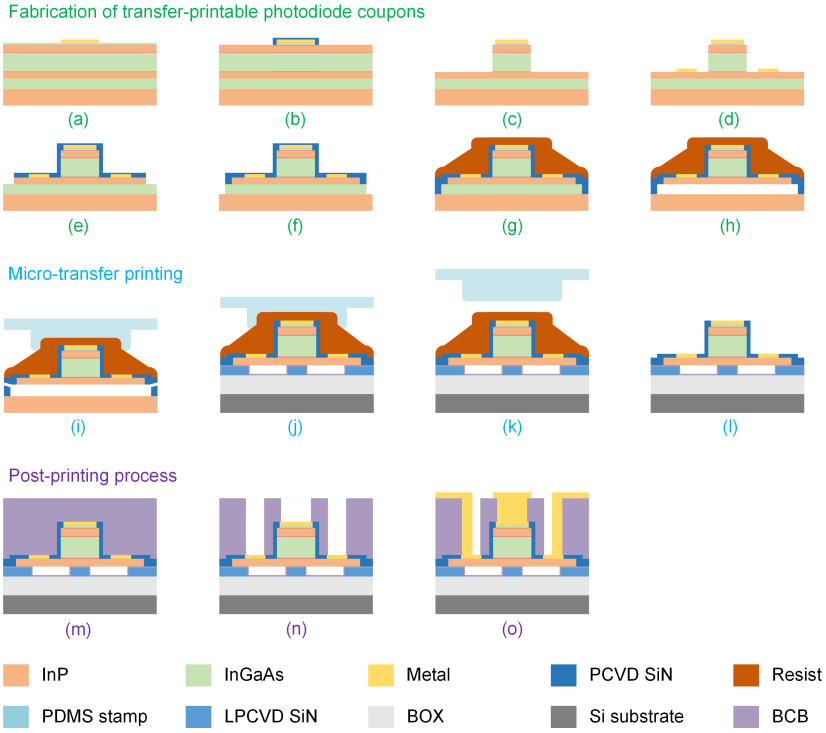


Figure 2.9: Complete process flow for O-band InGaAs/InP PDs integrated on SiN PICs, including the fabrication of transfer-printable PD coupons, μ TP integration, and post-printing processing.

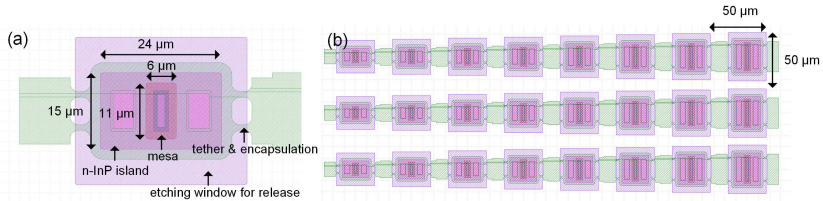


Figure 2.10: PD coupon layout design. (a) GDS layout of a single PD coupon with an 11 μ m mesa length. (b) GDS layout of a PD array with a 50 μ m pitch. A total of eight different mesa lengths were implemented, ranging from 11 μ m to 25 μ m.

partially removed, creating an air gap under the anode, as shown in Fig. 2.11(a). To solve this issue, a PECVD SiN layer was deposited to protect both the anode metal and the underlying InGaAs contact layer. The 40 nm InGaAs contact layer was first completely etched through by ICP for 2 minutes, using the anode metal as a hard mask. For this and the subsequent ICP etching steps on the InGaAs/InP layers, a CH_4/H_2 gas mixture was employed, with etch rates of approximately 30 nm/min for InGaAs and 80 nm/min for InP. After dry etching, the sample was dipped in a $\text{HCl}:\text{DI}$ water (1:20) solution for 10 seconds to remove the contamination due to the ICP dry etching. A 200 nm PECVD SiN layer was subsequently deposited to encapsulate the anode metal and seal the exposed edge of the 40 nm InGaAs contact layer, isolating it from the etchant in the following wet etching step. The resulting mesa cross-section is shown in Fig. 2.11(b).

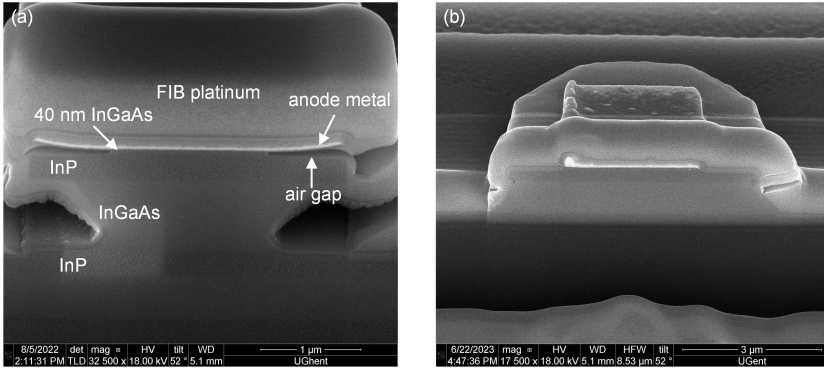


Figure 2.11: FIB cross-section images of the PD mesa. (a) Without protection for the anode metal and underlying 40 nm InGaAs, an air gap formed due to the wet etching. (b) With a SiN protective layer covering the anode metal and the 40 nm InGaAs contact layer.

The SiN layer was subsequently patterned using EBL followed by reactive ion etching (RIE). ARP6200.13 resist was used for EBL, and an Electra-92 conductive polymer coating was applied to improve charge dissipation during exposure. The RIE process employed a $\text{CF}_4/\text{SF}_6/\text{H}_2$ gas mixture, providing an etch rate of approximately 90 nm/min and offering high selectivity between SiN and the underlying InGaAs/InP layers.

The PD mesa was subsequently defined using the patterned SiN protection layer as a hard mask. Wet etching was employed with $\text{HCl}:\text{H}_3\text{PO}_4 = 1:4$ for InP and $\text{H}_2\text{O}_2:\text{H}_3\text{PO}_4:\text{DI water} = 1:1:20$ for InGaAs. In regions containing band-smoothing layers, where the wet etch rate was significantly reduced, ICP dry etching was applied. Upon reaching the final band-smoothing layer, a controlled over-etch was performed to slightly extend into the n-contact InP layer, as shown in Fig. 2.12, ensuring good contact for the subsequent cathode metallization. After mesa definition,

the SiN protection layer was removed by RIE.

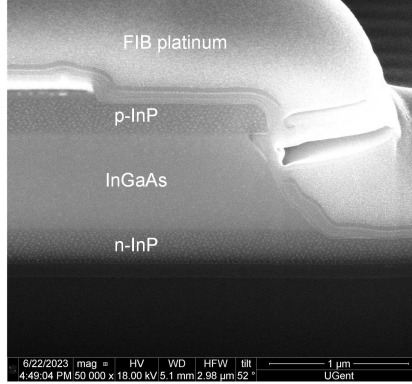


Figure 2.12: FIB cross section of the PD mesa. The n-InP layer is slightly etched.

The PD cathode metal was patterned using EBL followed by a standard lift-off process. The ARP6200.18 resist layer was used to provide sufficient thickness (900 nm) for reliable lift-off. Figure 2.13(a) shows the microscope image after EBL exposure and development. Prior to metal deposition, the sample was dipped in a diluted HCl solution ($\text{HCl:DI} = 1:20$) for 10 seconds to remove native oxides on the n-type InP surface and thereby reduce contact resistance. Metal deposition was then carried out by electron-beam evaporation, forming a 30/20/50 nm Ni/Ge/Au stack followed by a 40/200 nm Ti/Au overlay. Lift-off was performed using AR600-71 resist remover. The resulting metal pattern is shown in Fig. 2.13(b).

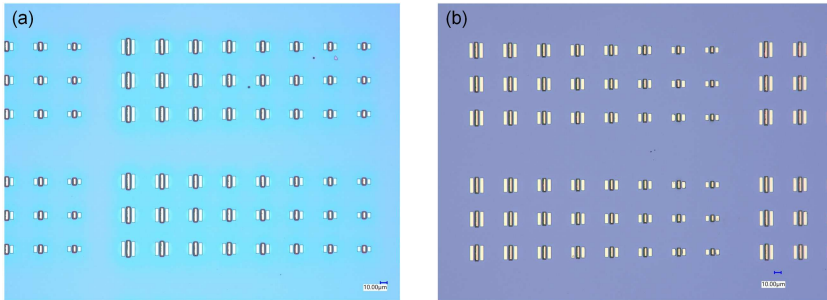


Figure 2.13: Microscope images of the cathode metal patterning process. (a) After EBL development. (b) After metal lift-off.

The sample then underwent a mesa surface cleaning procedure using diluted chemical etchants. It was sequentially dipped in $\text{H}_2\text{O}_2:\text{H}_3\text{PO}_4:\text{DI} = 1:1:20$ for 10 seconds and $\text{HCl:DI} = 1:20$ for 10 seconds to remove surface residues from the InGaAs/InP mesa sidewalls and top surface. A 300 nm PECVD SiN layer was subsequently

deposited for device passivation. During sample loading into the PECVD chamber, the chamber was maintained at room temperature to minimize oxidation of the cleaned mesa surface.

The passivation SiN layer was patterned using photolithography followed by RIE dry etching, and subsequently served as a hard mask for etching the n-InP layer. An initial ICP dry etching was performed for 160 s, removing approximately 170 nm of n-InP to reduce the duration of the subsequent wet etching and mitigate excessive lateral undercut. The sample was then immersed in an InP wet etchant ($\text{HCl} : \text{H}_3\text{PO}_4 = 1 : 4$) for 20 s to precisely stop the etching at the InGaAs release layer. A microscope image of the sample after the n-InP patterning is shown in Fig. 2.14. At this stage, the PDs have been fully defined on the III–V source wafer and are mutually isolated.

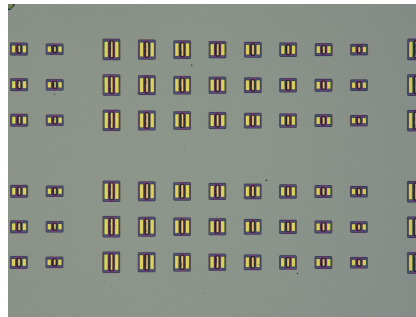


Figure 2.14: Microscope image of the sample after the n-InP layer patterning.

To pattern the InGaAs release layer, a 200 nm PECVD SiN film was deposited, patterned via photolithography, and etched by RIE to form a hard mask for the subsequent InGaAs etch. An ICP dry etch with a duration of 15 min was then performed to etch through the 550 nm InGaAs release layer and slightly into the underlying InP substrate. A microscope image of the sample after the release-layer patterning is shown in Fig. 2.15.

The SiN layer on the PDs was then partially thinned using RIE, followed by the deposition of a 700 nm SiN encapsulation layer. Contact via openings and SiN tether structures were defined in the same photolithography and RIE dry etching steps. A microscope image of the sample after this step is shown in Fig. 2.16.

Prior to release, a 3.5 μm -thick TI 35E photoresist layer was spin-coated and patterned to planarize the surface and protect the PDs during the subsequent release process. The release was carried out by immersing the sample in an aqueous FeCl_3 solution at 5 $^\circ\text{C}$ for 1 h, selectively etching the underlying InGaAs release layer. As a result, the PD coupons became suspended while remaining connected to the InP

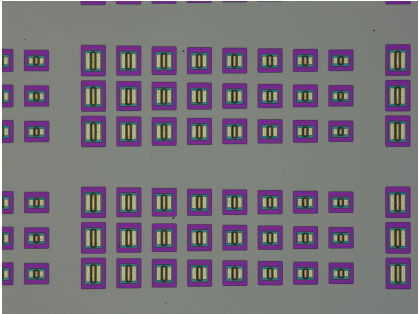


Figure 2.15: Microscope image of the sample after the release-layer patterning.

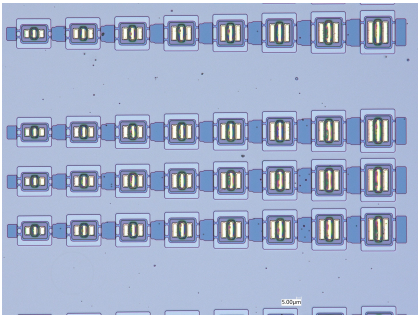


Figure 2.16: Microscope image of the sample after tether patterning and contact via opening.

substrate through SiN tethers. Figures 2.17(a) and 2.17(b) show optical microscope images of the sample before and after release, respectively. Following the release, the SiN tethers and encapsulation appeared uniform pink rather than the original blue, indicating successful removal of the sacrificial InGaAs layer underneath.

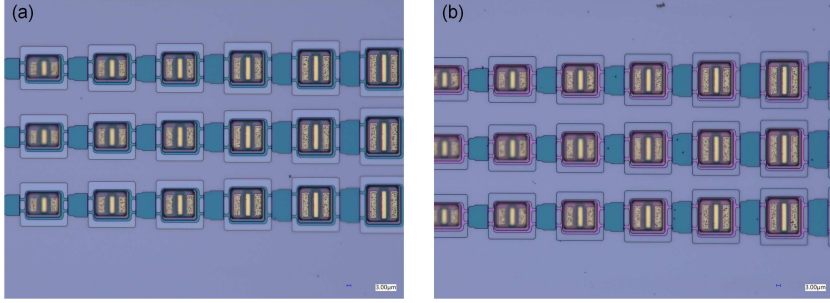


Figure 2.17: Microscope images of the sample (a) before release and (b) after release.

Among the fabrication steps, the coupon release process is considered particularly critical because it directly affects the coupon yield and printability. After the sacrificial layer is selectively removed, the coupon is undercut and remains mechanically connected to the donor substrate only through narrow tether structures. The tether geometry must provide sufficient mechanical robustness during processing while still allowing reliable fracture during micro-transfer printing. Improper tether design, non-uniform release etching, excessive mechanical disturbance, or residual stress in the epitaxial layers may cause coupon collapse or premature coupon detachment. Careful optimization of the release structure and process conditions is therefore essential for obtaining intact and printable coupons.

2.4.3 Micro-transfer printing

The second phase involves the μ TP process. A passive SiN target PIC was first fabricated using EBL and RIE dry etching on a 300-nm-thick LPCVD SiN platform. A 100 nm DVS-BCB adhesive layer was then spin-coated onto the target sample, which was reduced to approximately 30 nm after printing. The sample was then pre-baked to reflow the BCB, with the temperature ramped up to 150 °C.

Next, both the SiN PIC target and the PD coupon source were loaded onto an X-Celeprint μ TP-100 system. A PDMS stamp was used for transfer printing, providing tunable adhesion via control of the retrieval velocity. When laminating the PDMS stamp to the PD coupon and pulling-back, the SiN tethers ruptured, allowing the coupon to be successfully picked up by the stamp. The PD coupon was then aligned to the SiN waveguide on the target chip under a microscope and

printed onto the surface. By lowering the stamp lifting speed, the adhesion was reduced, enabling the coupon to release from the stamp and remain accurately positioned on the SiN target.

After the μ TP process, the photoresist on top of the PD was removed using a soft oxygen plasma recipe in an RIE system. The sample was then placed into an oven to cure the BCB at 270 °C. A microscope image of a printed PD positioned on top of a SiN waveguide is shown in Fig. 2.18.

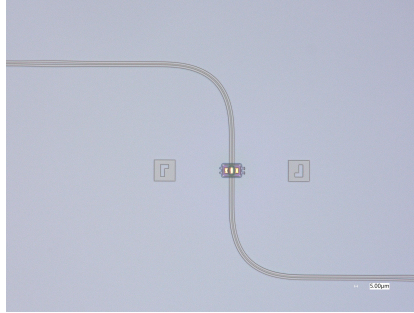


Figure 2.18: Microscope image of a PD printed on top of a SiN waveguide.

2.4.4 Post-printing process

Several post-printing processing steps were required before the PDs could be characterized. A 2 μ m-thick DVS-BCB cladding layer was spin-coated and cured at 270 °C, followed by via formation above the anode and cathode electrodes using photolithography and RIE. During photolithography, TI 35E photoresist was spin-coated at 3000 rpm to produce a sufficiently thick resist layer for the subsequent RIE etch. After development, a reflow step at 145 °C for 15 s was performed to form a ramp, which is subsequently transferred to the BCB layer by RIE, facilitating metal step coverage in later processing. A microscope image of a printed PD after via opening on the anode and cathode electrodes is shown in Fig. 2.19.

Finally, a 40 nm / 800 nm Ti/Au metal stack was deposited and used a standard lift-off process to form the probing electrodes, thereby completing the device fabrication. Figure 2.20 shows a microscope image of the resulting waveguide-coupled PD.

A high qualitative yield was observed for the PD transfer-printing process, with nearly all selected coupons being successfully picked up and printed. The occasional failures observed in the completed devices were mainly associated with subsequent post-printing fabrication steps. However, the yield was not systematically quantified in this work.

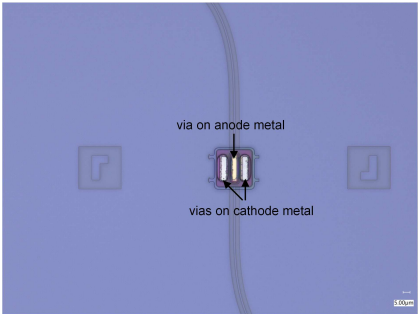


Figure 2.19: Microscope image of a printed PD after via opening.

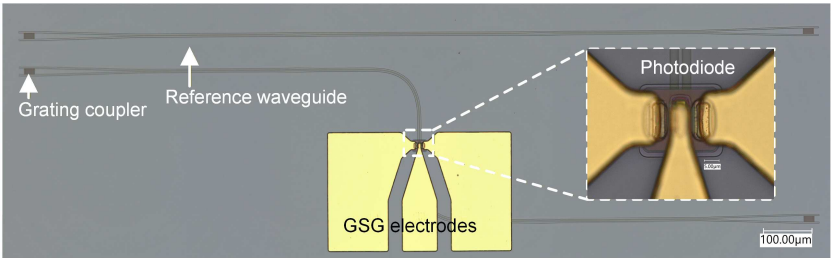


Figure 2.20: Microscope image of the fabricated waveguide-coupled PD. The inset provides a zoomed-in view of the PD region.

2.5 Characterization and discussion

2.5.1 Electrical properties

The current-voltage characteristics of the MUTC PDs with varying mesa lengths were measured in the dark, as shown in Fig. 2.21. At a bias voltage of -2 V, the dark current ranges from 11 to 38 nA. As the PD mesa length increases, the dark current increases.

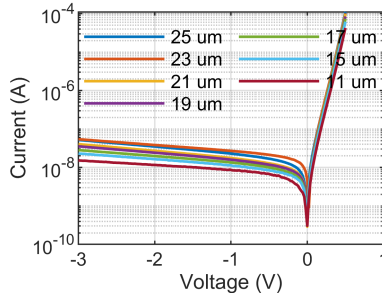


Figure 2.21: The MUTC PD current-voltage characteristics in the dark for different device mesa lengths.

The series resistance and junction capacitance of the PDs were extracted by fitting the S_{11} parameter using an equivalent circuit model as shown in Fig. 2.22. This model is based on established methods reported in Refs. [61, 68], and includes contributions from the PD itself, GSG pads, substrate effects, and the load. These four components were identified as the dominant contributors through a process of iterative fitting, in which elements were introduced or omitted to assess their impact on fitting accuracy. The final model configuration yielded satisfactory agreement between fitting and measurement, allowing other minor parasitic elements to be safely neglected. The substrate branch is placed on the right-hand side of GSG pads to represent the dominant substrate coupling underneath the relatively large RF pads.

The S_{11} parameter measurement was carried out using a vector network analyzer (VNA, R&S ZNB) up to 43.5 GHz. To ensure accurate characterization of the device under test (DUT), open-short-match (OSM) de-embedding was applied using a CS-5 calibration substrate. This procedure calibrated and removed the parasitic effects of the GSG RF probe (T40A-GSG0100), and the RF cable via one-port calibration. An example of the fitting for a MUTC PD with a length of 17 μm at a bias voltage of -2 V is presented in Fig. 2.23. This PD was used in the high-speed signal reception experiment.

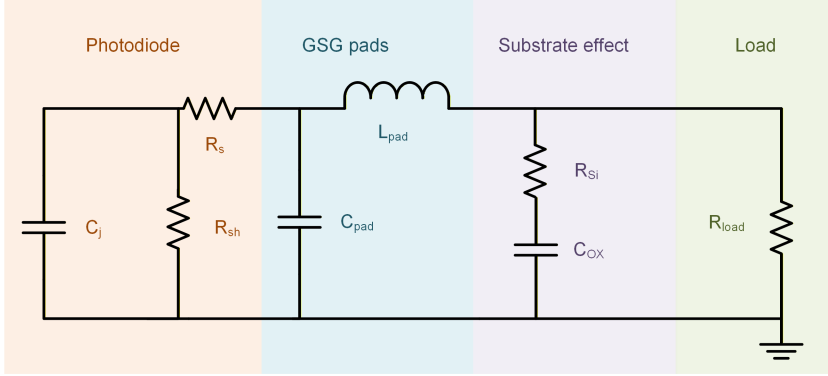


Figure 2.22: Equivalent circuit model of the waveguide-coupled PDs for S_{11} fitting (C_j : junction capacitance, R_{sh} : shunt resistance, R_s : series resistance, C_{pad} : capacitance of the GSG pads, L_{pad} : inductance of the GSG pads, R_{Si} : substrate resistance, C_{OX} : capacitance of the buried oxide, R_{load} : 50Ω load resistance).

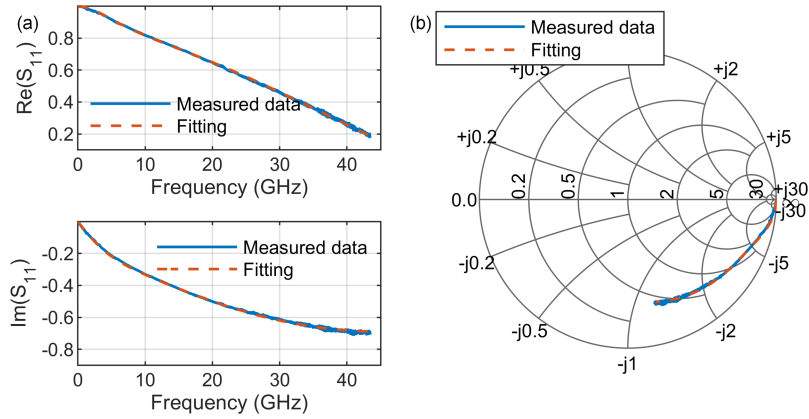


Figure 2.23: Measured and fitted S_{11} parameter for a MUTC PD with a mesa length of $17 \mu\text{m}$ at a bias voltage of -2 V . (a) Real and imaginary parts of S_{11} . (b) Smith chart.

When operated at a bias voltage of -2 V, the junction capacitance and series resistance of the MUTC PDs range from 15 to 37 fF and 90 to 41 Ω , respectively, as the PD mesa length increases from 11 to 25 μm , as shown in Fig. 2.24(a) and (b). The unit capacitance is $0.24 \text{ fF}/\mu\text{m}^2$, consistent with the expected value for a 500 nm-thick InGaAs depleted absorber. The series resistance is relatively high but can be further optimized through improved metal–semiconductor contact processing. Compared with reference PIN PDs, the MUTC PDs exhibit a higher junction capacitance but a lower series resistance. This difference is attributed to the thinner intrinsic InGaAs layer in the absorber.

A further rapid thermal annealing (RTA) step at 400°C for 15 s was performed to reduce the series resistance. The impedance characteristics, including the junction capacitance and series resistance, are shown in Fig. 2.24(c) and (d), respectively. The junction capacitance after RTA remains consistent with that before RTA. The series resistance is reduced, particularly for shorter PD mesa lengths, for both MUTC and PIN PDs. After annealing, the series resistance ranges from 60 to 40 Ω for MUTC PDs and from 95 to 50 Ω for PIN PDs.

The extracted capacitance of the GSG pads (C_{pad}) is shown in Fig. 2.25, ranging from 20 to 28 fF for MUTC PDs and 20 to 23 fF for the reference PIN PDs. Other parameters exhibit minimal variation between devices. The inductance of the GSG pads (L_{pad}) is approximately 50 pH, while the capacitance of the buried oxide (C_{OX}) and the substrate resistance (R_{Si}) are around 40 fF and 500 Ω , respectively. For parasitic extraction, each PD is analyzed independently.

2.5.2 Responsivity

Responsivity measurements were conducted on both MUTC and reference PIN PDs of varying lengths at a wavelength of 1310 nm under a bias voltage of -2 V. The input optical power was calibrated by accounting for the loss of the grating coupler, which was measured on the reference waveguides. The responsivity results are presented in Fig. 2.26(a). At 1310 nm, the responsivity remains approximately 1 A/W as the mesa length increases from 11 to 25 μm for both MUTC and reference PIN PDs, which is consistent with the simulation result. A slight difference between the measured and simulated responsivity can be attributed to the calibration inaccuracy of the optical power, caused by variations in coupling efficiency between the grating couplers. The corresponding quantum efficiency is 95%, which is a result of the effective waveguide coupling structure. Figure 2.26(b) shows the photo-current of a 17 μm MUTC PD as a function of the on-chip input optical power, which shows good linearity.

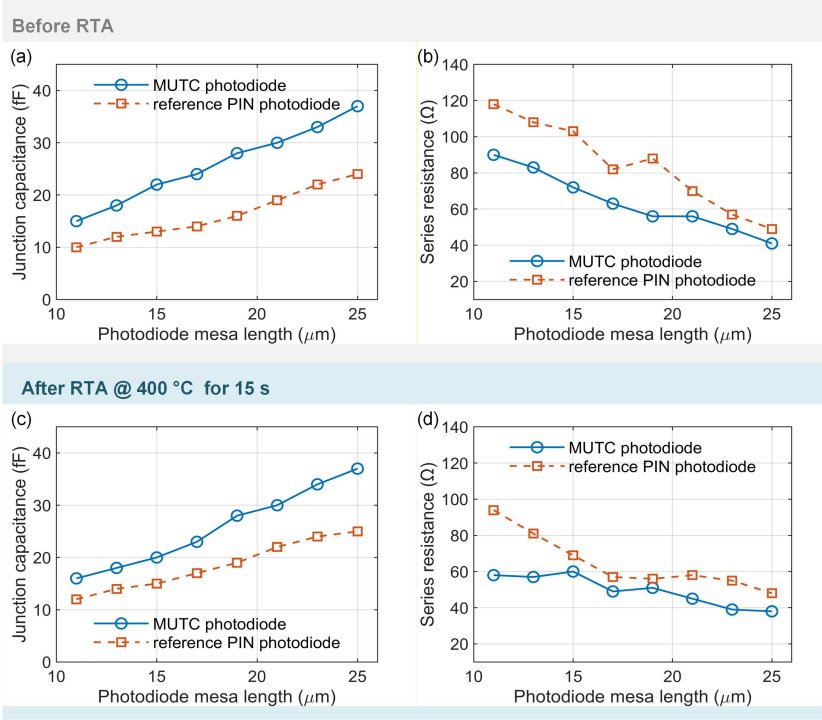


Figure 2.24: Impedance characteristics of MUTC PDs with mesa lengths ranging from 11 to 25 μm at a bias voltage of -2 V, compared with a reference PIN PD. (a) Junction capacitance before rapid thermal annealing (RTA). (b) Series resistance before RTA. (c) Junction capacitance after RTA at 400 °C for 15 s. (d) Series resistance after RTA at 400 °C for 15 s.

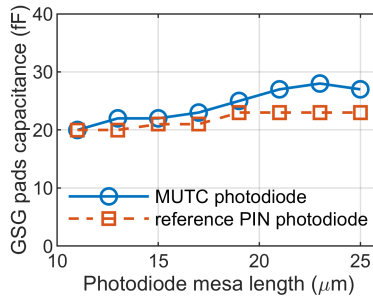


Figure 2.25: GSG pads $C(C_{\text{pad}})$ of the MUTC PDs with mesa length from 11 to 25 μm when operating at -2 V bias voltage, compared with the reference PIN PD.

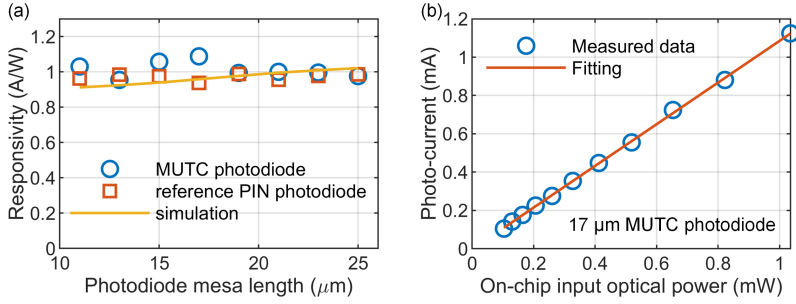


Figure 2.26: Responsivity characterization results at a wavelength of 1310 nm and a bias voltage of -2 V. (a) Responsivity of PDs with mesa lengths ranging from 11 to 25 μm , compared with the simulation result. (b) Photo-current of a 17 μm MUTC PD as a function of the on-chip input optical power.

2.5.3 3-dB bandwidth

The bandwidth performance of the PDs was evaluated through small-signal S_{21} characterization using the experimental setup shown in Fig. 2.27. The measurement system consists of an O-band tunable laser (TSL510-1310), two polarization controllers (PC), an O-band 40 Gbit/s Mach-Zehnder modulator (MZM, MX1300-LN-40), a 43.5 GHz VNA (R&S ZNB), a GSG probe (T40A-GSG0100), and a source meter (Keithley 2400). The 1310 nm laser is modulated by the MZM and subsequently received by the PD under test. The MZM is connected to Port 1 of the VNA, while the PD is connected to Port 2 via the GSG probe. The source meter is connected to the bias port of the VNA to supply a -2 V bias voltage. During calibration, the losses of the K-type cables were de-embedded using a ROHDE & SCHWARZ ZN-Z129E calibration kit. The electro-optic (EO) response of the MZM was characterized using a 50 GHz PD (XPDV2120R), and the insertion loss of the RF probe was accounted for using datasheet values. Both the modulator response and the RF probe loss were removed from the final S_{21} calculation.

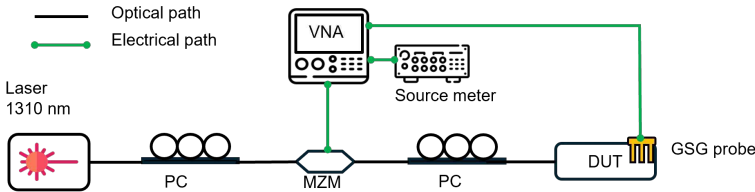


Figure 2.27: Setup for the small-signal S_{21} characterization.

The normalized S_{21} response of a 17 μm -long MUTC PD is shown in Fig. 2.28(a).

The measured S_{21} trace exhibits noticeable noise, primarily due to the low RF output power of the PD. This originates from the limited optical input power, which results from significant insertion losses in the grating coupler and modulator, as no optical amplifiers were used. To ensure a fair comparison, the DC photocurrent was maintained at 0.1 mA by adjusting the input optical power. In addition, operating the modulator in the small-signal regime further reduced the modulation of the photocurrent, leading to a weak RF output signal and a correspondingly noisy S_{21} response.

After smoothing, a 3-dB bandwidth of 32 GHz was extracted, which is 12 GHz higher than that of the reference PIN PD with the same length. This result confirms the bandwidth advantage of the MUTC epitaxial layer structure.

Figure 2.28(b) summarizes the extracted 3-dB bandwidths of the MUTC PDs and the reference PIN PDs with mesa lengths ranging from 11 to 25 μm . For the MUTC devices, the measured bandwidths are significantly lower than the theoretically estimated transit-time-limited bandwidth of the MUTC epitaxial stack (65 GHz), indicating that the device performance is primarily limited by the RC time constant. In contrast, the bandwidths of the reference PIN PDs remain consistently around 20 GHz, close to the 25 GHz transit-time-limited bandwidth of the PIN epitaxial stack, confirming that these devices operate in a transit-time-limited regime.

Figures 2.28(c) and (d) show the measured normalized S_{21} response and the extracted 3-dB bandwidth after RTA. For MUTC PDs with shorter mesa lengths, an improvement in bandwidth is observed due to the reduction in series resistance. The 11 μm -long MUTC PD exhibits the highest 3-dB bandwidth of 37 GHz.

Fig. 2.29 presents the fitted normalized S_{21} frequency responses of the 19- μm -long MUTC photodiode under different reverse-bias voltages. A clear increase in bandwidth is observed as the reverse bias is raised. The extracted 3-dB bandwidth increases from 14.33 GHz at 0 V to 25.27 GHz at -1 V, 30.76 GHz at -2 V, and 32.32 GHz at -3 V. This improvement is mainly attributed to the enhanced electric field in the depletion region at higher reverse bias, which promotes faster carrier collection and reduces the carrier transit time. The smaller bandwidth increase from -2 V to -3 V indicates that the device response gradually approaches a bias-limited saturation regime.

Although the MUTC structure provides a much higher intrinsic carrier-transit-time bandwidth than the reference PIN photodiode, the measured bandwidth of the fabricated devices is also affected by the RC constant. Therefore, the final 3-dB bandwidth is determined by the combined effect of carrier transport and the RC response of the photodiode.

The overall bandwidth of the photodiode can be estimated by combining the transit-

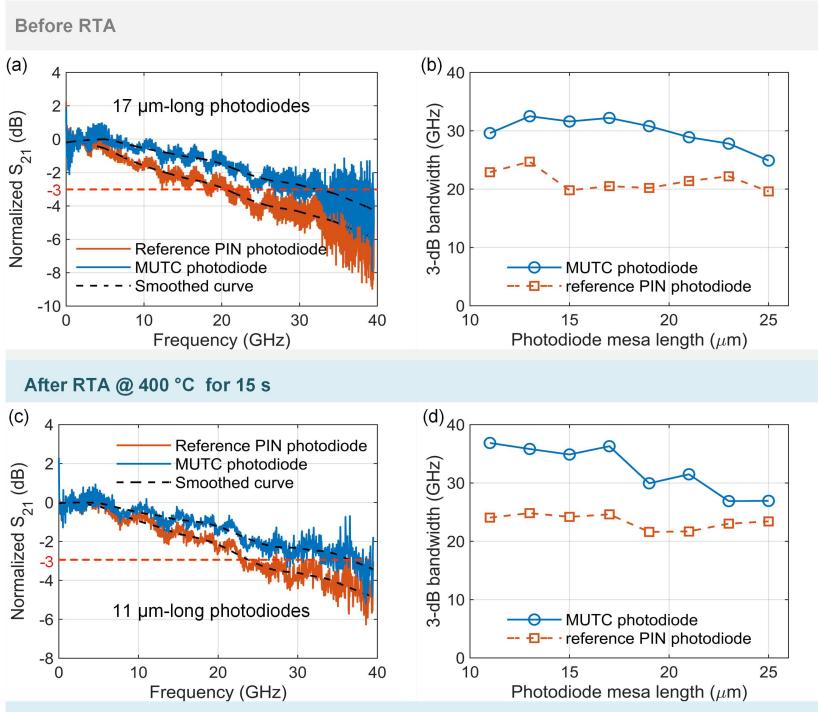


Figure 2.28: Measured frequency response and bandwidth performance of MUTC PDs compared with reference PIN PDs. (a) Measured normalized S_{21} response of a 17 μm -long MUTC PD at a bias voltage of -2 V, compared with a reference PIN PD of the same length before rapid thermal annealing (RTA). The dashed line indicates the smoothed response. (b) Extracted 3-dB bandwidth as a function of PD mesa length (11–25 μm) before RTA. (c) Measured normalized S_{21} response of an 11 μm -long MUTC PD at -2 V after RTA at 400 °C for 15 s, compared with a reference PIN PD of the same length. The dashed line indicates the smoothed response. (d) Extracted 3-dB bandwidth as a function of mesa length after RTA.

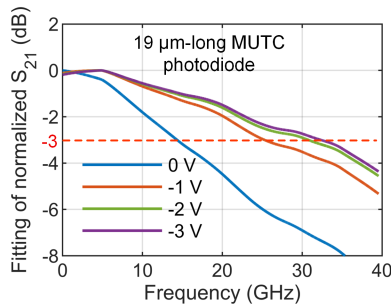


Figure 2.29: Fitted normalized S_{21} frequency responses of the 19- μm -long MUTC photodiode measured under different reverse-bias voltages.

time bandwidth simulation results and the impedance measurement results, as expressed in the following formula:

$$BW = \frac{1}{\sqrt{\left(\frac{1}{BW_{tr}}\right)^2 + \left(\frac{1}{BW_{RC}}\right)^2}} \quad (2.7)$$

where BW_{tr} is the transit-time bandwidth, and BW_{RC} is the RC bandwidth.

Fig. 2.30 shows the calculated RC bandwidth and the estimated overall bandwidth as a function of photodiode mesa length. For the reference PIN photodiode, the RC bandwidth is relatively high, but the estimated overall bandwidth remains around 20–25 GHz because it is mainly limited by the slow hole transport in the intrinsic absorption region. In contrast, the MUTC photodiode exhibits a much higher transit-time bandwidth owing to the introduction of the p-InGaAs absorption layer. As a result, the estimated overall bandwidth is significantly improved compared with the reference PIN photodiode.

However, the estimated overall bandwidth of the MUTC photodiode follows the trend of the RC-limited bandwidth, indicating that the fabricated MUTC devices are mainly RC-limited. This explains why the measured bandwidth does not reach the intrinsic bandwidth potential suggested by the carrier-transport analysis. The current limitation is mainly attributed to the relatively large junction capacitance associated with the mesa dimension and the series resistance. Further improvement can therefore be achieved by reducing the mesa width to lower the capacitance, optimizing the contact and metallization process to reduce the series resistance, and improving the RF pad and interconnect layout to reduce parasitic effects.

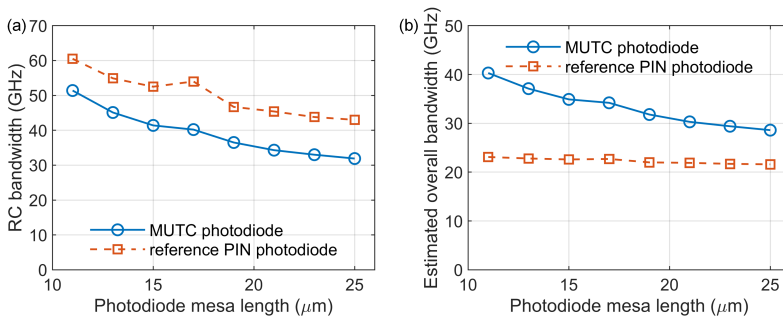


Figure 2.30: Bandwidth estimation. (a) Calculation of RC bandwidth based on photodiode impedance measurement results. (b) Estimation of the photodiode overall bandwidth by combining the simulated transit-time bandwidth with the RC bandwidth derived from the measured impedance.

2.5.4 High-speed large-signal reception

The high-speed, large-signal reception characteristics of the MUTC PDs were evaluated using an eye diagram test. Here, “large-signal” refers to the use of a high-speed NRZ electrical data signal to drive the Mach–Zehnder modulator. The continuous-wave optical carrier was therefore converted into a wideband intensity-modulated optical data signal before being detected by the PD. No large electrical signal was applied directly to the PD, and the term does not imply operation of the PD in the nonlinear or saturation regime.

The setup for the high-speed large-signal reception measurement is illustrated in Fig. 2.31. An O-band tunable laser (Santec TSL510-131) was set to the wavelength of 1310 nm. The laser signal was modulated using a 40 Gbit/s modulator (Photline MX-LN-40), which was packaged with an RF amplifier (Photline DR-DG-40). The modulator was driven by an arbitrary waveform generator (AWG, Keysight M9502A) to load the signal onto the laser. To enhance the optical signal, an O-band fiber amplifier (Thorlabs PDFA100) was used for inline optical amplification. A variable optical attenuator (VOA) was placed after the amplifier to adjust the optical power supplied to the PD. The laser output was then split, with 50% directed to the PD under test and the remaining 50% monitored by an optical power meter (HP 81531A). The PD was electrically probed using a GSG probe (MPI T40A-GSG0100), which was connected to a bias-T (SHF BT65R-A). The PD was biased using a source meter (Keithley 2400). The RF signal generated by the PD was amplified using an RF amplifier (SHF S807) before being measured by a sampling oscilloscope (Agilent DCA-X 86100D).

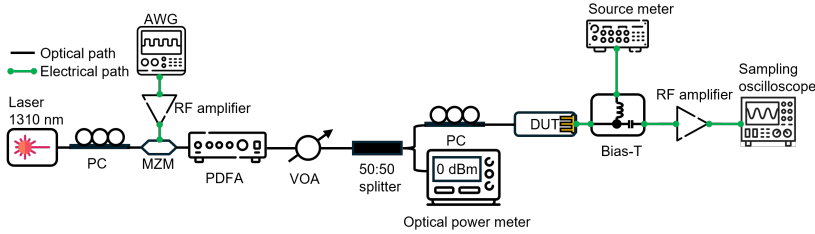


Figure 2.31: Setup for the high-speed large-signal measurement.

A non-return-to-zero (NRZ) signal composed of a pseudo-random binary sequence (PRBS) with a length of $2^7 - 1$ was generated at the wavelength of 1310 nm. A 17 μm -long MUTC PD was tested under a -2 V bias voltage. The measured eye diagrams are presented in Fig. 2.32(a). An optical power of -6.06 dBm was launched into the PD, resulting in a photocurrent of 0.23 mA. Clear eye openings are observed for bit rates up to 40 Gbit/s. High signal-to-noise ratios (SNRs) of 11.9

and 9.51 were obtained for the 20 Gbit/s and 30 Gbit/s measurements, respectively. At 40 Gbit/s, however, the SNR decreases to 4.49, primarily due to the speed limitation of the modulator in the measurement system. This limitation leads to the higher bit-error rate (BER) observed at 40 Gbit/s, as shown in Fig. 2.32(b). At a BER of 10^{-12} , the receiver sensitivities are -10.9 dBm and -9.5 dBm for 20 Gbit/s and 30 Gbit/s, respectively.

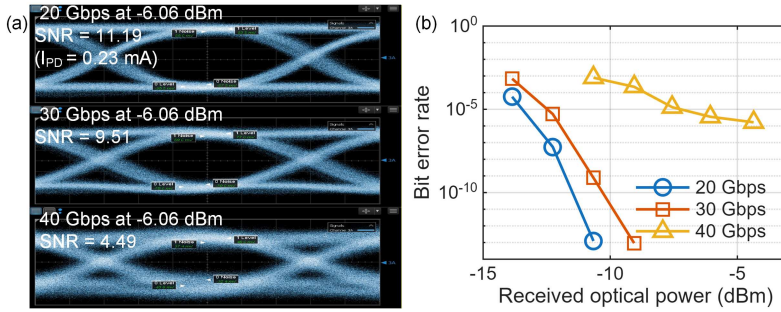


Figure 2.32: The measured high-speed data reception performance of a $17\ \mu\text{m}$ long MUTC PD when operating at -2 V bias voltage. (a) The measured eye diagrams for 20, 30, and 40 Gbit/s NRZ signals at a received optical power of -6.06 dBm. (b) The measured bit error rate as a function of received optical power for 20, 30, and 40 Gbit/s NRZ signals.

The performance of the measurement system was evaluated by replacing the PD under test with a 43 GHz commercial photodetector (Discovery DSC-10H). Figure 2.33(a) shows its frequency response, taken from the test report provided by Discovery Semiconductor, Inc. The corresponding eye diagrams at 20 Gbit/s, 30 Gbit/s, and 40 Gbit/s for NRZ signals, measured at a photocurrent of 0.23 mA, are shown in Fig. 2.33(b). A notable SNR degradation—from 9.04 to 4.93—occurs when increasing the bit rate from 30 Gbit/s to 40 Gbit/s, indicating that the system performance becomes limited by the modulator at 40 Gbit/s operation.

2.6 Conclusion

This chapter presents the successful integration of high-speed, high-responsivity O-band InGaAs/InP PDs on an LPCVD SiN photonic platform using μTP . The demonstrated PDs exhibit a high responsivity of 1 A/W at 1310 nm and maintain a low dark current below 38 nA at -2 V bias voltage. By employing a MUTC-type epitaxial layer design, the 3-dB bandwidth is extended to 37 GHz, a 12 GHz improvement over a reference PIN PD, demonstrating enhanced high-speed performance. The PDs support NRZ signal reception at rates up to 40 Gbit/s, with clear eye diagrams observed. Excellent sensitivity performance is achieved at a

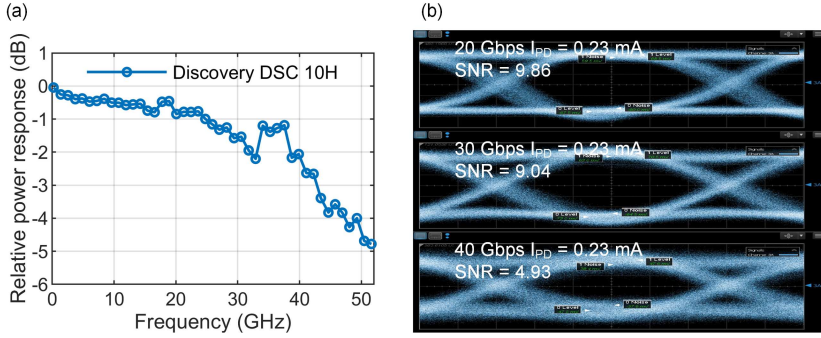


Figure 2.33: Evaluation of the eye-diagram measurement system using a 43-GHz commercial photodetector (Discovery DSC-10H). (a) Frequency response of the photodetector, with data points taken from the test report provided by Discovery Semiconductor, Inc. (b) Eye diagrams at 20 Gbit/s, 30 Gbit/s, and 40 Gbit/s NRZ signals measured at a photocurrent of 0.23 mA.

BER level of 10^{-12} for 20 Gbit/s and 30 Gbit/s signals, notably without the use of equalization techniques. These results establish the demonstrated PDs as a key building block for high-performance photonic receivers on SiN platforms. Based on this foundation, more advanced receiver architectures, such as multi-channel CWDM receivers, can be realized.

3

O-band 4×32 Gbit/s CWDM receiver on silicon nitride with micro-transfer-printed InGaAs/InP photodiodes

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3.1 Introduction

The integration of high-speed InGaAs/InP photodiodes on a silicon nitride (SiN) platform using micro-transfer printing, as demonstrated in Chapter 2, establishes a key building block for SiN-based optical receivers. However, practical optical interconnect systems require not only high-performance photodetectors, but also the integration of wavelength-selective components and multi-channel architectures to achieve high aggregate bandwidth.

This system-level requirement is driven by the rapid advancement of artificial intelligence, which is leading to a dramatic increase in bandwidth demand for data centers [69–72] and high-performance computing systems [72–75]. Silicon photonics (SiPh) has therefore emerged as a key enabling technology, offering a much higher bandwidth density than conventional copper interconnects. State-of-the-art platforms, such as imec’s iSiPP50G, provide essential building blocks—including high-speed modulators, Ge photodetectors, and WDM filters—through scalable and cost-effective manufacturing processes [76]. More recently, chiplet-based optical I/O architectures compatible with UCIe have been proposed to overcome the bandwidth, power, and reach limitations of electrical interconnects by employing highly parallel optical lanes at moderate per-lane data rates (e.g., 32 Gbit/s), enabling terabit-class aggregate bandwidth [77].

In such systems, bandwidth scaling is typically achieved through wavelength-division multiplexing (WDM), where multiple wavelength channels are transmitted and detected in parallel. In particular, coarse WDM (CWDM) in the O-band provides an efficient trade-off between system complexity and throughput, allowing high aggregate data rates while maintaining moderate per-lane speeds.

To implement wavelength-selective receiver architectures, the choice of photonic integration platform is critical. Compared with silicon (Si), silicon nitride (SiN) offers several distinct advantages, particularly its low waveguide loss and low thermo-optic coefficient. Ultralow waveguide losses below 1 dB/m have already been experimentally demonstrated in SiN platforms [42]. In addition, the thermo-optic coefficient of SiN ($2.45 \times 10^{-5} / ^\circ\text{C}$) is approximately one-seventh that of

silicon, leading to significantly improved thermal stability. For example, the thermal sensitivity of SOI CWDM filters is typically 70–80 pm/°C, whereas SiN-based devices exhibit values as low as 14–19 pm/°C [78–80]. Furthermore, reliable operation of SiN-based (de-)multiplexers at temperatures up to 80 °C has been demonstrated [79]. Compared with SiPh platforms, the lower refractive-index contrast of the SiN/SiO₂ system also inherently reduces the sensitivity of the optical phase to fabrication-induced dimensional variations. These properties make SiN particularly attractive for wavelength-selective circuits in WDM receivers.

However, despite these advantages, SiN lacks intrinsic photodetection capability, in contrast to silicon photonics platforms that support monolithic integration of germanium photodiodes. As a result, the realization of fully integrated SiN-based receivers requires the heterogeneous integration of high-performance III–V photodiodes. Micro-transfer printing is a scalable and versatile approach for this purpose, enabling the deterministic integration of prefabricated active devices onto Si/SiN photonic platforms with high placement accuracy, high throughput, and excellent yield [21, 22, 64, 81, 82]. This technique is particularly well suited for integrating compact, high-bandwidth InGaAs/InP photodiodes at the output ports of wavelength demultiplexers.

Recent demonstrations have validated the feasibility of integrating III–V photodiodes on SiN using micro-transfer printing [56, 83]. Building on the device-level results presented in Chapter 2, this chapter advances toward system-level integration by demonstrating an O-band four-channel CWDM receiver photonic integrated circuit (PIC) on a 300 nm low-pressure chemical vapor deposition (LPCVD) SiN platform. The receiver integrates a compact cascaded MZI lattice filter demultiplexer with micro-transfer-printed InGaAs/InP photodiodes exhibiting a 33 GHz 3-dB bandwidth. High-speed reception at 32 Gbit/s NRZ is demonstrated across all four wavelength channels, achieving bit-error rates (BERs) below the HD-FEC threshold. To the best of our knowledge, this represents the first demonstrations of a multi-channel O-band CWDM receiver on SiN with micro-transfer-printed photodiodes supporting > 30 Gbit/s operation, paving the way for scalable and energy-efficient optical interconnect systems.

3.2 Theory of FIR Wavelength Filters for CWDM Systems

3.2.1 Fundamentals of CWDM

Coarse wavelength division multiplexing (CWDM) is an optical multiplexing technique that increases the bandwidth capacity of optical communication systems by allowing multiple wavelength channels to propagate simultaneously within a single optical fiber or waveguide. Each channel can independently carry high-speed data, allowing efficient utilization of the available optical spectrum.

ITU-T Recommendation G.694.2 specifies CWDM channels spanning a wavelength range of approximately 1270–1610 nm, as illustrated in Fig. 3.1. In contrast to dense wavelength division multiplexing (DWDM), CWDM adopts a relatively coarse channel spacing of 20 nm, which permits a nominal wavelength tolerance of ± 6.5 nm. This relaxed spacing significantly reduces the requirements on wavelength accuracy, temperature control, and fabrication tolerances of optical components, thereby lowering system complexity and cost. Consequently, CWDM is well suited for short- to medium-reach optical links and cost-sensitive applications. Within the O-band (1260–1360 nm), the standardized CWDM center wavelengths are 1271, 1291, 1311, and 1331 nm.

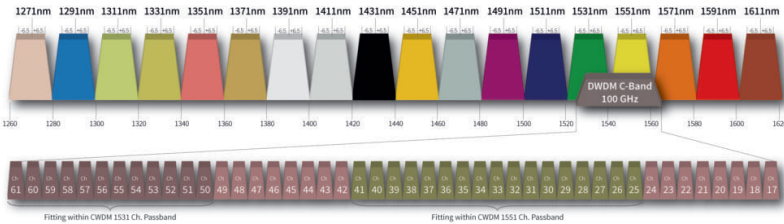


Figure 3.1: CWDM and DWDM channel diagram, reproduced from [84].

3.2.2 Finite impulse response wavelength filters

Efficient wavelength (de-)multiplexing requires optical filters with low insertion loss and a high rejection ratio for adjacent channels. Figure 3.2 illustrates several common implementations of wavelength-selective optical filters. Most of these designs rely on a finite number of interfering optical delay lines arranged in a feed-forward architecture, and therefore belong to the class of finite impulse response (FIR) filters. Representative examples include the Mach–Zehnder interferometer

(MZI) lattice filter, the arrayed waveguide grating (AWG), and the echelle grating, as shown in Fig. 3.2(a)–(c).

In contrast, coupling optical delay lines to form a feedback loop that supports resonant behavior results in an infinite impulse response (IIR) filter. A representative example is the ring resonator, as illustrated in Fig. 3.2(d). Compared to FIR filters, IIR filters are typically more compact, as the same delay line is reused multiple times through feedback. However, the resonant nature of IIR filters leads to significantly enhanced intracavity optical power, which makes them more susceptible to nonlinear effects.

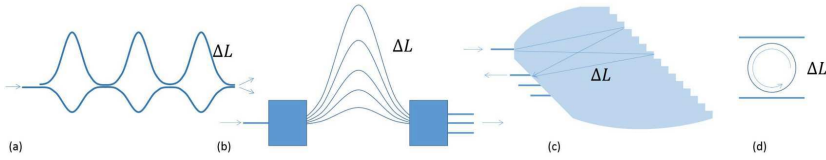


Figure 3.2: Different implementations of delay-line-based optical filters. (a) Mach-Zehnder interferometer (MZI) lattice filter, (b) arrayed waveguide grating (AWG), (c) echelle grating, and (d) ring resonator. The structures in (a)–(c) operate as finite impulse response (FIR) filters, consisting exclusively of feed-forward delay lines. In contrast, the ring resonator in (d) incorporates a feedback loop, resulting in an infinite impulse response (IIR) filter. Figure is reproduced from Ref. [85].

MZI lattice filters implement FIR wavelength filtering by cascading multiple MZIs to generate a set of discrete optical delay paths. Light propagates through different combinations of interferometric arms, and contributions with identical delays are coherently recombined at the output. The spectral response depends on the relative amplitudes and phases of light in the delay paths, determined by the coupling coefficients and delay-line lengths at each stage. This architecture offers a high degree of freedom in shaping the filter response, enabling sharp roll-off, low crosstalk, and flat passbands when properly designed. However, as the filter order increases, phase errors in the delay lines and inaccuracies in the coupling coefficients accumulate, making high-order MZI lattice filters increasingly sensitive to fabrication variations and environmental changes.

AWGs realize FIR wavelength filtering by distributing light over a large number of waveguides with incremental path length differences and recombining them using slab-waveguide star couplers. The star couplers act as imaging systems: when all delay contributions are in phase, the input field is imaged onto a specific position in the output plane, while changes in wavelength cause a lateral shift of the image. As a result, different wavelengths are directed to different output waveguides, making AWGs particularly well suited for multi-channel wavelength demultiplexing on a regular wavelength grid. Compared to MZI lattice filters,

AWGs provide a compact and scalable solution for high channel counts. However, the imaging-based recombination leads to a convolution of the ideal filter response with the mode profiles of the apertures, which limits passband flatness and reduces independent control over the individual delay-line coefficients.

Echelle gratings also implement FIR wavelength filtering using an imaging principle. Light propagates through a free-space region and is reflected from a set of grating facets positioned at different optical distances, typically arranged along a Rowland circle. The reflected beams interfere constructively or destructively depending on wavelength, and the resulting angular dispersion allows different wavelengths to be focused onto different output waveguides. Echelle gratings offer high spectral resolution and can achieve compact layouts with relatively simple geometries. Similar to AWGs, their performance is influenced by imaging effects and fabrication accuracy of the grating facets, which constrains independent control of the delay-line weights and introduces trade-offs between insertion loss, crosstalk, and footprint.

Ref. [86] provides a systematic comparison of the three aforementioned demultiplexer architectures for a four-channel C-band wavelength demultiplexer, considering key performance metrics including insertion loss, channel crosstalk, the 1 dB/10 dB bandwidth ratio, and device footprint, as summarized in Table 3.1. The cascaded MZI lattice filter shows superior performance in terms of insertion loss and 1 dB/10 dB ratio, while the AWG and Echelle grating architectures offer lower channel crosstalk.

Table 3.1: Performance comparison of different C-band four-channel wavelength demultiplexers. The data are reproduced from Ref. [86].

Device	IL (dB)	XT (dB)	1 dB/10 dB	Footprint (μm^2)
MZI lattice filter	1.2	-11	0.9	280×260
AWG	5.0	-20	0.6	270×270
Echelle grating	5.2	-21	0.44	610×310

3.3 Design and simulation of the O-band CWDM receiver

3.3.1 Operating principle of the CWDM demultiplexer

An O-band four-channel CWDM demultiplexer is designed based on a cascaded MZI lattice filter architecture. A schematic of the proposed demultiplexer is shown in Fig. 3.3.

The demultiplexer consists of two filtering stages. The first stage employs a single lattice filter (Filter 1) to separate the input optical signal into odd and even wavelength channels. In the second stage, two additional lattice filters (Filter 2 and Filter 3) further demultiplex the separated wavelength groups into four individual output channels. As a result, each CWDM wavelength is routed to a distinct output port.

Each lattice filter is a four-port device formed by two cascaded MZIs and consists of three directional couplers and two asymmetric delay lines. The spectral response of the filter is governed by the combined effect of the directional coupler coupling ratios and the relative phase delays introduced by the unequal interferometer arm lengths. By properly selecting these parameters, flat-top passbands with high channel isolation can be achieved.

The power cross-coupling coefficients of the three directional couplers are chosen to be 0.50, 0.29, and 0.08, respectively, following the optimized design reported in Ref. [87].

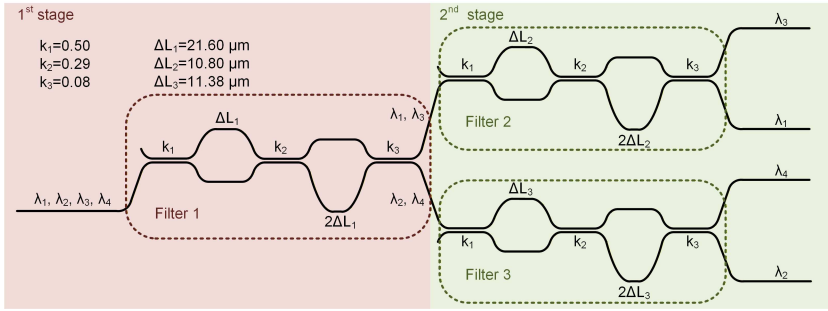


Figure 3.3: Schematic of the O-band four-channel CWDM demultiplexer based on cascaded MZI lattice filters.

3.3.2 Directional coupler design and numerical simulation

Directional couplers are designed to realize the target power cross-coupling coefficients of 0.50, 0.29, and 0.08. Fig. 3.4 shows the GDS layout of the implemented directional couplers. Each coupler is configured as a four-port structure and incorporates four 90-degree waveguide bends at the input and output ports. All bends have a radius of 40 μm to minimize bending loss.

The coupling region consists of a pair of closely spaced straight waveguides with a width of 1.15 μm and an inter-waveguide gap of 250 nm. The coupling strength is controlled by adjusting the interaction length of the straight coupling section,

allowing the desired power cross-coupling coefficients to be accurately achieved.

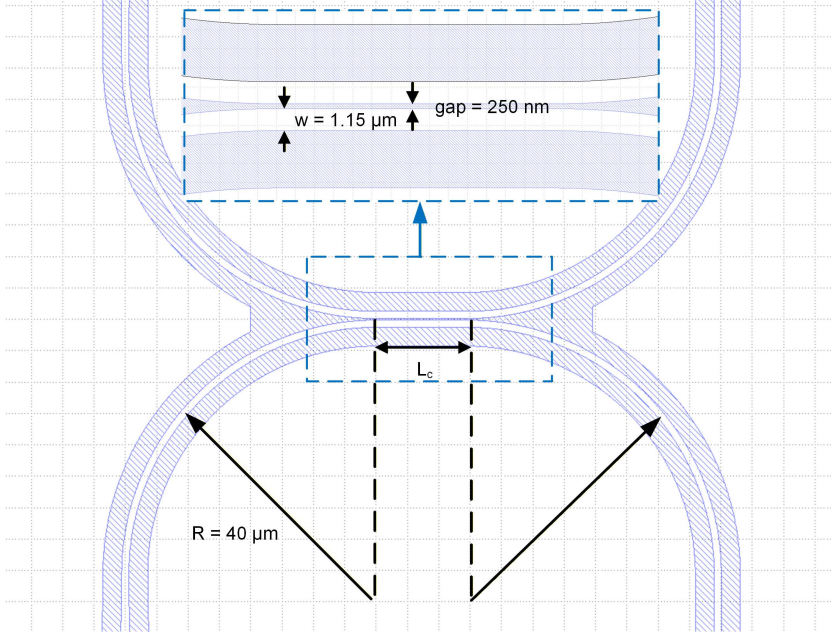


Figure 3.4: GDS layout design of the directional couplers.

Numerical simulations of the directional couplers were performed using the Lumerical FDTD solver. The simulation results are presented in Fig. 3.5. Fig. 3.5(a) shows the simulated power cross-coupling coefficient k as a function of the straight coupling length L_c . To realize the target coupling coefficients of $k = 0.50, 0.29$, and 0.08 , the corresponding straight coupling lengths are determined to be $13.35, 7.34$, and $0 \mu\text{m}$, respectively. Figures 3.5(b)–(d) show the simulated optical power distributions for the three designed directional couplers.

3.3.3 Delay-line parameter determination

The spectral characteristics of the demultiplexer are designed to meet a target channel spacing of 20 nm in the O-band. To achieve this spacing, the FSRs of the lattice filters in the first and second stages are selected to be 40 nm and 80 nm , respectively. The FSR of an MZI-based filter is inversely proportional to the optical path length difference between its two arms and is given by

$$FSR = \frac{\lambda^2}{n_g \Delta L}, \quad (3.1)$$

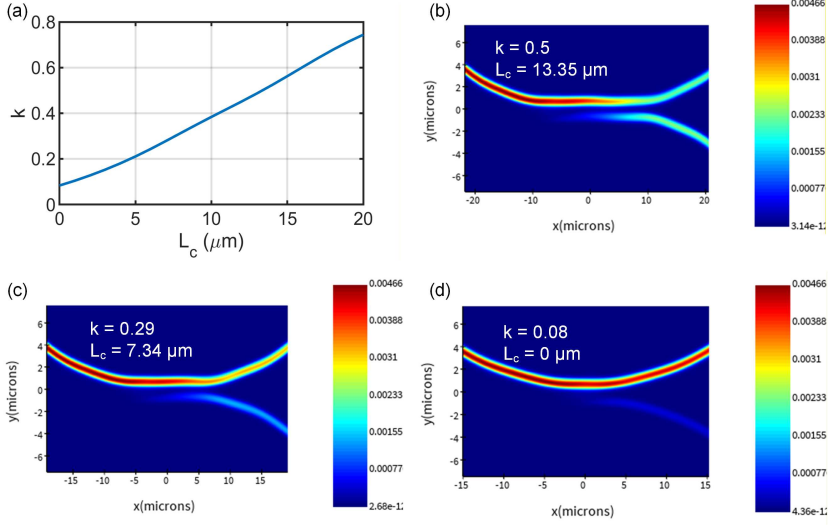


Figure 3.5: FDTD simulation results of the directional couplers. (a) Power cross-coupling coefficient k as a function of the straight coupling length L_c . (b)–(d) Simulated optical power distributions for directional couplers with power cross-coupling coefficients of 0.50, 0.29, and 0.08, corresponding to straight coupling lengths of 13.35, 7.34, and $0 \mu\text{m}$, respectively.

where λ is the center wavelength of interest, n_g is the group index of the waveguide, and ΔL is the physical length difference between the interferometer arms.

The group index of the silicon nitride waveguide is obtained from finite difference eigenmode (FDE) simulations. Figure 3.6(a) shows the simulated group index of a $1.15\text{-}\mu\text{m}$ -wide SiN strip waveguide across the O-band wavelength range. Using the extracted group index at the target center wavelength, the required delay length parameters are calculated to be $\Delta L_1 = 21.60 \mu\text{m}$ for Filter 1 and $\Delta L_2 = 10.80 \mu\text{m}$ for Filter 2. For each lattice filter, two delay lines with lengths of ΔL and $2\Delta L$ are implemented.

In the lower branch of the second stage, corresponding to Filter 3, a slight modification of the delay-line length is introduced to align the filter passbands with the CWDM wavelength grid. Specifically, an additional phase shift of $3\pi/2$ is required. This phase shift is implemented by increasing the delay length by

$$\Delta L' = \frac{3\lambda}{4n_{\text{eff}}}, \quad (3.2)$$

where n_{eff} is the effective index of the guided mode. The simulated effective index of the waveguide is shown in Fig. 3.6(b). Taking this correction into account, the delay length parameter for Filter 3 is determined to be $\Delta L_3 = 11.38 \mu\text{m}$.

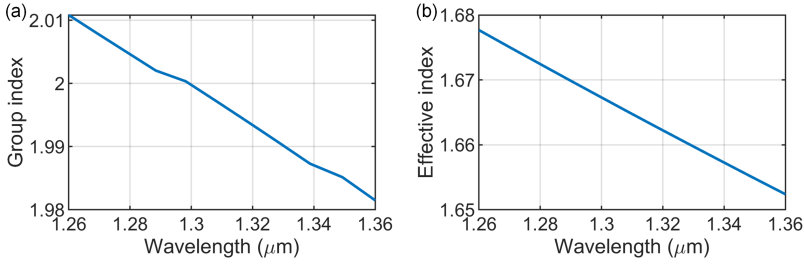


Figure 3.6: Numerical simulations of (a) the group index and (b) the effective index of a 1.15-μm-wide SiN strip waveguide across the O-band.

3.3.4 Transfer-matrix modeling of the MZI lattice filters

The transmission characteristics of the cascaded MZI lattice filters are analyzed using the transfer matrix method (TMM), which provides an efficient and accurate framework for modeling linear optical circuits composed of cascaded passive components. In this method, each building block of the circuit is represented by a 2×2 transfer matrix that relates the complex electric field amplitudes at its input and output ports.

A directional coupler is described by the transfer matrix

$$\mathbf{M}_{\text{DC}} = \begin{pmatrix} \sqrt{1-k} & -j\sqrt{k} \\ -j\sqrt{k} & \sqrt{1-k} \end{pmatrix}, \quad (3.3)$$

where k denotes the power cross-coupling coefficient of the coupler (e.g., $k = 0.5$ for a 3-dB coupler).

Propagation through asymmetric delay lines in the two arms of the Mach–Zehnder interferometer introduces wavelength-dependent phase shifts. These phase delays are represented by diagonal propagation matrices. When a delay line of length ΔL is placed in the upper arm, the corresponding matrix is given by

$$\mathbf{P}_1 = \begin{pmatrix} e^{-j\beta\Delta L} & 0 \\ 0 & 1 \end{pmatrix}, \quad (3.4)$$

whereas a delay line of length $2\Delta L$ in the lower arm is described by

$$\mathbf{P}_2 = \begin{pmatrix} 1 & 0 \\ 0 & e^{-j\beta(2\Delta L)} \end{pmatrix}, \quad (3.5)$$

with β denoting the propagation constant of the waveguide.

For each lattice filter, the overall transfer matrix is obtained by cascading the matrices of the three directional couplers and the two phase-delay sections. The

relationship between the input and output electric fields can therefore be written as

$$\begin{pmatrix} E_{\text{out}1} \\ E_{\text{out}2} \end{pmatrix} = \mathbf{M}_{\text{DC}3} \mathbf{P}_2 \mathbf{M}_{\text{DC}2} \mathbf{P}_1 \mathbf{M}_{\text{DC}1} \begin{pmatrix} E_{\text{in}1} \\ E_{\text{in}2} \end{pmatrix}. \quad (3.6)$$

3.3.5 Simulated spectral response of the demultiplexer

Using the transfer-matrix model described above, the transmission spectra of Filters 1, 2, and 3 are calculated as a function of wavelength. The simulated responses are shown in Fig. 3.7(a)–(c). In the first-stage filter, wavelength channels centered at 1270 nm and 1310 nm are routed to the cross port, while channels centered at 1290 nm and 1330 nm are directed to the bar port, thereby separating the odd and even channels.

The second-stage filters further demultiplex these wavelength pairs into individual channels. Filter 2 separates the channels routed to the upper branch of the first stage, while Filter 3 separates the channels routed to the lower branch. The delay-line adjustment introduced in Filter 3 ensures proper alignment of its passbands with the CWDM wavelength grid.

The overall transmission spectra at the four output ports of the demultiplexer are shown in Fig. 3.7(d). Each CWDM channel, centered at 1270 nm, 1290 nm, 1310 nm, and 1330 nm, is successfully routed to a distinct output port.

3.3.6 SiN PIC layout design of the O-band CWDM receiver

An overview of the GDS layout is presented in Fig. 3.8. The PIC integrates multiple structures, including two CWDM receivers with photodiodes and transimpedance amplifiers (TIAs) co-integrated via μTP , a CWDM receiver with photodiodes transfer-printed on grating couplers, a passive demultiplexer serving as a reference, and reference photodiodes transfer-printed on SiN waveguides.

The O-band four-channel CWDM receiver investigated in this chapter is shown in Fig. 3.9(a). The receiver consists of a wavelength demultiplexer based on three cascaded MZI lattice filters, four transfer-printed InGaAs/InP photodiodes integrated at the output waveguides, and a reference waveguide for calibration. In the demultiplexer, the first MZI stage separates the odd and even channels, while the second stage further resolves the individual CWDM wavelengths. The overall footprint of the receiver is $3300 \mu\text{m} \times 2200 \mu\text{m}$.

An advanced receiver layout with μTP -based co-integration of TIAs is shown in Fig. 3.9(b) and will be investigated in future work. By enabling compact co-

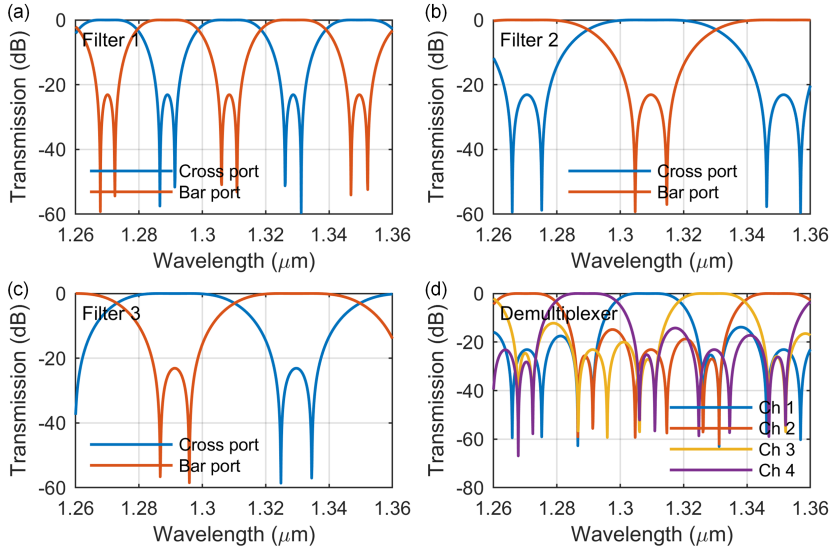


Figure 3.7: Simulated transmission spectra of the CWDM demultiplexer. (a) Transmission response of Filter 1. (b) Transmission response of Filter 2. (c) Transmission response of Filter 3. (d) Transmission spectra at the four output ports of the demultiplexer.

integration of photodiodes and TIAs in close proximity, parasitic capacitance and interconnect length can be reduced, leading to lower input-referred noise and improved receiver sensitivity.

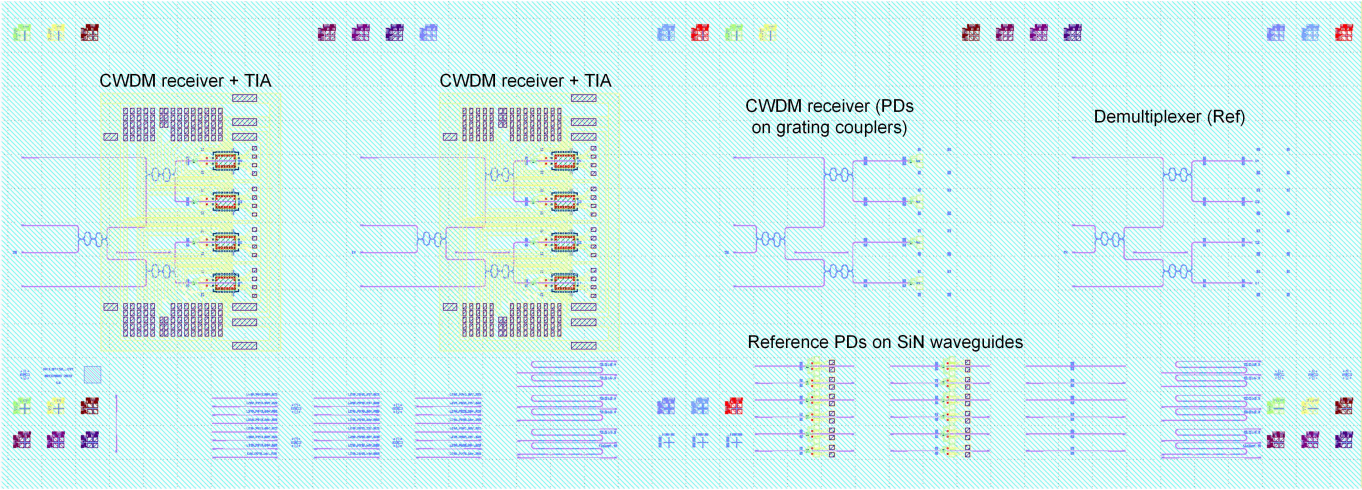


Figure 3.8: Overview of the SiN PIC GDS layout, with two CWDM receivers with PDs and TIAs co-integrated via μ TP, a CWDM receiver with PDs transfer-printed on grating couplers, a passive demultiplexer used as a reference, and reference PDs transfer-printed on SiN waveguides.

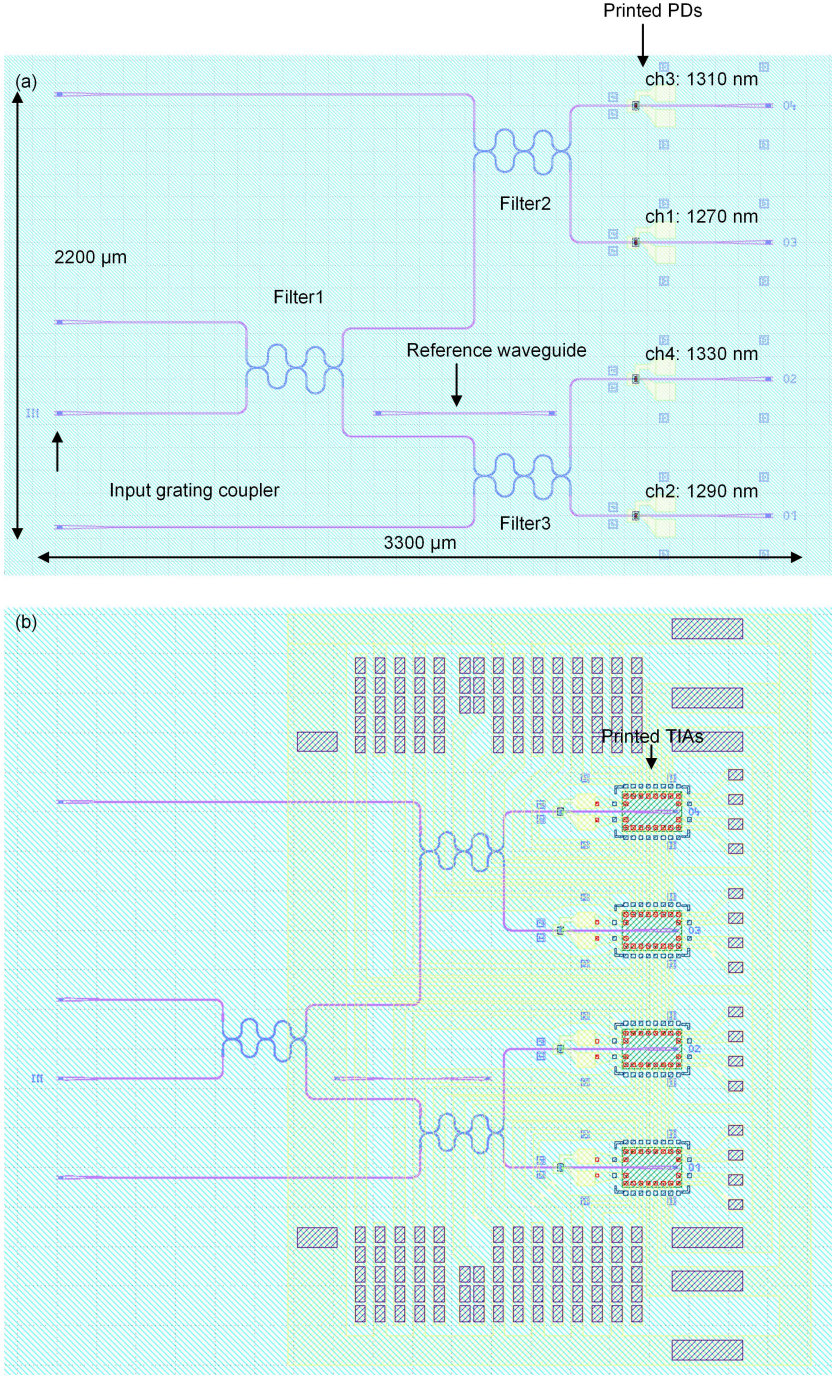


Figure 3.9: SiN PIC layout design. (a) GDS layout of the O-band four-channel CWDM receiver investigated in this chapter, in which PDs are transfer-printed on four output SiN waveguides. (b) An advanced receiver layout with μ TP-based co-integration of TIAs.

3.4 Fabrication

3.4.1 Overview of the fabricated receiver PIC

The fabricated O-band four-channel CWDM receiver PIC is shown in Fig. 3.10. The device is implemented on a 300 nm LPCVD SiN photonic platform with a 1.8 μm BCB cladding layer and has a total footprint of 3300 μm $\times$ 2200 μm .

Optical signals are coupled into the chip through grating couplers. The insertion loss of the grating couplers is characterized using a reference waveguide located at the center of the PIC and is subsequently de-embedded from the measured results. InGaAs/InP photodiodes are integrated at the output ports of the demultiplexer via micro-transfer printing. The inset of Fig. 3.10 shows a magnified view of the printed photodiodes. Each photodiode coupon is accurately aligned and placed on top of the SiN waveguide and includes cathode and anode metal pads for electrical probing.

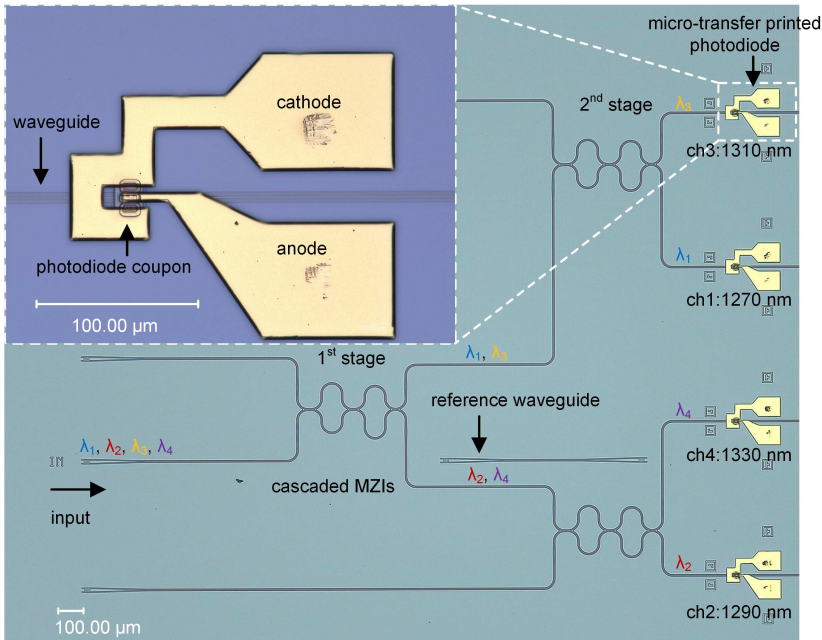


Figure 3.10: Microscope image of the O-band four-channel CWDM receiver PIC, with the inset showing a magnified view of the micro-transfer-printed photodiode.

3.4.2 Fabrication of the passive SiN PICs

The passive silicon nitride (SiN) photonic integrated circuits were fabricated on a 300 nm thick LPCVD SiN layer using electron-beam lithography (EBL) followed by reactive ion etching (RIE). The fabrication process started with a standard substrate cleaning sequence consisting of acetone, isopropanol (IPA), and deionized (DI) water, followed by a 15-minute oxygen plasma treatment in a Tepla system to enhance resist adhesion.

Electron-beam patterning was carried out using ARP 6200-13 resist, which was spin-coated at 3500 rpm for 60 s and baked at 150 °C for 1 min. After backside resist removal, a conductive polymer layer (Electra 92) was spin-coated at 2000 rpm for 60 s and baked at 90 °C for 2 min to suppress charging during EBL exposure. The patterns were written using a combination of fixed-beam moving-stage (FBMS) mode and direct writing, resulting in a total exposure time of approximately 5–6 hours for the full layout.

Following exposure, the sample was rinsed in DI water to remove the Electra 92 layer. Development was performed by immersing the sample in n-amyl acetate for 1 min, followed by a 30 s rinse in IPA.

The SiN layer was subsequently etched using CF_4/H_2 -based RIE. Complete etching of the SiN layer was achieved after 6 min 20 s, followed by an additional 1 min over-etch to ensure full pattern transfer. Residual resist was removed using AR 600-71 remover, followed by a soft oxygen plasma cleaning step.

The etch depth and remaining film thickness were characterized using multiple metrology techniques. Filmetrics measurements confirmed complete removal of the SiN layer down to the buried oxide in the waveguide regions, while Dektak profilometry measured an etch depth of approximately 337–340 nm.

3.4.3 Integration of the photodiodes

The photodiode design, fabrication, and heterogeneous integration follow the methods described in Chapter 2. Representative microscope images are shown in Figs. 3.11(a)–(c), illustrating (a) the fabricated photodiode coupons on the III-V source sample after release, (b) a photodiode coupon transfer printed onto a silicon nitride (SiN) waveguide, and (c) a completed device after post-printing processing and final metallization. The complete integration flow is schematically summarized in Fig. 3.11(d).

The use of micro-transfer printing (μTP) decouples the III-V device fabrication from the SiN photonic integrated circuit (PIC) processing. All critical III-V fabrication

steps are completed prior to heterogeneous integration, allowing the photodiode coupons developed in Chapter 2 to be directly reused [step (i)].

The released photodiode coupons are integrated onto a pre-fabricated passive SiN PIC using μ TP [steps (ii)–(iv)]. Before printing, a thin divinylsiloxane-benzocyclobutene (DVS-BCB) adhesive layer with a nominal thickness of approximately 100 nm is spin-coated onto the SiN PIC to promote adhesion. An X-Celeprint μ TP-100 system equipped with a polydimethylsiloxane (PDMS) stamp is used to pick up individual photodiode coupons from the source sample by mechanically breaking the SiN tethers. The coupons are then accurately aligned to the underlying SiN waveguides under optical microscopy and printed onto the target PIC. Controlled retraction of the stamp enables deterministic release of the coupon onto the BCB-coated surface, ensuring high placement accuracy and yield.

Following transfer printing, a series of post-printing processing steps is performed to complete the device integration. First, the protective photoresist layer on top of the photodiode coupon is removed, and the BCB adhesive layer is thermally cured at 270 °C to establish a mechanically stable bonding [step (v)]. Subsequently, a 1.8 μ m-thick BCB cladding layer is spin-coated and cured to provide electrical insulation and environmental protection [step (vi)]. Finally, via openings to the anode and cathode contacts are defined, followed by the deposition of the top-level metal interconnects and probe pads [steps (vii) and (viii)], thereby completing the fabrication of the waveguide-coupled photodiodes.

3.5 Characterization and discussion

3.5.1 Performance of the O-band four-channel demultiplexer

The performance of the demultiplexer was characterized using a reference structure without printed photodiodes. During all the measurements, the sample temperature was stabilized at 20 °C using a thermoelectric cooler (TEC). The spectra responses of the input and output grating couplers were de-embedded using the transmission of a reference waveguide. The measured transmission spectra are shown in Fig. 3.12. The device exhibits a free spectral range (FSR) of 77 nm, which is divided into four wavelength channels at 1270 nm, 1290 nm, 1310 nm, and 1330 nm, respectively. The key performance metrics of the demultiplexer are summarized in Table 3.2. The measured insertion losses are 2.4 dB at 1270 nm, 2.0 dB at 1290 nm, 1.7 dB at 1310 nm, and 2.4 dB at 1330 nm, with corresponding crosstalk levels of -14.4, -17.4, -14.0, and -16.6 dB. The reported crosstalk values were extracted by comparing the transmission of each channel with the maximum leakage from the other channels at

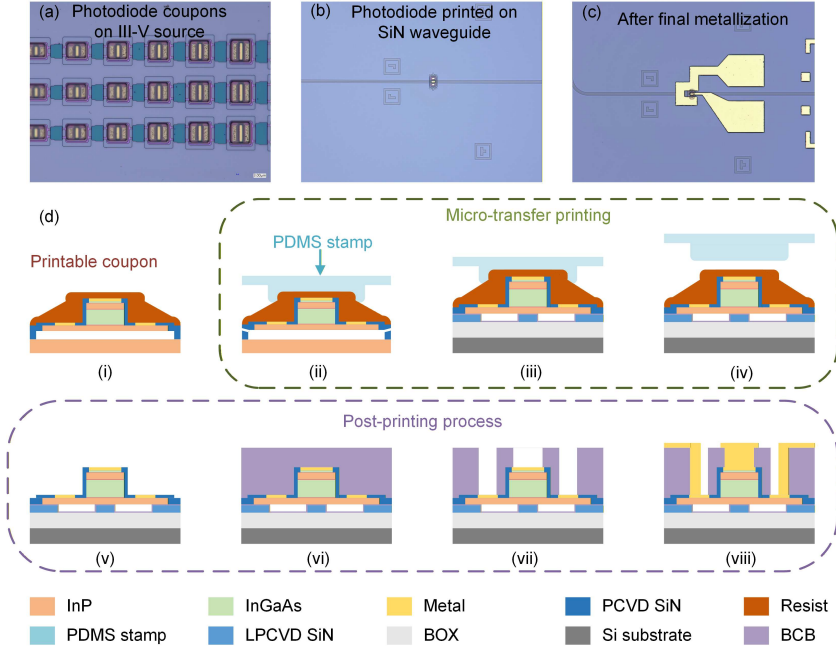


Figure 3.11: Integration process of photodiodes using micro-transfer printing. (a) Microscope image of photodiode coupons on the III–V source sample. (b) Microscope image of a photodiode printed onto a SiN waveguide. (c) Microscope image of a micro-transfer-printed photodiode after final metallization. (d) Process flow for photodiode integration: step (i) shows the prepared printable coupons; steps (ii)–(iv) correspond to the micro-transfer printing; steps (v)–(viii) illustrate the post-printing processes.

the same wavelength.

Although the measured channel transmission responses are not perfectly flat, the 32 Gbit/s NRZ signal used in the subsequent transmission experiment has an optical bandwidth considerably smaller than the overall transmission window of each channel. Therefore, the modulated signal occupies only a limited spectral range of the filter response. The measured filter bandwidth is thus considered sufficient for the demonstrated data-transmission experiment.

Expected thermal robustness of the SiN-based demultiplexer. As discussed in Section 3.1, the SiN platform offers an intrinsically low thermo-optic coefficient compared to Si, which translates into improved wavelength stability of passive photonic circuits. In the demonstrated receiver, this platform-level advantage directly benefits the cascaded MZI lattice demultiplexer, whose wide passband relaxes sensitivity to small temperature-induced wavelength shifts.

While a systematic temperature-dependent characterization of the complete receiver is beyond the scope of this work, the combination of the SiN platform and the lattice filter architecture is expected to provide robust operation under moderate temperature variations. Future work will focus on experimentally quantifying the temperature tolerance of the integrated receiver.

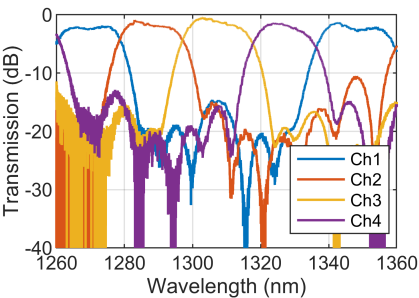


Figure 3.12: Measured transmission spectra of a reference four-channel demultiplexer.

Table 3.2: Metrics of the demultiplexer.

Metrics	1270 nm	1290 nm	1310 nm	1330 nm
Insertion loss (dB)	2.4	2.0	1.7	2.4
Crosstalk (dB)	-14.4	-17.4	-14.0	-16.6

Discussion on the impact of waveguide loss. Since no dedicated low-loss fabrication techniques, such as photonic Damascene processing or high-temperature

annealing, were employed, the SiN waveguides fabricated by conventional EBL and RIE are expected to exhibit propagation losses on the order of a few dB/cm [88, 89]. However, owing to the relatively short optical path length of the demultiplexer, the accumulated propagation loss is estimated to be below 1 dB. Consequently, propagation loss mainly contributes to a small increase in insertion loss and has little influence on the filter spectral response. The measured passband shape and channel isolation are therefore primarily governed by the coupling coefficients and the relative phase delays between the interferometer sections.

Fabrication tolerance, phase error and coupling-ratio deviations considerations. In cascaded MZI lattice filters, process variations, such as small deviations in waveguide width and effective index, can introduce phase errors in the interferometric delay arms. These phase errors may lead to passband misalignment with respect to the designed wavelength grid and result in wavelength-dependent performance variations, including differences in insertion loss and inter-channel crosstalk among the CWDM channels.

In the present work, the sensitivity to such phase errors is mitigated by employing relatively wide ($1.15\ \mu\text{m}$) single-mode TE SiN stripe waveguides in the delay arms. Compared to SiPh platforms, the lower refractive-index contrast of the SiN/SiO₂/BCB system inherently reduces the sensitivity of the optical phase to fabrication-induced dimensional variations. As a result, phase errors in SiN-based interferometric circuits are expected to be smaller for a given level of process variation.

Fabrication imperfections can also lead to deviations in the coupling coefficients of the directional couplers. Since the lattice-filter response relies on well-defined optical power splitting ratios, such deviations can distort the filter shape, increase the insertion loss, and degrade the channel isolation. Although several fabrication iterations were carried out to sweep and optimize the process parameters, residual process fluctuations can still introduce coupling-ratio errors and phase-delay errors, which partly explain the discrepancies between measurement and simulation.

While the measured transmission spectra indicate that the remaining wavelength-dependent variations are limited, further reduction of the measurement–simulation discrepancy would require improved fabrication accuracy and process stability. In addition, more accurate calibration of the coupling coefficients and effective indices, for example through dedicated test structures on the same wafer, could further improve the agreement between the designed and fabricated filter responses.

3.5.2 Performance of the micro-transfer-printed photodiodes

The performance of the micro-transfer-printed photodiodes was characterized using a reference device fabricated on the same PIC sample. Fig. 3.13(a) shows a microscope image of the reference structure, which incorporates a grating coupler for optical input and metal pads designed for GSG probing. The use of GSG probes enables more accurate probe de-embedding compared with GS probes, resulting in a more reliable bandwidth measurement. The I–V characteristics of the reference photodiode were measured using a source meter (Keithley 2400). As shown in Fig. 3.13(b), the device exhibits a dark current of 100 nA at a bias voltage of -2 V.

The responsivity was measured using an O-band tunable laser (TSL510-1310). The photodiode was biased at -2 V using the source meter. The laser wavelength was swept from 1260 to 1360 nm, and the resulting photocurrent was recorded. The grating coupler loss was de-embedded using a reference device during the responsivity calculation. The measured responsivity over the wavelength range of 1260–1360 nm is shown in Fig. 3.13(c). At wavelengths of 1270, 1290, 1310, and 1330 nm, the extracted responsivities are 0.54, 0.61, 0.65, and 0.72 A/W, respectively.

The S_{21} response was measured using the broadband electro-optic characterization setup described in Section 2.5.3, including the same calibration and de-embedding procedure. The 3-dB bandwidth of the device at 1310 nm under a bias of -2 V is 33.07 GHz, as extracted from the measured S_{21} response shown in Fig. 3.13(d).

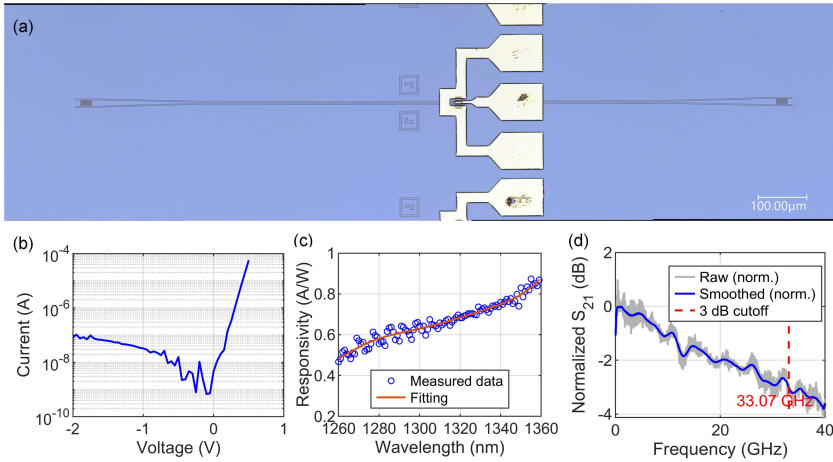


Figure 3.13: Measured performance of the reference photodiode. (a) Microscope image of the device. (b) I–V characteristics. (c) Responsivity over 1260–1360 nm. (d) S_{21} measurement at 1310 nm with the device biased at -2 V.

Discussion on bandwidth limitations and device reproducibility. The measured 3-dB bandwidth is primarily limited by the RC time constant of the device rather than by carrier transit time [83]. In the present design, the junction capacitance is mainly determined by the photodiode geometry and depletion region thickness defined at the coupon fabrication stage, where the mesa dimension is $13\ \mu\text{m} \times 6\ \mu\text{m}$ (corresponding to an active area of $78\ \mu\text{m}^2$).

As all photodiode coupons are fabricated using the same epitaxial structure and lithographic process on the III–V source wafer, similar junction capacitance and intrinsic RC-limited bandwidth are expected for all printed devices. Variations in optical coupling efficiency among printed photodiodes may arise from small placement offsets and local process variations during integration; however, such variations predominantly affect the measured responsivity and have a limited impact on the intrinsic electrical bandwidth.

The use of micro-transfer printing enables accurate placement of pre-fabricated photodiode coupons with high yield, supporting the scalability of this integration approach. A detailed device-to-device statistical analysis of the bandwidth is left for future work.

3.5.3 High-speed large-signal reception experiment

The high-speed large-signal reception performance of the receiver was evaluated by back-to-back eye-diagram measurements using the setup as shown in Fig. 3.14.

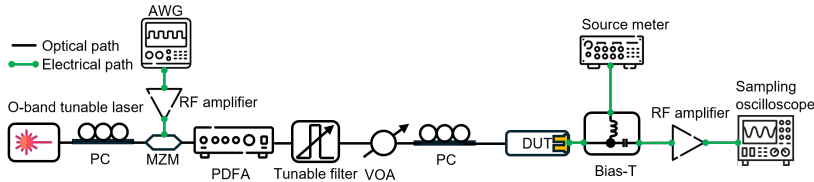


Figure 3.14: Back-to-back eye diagram measurement setup.

A 32 Gbit/s NRZ data stream based on a pseudo-random binary sequence (PRBS) of length $2^7 - 1$ was generated at 1270, 1290, 1310, and 1330 nm using an O-band tunable laser, a 40 Gbit/s MZM, and an arbitrary waveform generator (AWG, Keysight M9502A). The RF signal from the AWG was amplified to drive the MZM. The response of the external cables and connectors was pre-compensated using the AWG software. The modulated optical signal was subsequently amplified by an O-band praseodymium-doped fiber amplifier (PDFA), followed by a tunable optical filter to suppress amplified spontaneous emission (ASE) noise. A variable

optical attenuator was employed to control the input optical power. The signal was then coupled into the PIC through the input grating coupler and sequentially detected at the output ports by the integrated photodiodes, which were biased at -2 V. The generated RF signals were amplified by an SHF S807 RF amplifier and then recorded on a sampling oscilloscope (Agilent DCA-X 86100D). The eye diagrams were captured directly from the oscilloscope display.

The resulting back-to-back eye diagrams are shown in Fig. 3.15. During the measurement, the optical power was referenced to the waveguide power in front of the demultiplexer. All four channels operated at 32 Gbit/s NRZ with a demultiplexer-received optical power of -4.5 dBm and a photodiode bias of -2 V. The measured eye diagram SNRs for 1270, 1290, 1310, and 1330 nm were 6.43, 5.78, 5.83, and 5.86, respectively.

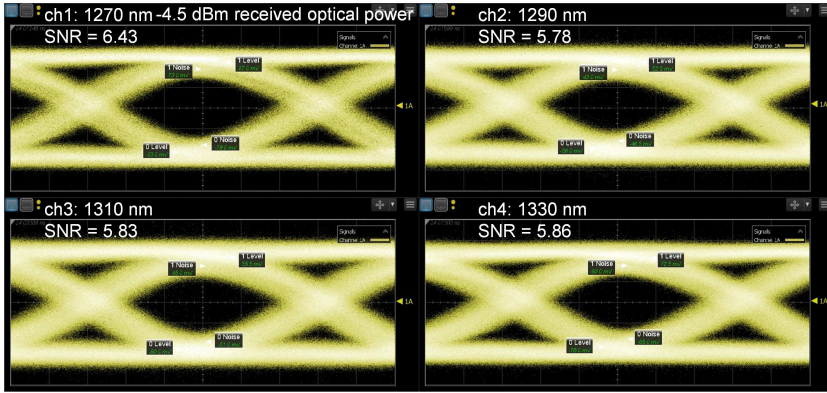


Figure 3.15: Back-to-back measured eye diagrams for the 4 channels operating with 32 Gbit/s NRZ signals at a received optical power of -4.5 dBm, with the photodiodes biased at -2 V.

In addition, the BER was measured as a function of the demultiplexer-received optical power for all four channels, as shown in Fig. 3.16. When the demultiplexer-received optical power exceeded -11 dBm, the BER values for all channels remained below 10^{-4} . The BER was derived from the SNR of the measured eye diagrams according to the Gaussian BER estimation. At lower demultiplexer-received optical powers, the eye diagrams became too noisy to allow accurate SNR extraction, thereby preventing reliable BER estimation.

Gaussian BER estimation based on eye diagram SNR. In this work, the BER is estimated from the measured eye diagram SNR. The eye diagram SNR is defined as

$$\text{SNR} = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}, \quad (3.7)$$

where μ_1 and μ_0 denote the mean voltage levels of the logical “1” and “0”, respectively, and σ_1 and σ_0 are the corresponding standard deviations extracted from the eye diagram.

Under the assumption of additive white Gaussian noise and symmetric decision thresholds, the BER for NRZ signaling can be approximated as

$$\text{BER} \approx \frac{1}{2} \text{erfc} \left(\frac{\text{SNR}}{\sqrt{2}} \right). \quad (3.8)$$

The measured eye diagrams shown in Fig. 3.15 exhibit clear eye openings without pronounced pattern-dependent distortions, indicating that the system is primarily noise-limited rather than inter-symbol-interference (ISI)-limited. Under such conditions, the noise distributions associated with logical “0” and “1” can be reasonably approximated as Gaussian. Nevertheless, it is acknowledged that Gaussian BER estimation may underestimate the true BER in the presence of residual ISI or other non-Gaussian noise contributions, particularly when extrapolated to very low BER levels (e.g., below 10^{-12}). In the present work, the estimated BER remains above this regime, where Gaussian-based BER estimation is generally considered to provide a reasonable approximation of system performance.

Analysis of channel-to-channel sensitivity variation. It can also be observed that the 1270 nm and 1330 nm channels exhibit better sensitivity compared with the 1290 nm and 1310 nm channels. The observed sensitivity variation among the channels can be attributed to a combination of factors, including the wavelength-dependent responsivity of the photodiodes, uncertainties in the insertion loss of the individual demultiplexer channels, and calibration inaccuracies of the grating coupler loss across different wavelengths.

The observed sensitivity differences among the four channels can be quantified to first order by the effective optical-to-electrical conversion gain of each channel, which scales with the product of the demultiplexer transmission and the photodiode responsivity. With the optical power referenced to the waveguide in front of the demultiplexer, the detected electrical signal amplitude is proportional to

$$G_i \propto R_i \times 10^{-IL_i/10}, \quad (3.9)$$

where R_i is the responsivity and IL_i is the demultiplexer insertion loss of channel i .

Using the measured demultiplexer insertion loss ($IL = 2.4/2.0/1.7/2.4$ dB) and responsivity ($R = 0.54/0.61/0.65/0.72$ A/W) at 1270/1290/1310/1330 nm, respectively, the relative gains G_i , normalized to the best-performing channel, are estimated to be 0.71/0.88/1.00/0.94. These correspond to $-1.51/-0.58/0/-$

0.26 dB. This indicates that the channel-to-channel sensitivity variation is largely explained by the combined effect of responsivity and demultiplexer insertion loss.

In addition, wavelength-dependent uncertainties in the grating-coupler calibration can introduce further apparent channel-to-channel variations and are likely responsible for the remaining mismatch between the simple gain-based estimate and the experimentally extracted BER trends. In practical systems, such variations can be readily mitigated by per-channel optical power leveling and/or electrical equalization, and therefore do not necessarily require a redesign of the demultiplexer.

Expected impact of inter-channel crosstalk in multi-wavelength operation.

In the back-to-back large-signal experiments, the eye diagrams were recorded by launching and detecting one wavelength channel at a time. Therefore, the measured eye diagrams and the corresponding SNR-derived BER mainly reflect the receiver performance without simultaneous data modulation on the other CWDM channels.

In practical multi-wavelength operation, signals leaking from the other demultiplexer channels would be detected together with the desired signal and would introduce data-dependent fluctuations in the received ‘0’ and ‘1’ levels. A conservative upper-bound estimate of the eye-opening reduction can be obtained from the measured optical crosstalk. For an interfering channel with a crosstalk level XT_i expressed in dB, the corresponding leaked optical-power ratio is

$$x_i = 10^{XT_i/10}. \quad (3.10)$$

Assuming equal launched powers, similar extinction ratios, and similar modulation depths for all wavelength channels, the total relative crosstalk from N interfering channels is

$$X_{\text{tot}} = \sum_{i=1}^N x_i. \quad (3.11)$$

Under a worst-case combination of data patterns, the leaked ‘1’ levels from the interfering channels may coincide with the ‘0’ level of the desired channel, whereas their ‘0’ levels may coincide with the desired ‘1’ level. The minimum relative eye opening can therefore be conservatively estimated as

$$\frac{\Delta P_{\text{eye}}}{\Delta P_{\text{eye},0}} \geq 1 - X_{\text{tot}}, \quad (3.12)$$

where $\Delta P_{\text{eye},0}$ is the eye opening without inter-channel crosstalk. The corresponding eye-opening penalty is

$$\text{Penalty}_{\text{XT}} \approx -10 \log_{10} (1 - X_{\text{tot}}). \quad (3.13)$$

This expression represents an eye-opening-based upper-bound estimate rather than an exact BER-derived receiver-sensitivity penalty.

The worst measured demultiplexer crosstalk is approximately -14 dB, corresponding to a leaked optical-power ratio of

$$10^{-14/10} \approx 0.040 \quad (3.14)$$

from one interfering channel. Assuming conservatively that each of the other three wavelength channels contributes the same worst-case leakage, the total relative crosstalk becomes

$$X_{\text{tot}} = 3 \times 10^{-14/10} \approx 0.119. \quad (3.15)$$

This corresponds to a worst-case eye-opening reduction of approximately 11.9% and an eye-opening penalty of approximately

$$-10 \log_{10}(1 - 0.119) \approx 0.55 \text{ dB}. \quad (3.16)$$

The actual penalty is expected to be lower because the crosstalk from all three interfering channels may not simultaneously reach the worst measured value, and the worst-case combination of data symbols does not occur continuously. Nevertheless, the estimate indicates that the measured crosstalk could produce a limited but non-zero impairment during simultaneous four-channel operation.

There is no unique crosstalk requirement corresponding to “no impact,” because this depends on the acceptable system penalty. Under the assumptions above, restricting the equivalent eye-opening penalty to below 0.5 dB would require the crosstalk from each of three equal-power interfering channels to be below approximately -14.4 dB. A more stringent penalty limit of 0.1 dB would require a crosstalk level below approximately -21.2 dB per interfering channel. The measured crosstalk levels of approximately -14.0 to -17.4 dB are therefore close to or better than the 0.5-dB criterion, but do not satisfy the more stringent 0.1-dB criterion for all channels. A simultaneous four-channel BER measurement would be required to determine the actual receiver-sensitivity penalty experimentally.

In addition to optical crosstalk, multi-channel receivers may be affected by electrical crosstalk arising from closely spaced electrodes and RF interconnects. Electrical crosstalk was not experimentally quantified in this work, and its impact therefore cannot be assessed quantitatively from the present measurements. In future implementations, GSG electrode configurations, improved grounding, and increased separation or shielding between adjacent RF interconnects could reduce capacitive and inductive coupling between the receiver channels.

Discussion on the impact of group delay. The phase response of the MZI lattice filter can influence the transmitted signal through group-delay variations across the modulation bandwidth. A constant group delay only introduces an overall temporal shift, whereas a non-uniform group delay may cause waveform distortion and inter-symbol interference. The phase response and group delay were not directly measured in this work and therefore cannot be quantitatively evaluated from the power transmission spectra alone. Nevertheless, the open eye diagrams and BER values below 10^{-4} obtained for all four channels indicate that the combined amplitude- and phase-response-induced distortion was acceptable at the demonstrated data rate of 32 Gbit/s.

3.5.4 Comparison with prior CWDM and WDM receivers

To contextualize the demonstrated receiver at the system level, Table 3.3 provides a concise comparison with representative SiN-based CWDM devices and Si-based WDM receivers reported in the literature. As summarized in the table, SiN platforms have predominantly been explored for passive CWDM wavelength-selective components, whereas receiver-level implementations are more commonly realized on Si using monolithically integrated Ge photodiodes or Ge/Si avalanche photodiodes (APDs) in combination with electronic front-ends.

The present work bridges this gap by demonstrating a fully integrated O-band CWDM receiver on a SiN platform enabled by micro-transfer printing of high-speed InGaAs/InP photodiodes, achieving four-channel 32 Gbit/s reception without the use of transimpedance amplifiers. Owing to the low thermo-optic coefficient of SiN, the use of a SiN platform is expected to reduce sensitivity to temperature variations compared to Si-based implementations, potentially alleviating the reliance on active thermal tuning.

In the present implementation, the overall footprint of the receiver is primarily determined by the waveguide routing rather than by the MZI lattice filters themselves, and could be further reduced through layout optimization. Compared to other heterogeneous integration approaches such as hybrid bonding or flip-chip

photodiode integration, micro-transfer printing offers improved scalability and flexibility for integrating multiple photodiodes on passive SiN photonic circuits, while maintaining a compact and system-level integrated receiver architecture.

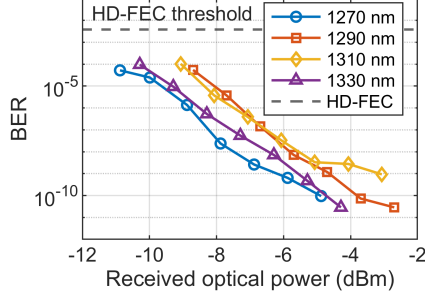


Figure 3.16: Back-to-back BER performance of the four channels as a function of received optical power for 32 Gbit/s NRZ operation, with the photodiodes biased at -2 V.

3.6 Conclusion

We have demonstrated a four-channel O-band CWDM receiver on a silicon nitride photonic platform integrating high-speed InGaAs/InP photodiodes enabled through micro-transfer printing. The cascaded MZI lattice filter demultiplexer provides low insertion loss and low crosstalk across the CWDM wavelength grid. The integrated photodiodes exhibit responsivities up to 0.72 A/W and a 33 GHz bandwidth, enabling 32 Gbit/s NRZ detection across all channels. Back-to-back measurements confirm open eye diagrams and BER levels below 10^{-4} at received optical powers above -11 dBm. These results validate the suitability of micro-transfer-printed photodiodes for high-speed SiN-based receivers and highlight the potential of this heterogeneous integration approach for future multi-wavelength short-reach optical interconnects. Future work will focus on co-integration with TIAs, as well as extending the architecture toward higher data rates and larger channel counts.

Table 3.3: Concise system-level comparison with representative SiN-based CWDM devices and silicon-based WDM receivers.

Work	PD integration	Electronics	Data rate / BW	Scope / Remarks
This work	μ TP InGaAs/InP	None	4×32 Gbit/s / 33 GHz	PIC-level CWDM receiver on SiN
Ref. [79]	–	–	–	Passive CWDM demultiplexer
Ref. [90]	–	–	–	Passive CWDM scalability study
Ref. [91]	Ge	WB TIA	4×50 Gbit/s / 50 GHz	Si-based WDM receiver
Ref. [92]	Ge/Si APD	External	25 Gbit/s / 25 GHz	Si-based DWDM receiver

4

Micro-transfer printing of InP SOAs on advanced silicon photonics platform for C-band pre-amplified receivers

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4.1 Introduction

Pre-amplified receivers, which combine a semiconductor optical amplifier (SOA) with a high-speed photodiode (PD), are particularly attractive for loss-limited communication systems, such as long-haul telecom or wafer-level photonic interposers with large-scale photonic fabrics and long waveguide routing [10]. In these scenarios, receiver sensitivity is a key performance metric, as it directly determines the available optical power budget and, consequently, the achievable system reach and scalability.

In practical optical links, the optical power available at the receiver is often limited by several factors. At the transmitter, the output power of integrated lasers is constrained by efficiency, thermal management, and reliability considerations. In addition, high-speed electro-optic modulators introduce non-negligible insertion loss, which reduces the launched optical power. Further losses are accumulated along the link due to passive components such as waveguides, fiber-to-chip couplers, wavelength multiplexers, and optical switches. In reconfigurable photonic systems, optical switches are commonly employed and can introduce additional insertion loss. As a result, the optical power reaching the receiver can be relatively low, particularly in high-speed links with limited power margins, creating a strong demand for receivers with enhanced sensitivity.

Silicon photonics has emerged as a leading platform for large-scale photonic integration, leveraging the well-established CMOS fabrication infrastructure. This enables high-throughput manufacturing and tight process control, while providing access to high-speed germanium (Ge) photodiodes integrated directly on silicon waveguides. The state of the art has demonstrated Ge photodiodes with 3-dB bandwidths exceeding 100 GHz [93], making silicon photonics highly attractive for high-speed receiver applications. However, silicon photonics cannot provide on-chip optical amplification, as silicon is an indirect bandgap material. This fundamental limitation prevents the monolithic realization of pre-amplified receivers on a silicon photonics platform.

As a consequence, most reported pre-amplified receivers rely on either discrete implementations [94] or full integration on indium phosphide (InP) platforms [95, 96]. In discrete solutions, external SOAs are combined with silicon photonic receivers through fiber-based or free-space coupling, which increases system complexity,

footprint, and packaging cost. Alternatively, pre-amplified receivers can be monolithically integrated on InP platforms, where both optical gain and high-speed photodetection are readily available. While InP-based integration offers excellent active device performance, it generally lacks the manufacturing scalability and cost advantages associated with CMOS-based silicon photonics.

Heterogeneous integration provides an attractive approach to overcome this limitation by combining the scalability of silicon photonics with the active functionality of III–V materials. Among the available heterogeneous integration techniques, micro-transfer printing (μ TP), a technology available under license from X-Celeprint, Ltd., has emerged as a scalable [22, 23] and back-end compatible [26] solution. μ TP enables the deterministic placement of pre-fabricated III–V devices onto a processed silicon photonics wafer, allowing III–V optical gain sections to be integrated without modifying the front-end CMOS process flow. This approach preserves the advantages of silicon photonics manufacturing while enabling on-chip optical amplification.

In this chapter, a C-band pre-amplified receiver implemented on imec's iSiPP200 silicon photonics platform using micro-transfer printing technology is presented. The receiver integrates a high-speed Ge photodiode from the process design kit (PDK), offering a bandwidth of 50 GHz, with an InP-based quantum-well SOA integrated in front of the PD using μ TP. The integrated SOA provides optical gain prior to photodetection, compensating for transmitter and link insertion losses, thereby improving the receiver sensitivity.

In pre-amplified receiver architectures, amplified spontaneous emission (ASE) noise generated by the SOA can degrade the signal-to-noise ratio (SNR) at the photodetector and limit overall receiver performance. To address this issue, a dual micro-ring resonator (DMRR) filter is integrated between the SOA and the PD, suppressing out-of-band ASE noise while maintaining low insertion loss for the signal of interest.

The work presented in this chapter demonstrates that micro-transfer printing enables the realization of compact, high-speed, and high-sensitivity pre-amplified receivers on a silicon photonics platform. By combining CMOS-compatible silicon photonics with III–V optical gain and integrated ASE filtering, this approach addresses the optical power limitations imposed by laser output constraints, transmitter insertion losses, and additional losses introduced by complex optical links, such as those including optical switches.

4.2 Working principle of pre-amplified receivers

4.2.1 Receiver sensitivity and system-level power limitation

In high-speed optical communication systems, receiver sensitivity is a key performance metric, as it determines the minimum received optical power required to achieve a target bit-error rate (BER). Datacenter optical interconnects typically require a post-FEC BER of approximately 10^{-12} to ensure reliable system operation. Similarly, Optical I/O (OIO) architectures, which enable chip-to-chip and package-level optical interconnects, generally target comparable system-level BERs on the order of 10^{-12} , aligning with datacom-class reliability requirements.

In this section, we present the fundamental concepts of receiver sensitivity, based on *Fiber-Optic Communication Systems* by Govind P. Agrawal [97].

With an optimally set decision threshold and assuming Gaussian noise statistics, the BER depends only on the Q parameter and is given by

$$\text{BER} = \frac{1}{2} \operatorname{erfc}\left(\frac{Q}{\sqrt{2}}\right) \approx \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}}, \quad (4.1)$$

where the parameter Q is defined as

$$Q = \frac{I_1 - I_0}{\sigma_1 + \sigma_0}. \quad (4.2)$$

Here, I_1 and I_0 denote the mean photocurrents corresponding to logical “1” and “0”, respectively, while σ_1 and σ_0 represent the standard deviations (RMS values) of the noise distributions at the two logic levels.

Fig. 4.1 illustrates the dependence of the BER on the Q parameter. Achieving a BER below 10^{-12} requires $Q > 7$. For a PIN photodiode receiver operating in the thermal-noise-dominated regime, the receiver sensitivity can be approximated as

$$(\bar{P}_{\text{rec}})_{\text{PIN}} \approx \frac{Q \sigma_T}{R}. \quad (4.3)$$

Here, σ_T denotes the RMS thermal noise current of the receiver, and R is the photodiode responsivity. The thermal noise variance is given by

$$\sigma_T^2 = \frac{4k_B T}{R_L} \Delta f. \quad (4.4)$$

In this expression, k_B is the Boltzmann constant, T is the absolute temperature, R_L is the equivalent load resistance, and Δf is the effective electrical noise bandwidth. For NRZ signaling, Δf is typically chosen to be on the order of half the bit rate.

Consequently, in the thermal-noise-limited regime, the receiver sensitivity degrades proportionally to the square root of the data rate.¹

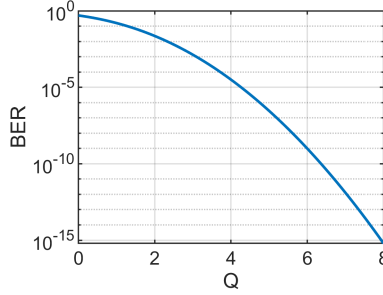


Figure 4.1: BER versus the Q parameter.

In practical links, the available received power is increasingly constrained by system-level loss mechanisms rather than by fiber attenuation alone. While fiber loss is negligible over typical intra-data center distances (for example, less than 0.5 dB over 2 km of single-mode fiber), the dominant penalties arise from active and passive components integrated within the transmitter, receiver, and intermediate optical network elements.

At the transmitter, the usable launched power is limited by both laser output constraints and modulator insertion loss. Commercial semiconductor lasers used in data-center and short-reach optical communication systems typically provide output powers ranging from a few milliwatts to several tens of milliwatts (approximately 0–15 dBm), while state-of-the-art integrated and externally packaged devices can reach output powers on the order of 50–130 mW (17–21 dBm), subject to thermal, efficiency, and reliability constraints [98,99]. High-speed electro-optic modulators typically introduce a few decibels of insertion loss, with reported values ranging from ~ 1 –3 dB for heterogeneous LN-based devices to several dB for silicon plasma-dispersion modulators, depending on the modulator architecture and the definition of loss (device-level vs. module-level) [98].

Additional losses arise from photonic integration and packaging, which are increasingly prevalent in modern transceivers. On-chip waveguide propagation loss, passive component losses (e.g., de-multiplexers), and fiber-to-chip coupling loss can together contribute several decibels of attenuation. Even with optimized edge or grating couplers, practical fiber-to-chip coupling losses of 1–3 dB per facet are common in deployed systems, and routing loss within complex PICs further adds to the total budget [100].

¹This scaling assumes that the same equivalent load resistance R_L is maintained irrespective of the bit rate.

Furthermore, wavelength-division multiplexing components and optical switching elements introduce non-negligible additional penalties. Wavelength (de)multiplexers typically contribute 1–3 dB of insertion loss, while optical circuit switches introduce losses ranging from approximately 1–2 dB for MEMS-based broadband switches to more than 10 dB for high-port-count or wavelength-selective switching fabrics [13]. As data-center networks increasingly adopt reconfigurable optical architectures to improve resource utilization and energy efficiency, such switching losses become unavoidable at the system level.

As a result of these cumulative effects, the total end-to-end optical loss in modern short-reach and intra-data center links can readily exceed 6–10 dB, even over modest fiber distances. This trend places stringent requirements on receiver sensitivity and motivates receiver architectures capable of operating under large loss budgets, particularly in systems that prioritize photonic integration, scalability, and reconfigurability over raw transmitter power.

4.2.2 Optical pre-amplification using optical amplifiers

An optical amplifier provides optical gain when the gain medium is pumped, either optically or electrically, to establish population inversion. Under this condition, an incident optical signal is amplified via stimulated emission.

In optical communication systems, optical amplifiers are typically used in three configurations, as illustrated in Fig. 4.2. These include in-line amplification, where amplifiers are inserted between fiber spans to compensate transmission loss, and transmitter-side booster amplification, where the amplifier is placed after the transmitter to increase the launch power. These configurations are widely used in long-haul and wavelength-division-multiplexed (WDM) systems.

The focus of this chapter is on the use of optical amplifiers as receiver-side preamplifiers. In this work, a semiconductor optical amplifier (SOA) is employed as the preamplifier due to its compact size, integrability, and compatibility with photonic integrated circuits. In this configuration, the optical amplifier is placed immediately before the photodetector to amplify weak incoming optical signals prior to optical-to-electrical conversion. By preamplifying the optical signal, the impact of receiver thermal noise is significantly reduced, and the overall noise performance becomes dominated by the noise introduced by the optical amplifier itself. As a result, the receiver sensitivity can be substantially improved.

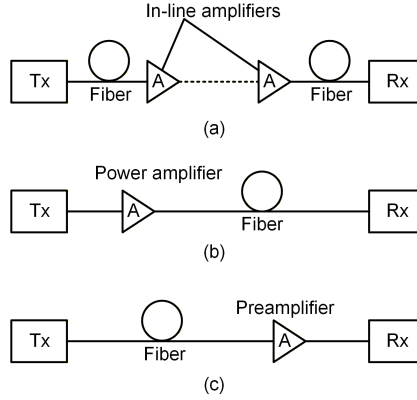


Figure 4.2: Typical applications of optical amplifiers in optical communication systems: (a) in-line amplification; (b) transmitter-side power amplification (booster); and (c) receiver-side preamplification. Adapted from [97].

4.2.3 Noise mechanisms

This section introduces the fundamental noise mechanisms in pre-amplified optical receivers, following [101, 102]. In particular, the analysis focuses on receivers employing an SOA as a preamplifier.

In addition to amplifying the signal, the SOA generates amplified spontaneous emission (ASE) noise. After photodetection, the total noise consists of receiver thermal noise, shot noise, and ASE-related beat noise. The ASE-related beat noise includes (i) signal–ASE beat noise, arising from beating between the amplified signal and the ASE field, and (ii) ASE–ASE beat noise, arising from mutual beating among ASE spectral components. The contribution of these noise components depends on the SOA gain G , the spontaneous emission factor N_{sp} , and the optical noise bandwidth B_o .

At low SOA gain, the contribution of ASE is weak and the receiver operates in the thermal-noise-limited regime; therefore, increasing the optical gain leads to an approximately linear improvement in sensitivity. As the gain is increased, ASE-related beat noise becomes dominant and the receiver transitions to an ASE-noise-limited regime. In this regime, further increases in SOA gain provide diminishing sensitivity improvement, and the achievable sensitivity is primarily determined by the ASE noise properties of the amplifier and the applied optical filtering.

The noise model used to describe the pre-amplified receiver is based on the work by N.A. Olsson [101]. In the following, the optical powers are expressed in photo-

current-equivalent (PCE) form, defined as the photocurrent that would be generated by detecting the optical power with a detector of unity quantum efficiency.

The PCE of ASE power within the optical bandwidth B_o is (see Table 4.1 for definitions of the symbols):

$$I_{\text{ASE}} = \frac{eP_{\text{ASE}}}{h\nu} = N_{\text{sp}} (G - 1) eB_o. \quad (4.5)$$

After square law detection in the receiver, the detected electrical signal power is:

$$S = (GI_s\eta_{\text{in}}\eta_{\text{out}}L)^2. \quad (4.6)$$

The noise terms are:

Shot noise:

$$N_{\text{shot}} = 2B_e e\eta_{\text{out}}L (GI_s\eta_{\text{in}} + I_{\text{ASE}}) \quad (4.7)$$

Signal-ASE beat noise:

$$N_{\text{s-ASE}} = 4GI_s\eta_{\text{in}}\eta_{\text{out}}^2 I_{\text{ASE}} L^2 B_e / B_o \quad (4.8)$$

ASE-ASE beat noise:

$$N_{\text{ASE-ASE}} = (I_{\text{ASE}}\eta_{\text{out}}L)^2 B_e (2B_o - B_e) / B_o^2 \quad (4.9)$$

Thermal noise:

$$N_{\text{th}} = I_{\text{th}}^2. \quad (4.10)$$

And the total noise is:

$$N_{\text{tot}} = N_{\text{shot}} + N_{\text{s-ASE}} + N_{\text{ASE-ASE}} + N_{\text{th}}. \quad (4.11)$$

For an amplitude-modulated NRZ signal with average input power P_{in} , 50% duty cycle, and extinction ratio r , the PCEs of the input power for a mark ($I_s(1)$) and a space ($I_s(0)$) are:

$$I_s(1) = eP_{\text{in}}2r / (h\nu(r + 1)) \quad (4.12)$$

$$I_s(0) = eP_{\text{in}}2 / (h\nu(r + 1)) \quad (4.13)$$

Using the definition of the Q parameter introduced in Eq. 4.2, the Q factor of the preamplified receiver can be expressed in terms of the detected electrical signal and noise powers as

$$Q = \frac{\sqrt{S(1)} - \sqrt{S(0)}}{\sqrt{N_{\text{tot}}(1)} + \sqrt{N_{\text{tot}}(0)}}. \quad (4.14)$$

Table 4.1: Definitions of symbols used in the preamplified receiver noise model

Symbol	Description
B_e	Electrical bandwidth of the receiver
B_o	Optical noise bandwidth (defined by the optical filter)
e	Elementary charge
G	Optical gain of the amplifier
$h\nu$	Photon energy
η_{in}	Input coupling efficiency of the amplifier
η_{out}	Output coupling efficiency of the amplifier
L	Optical transmission factor between amplifier and photodiode
I_s	PCE of the amplifier input signal power
$I_s(1)$	PCE of the amplifier input signal for logical “1” (mark)
$I_s(0)$	PCE of the amplifier input signal for logical “0” (space)
I_{ASE}	PCE of the amplified spontaneous emission (ASE) power
N_{sp}	Spontaneous emission factor of the amplifier
N_{shot}	Shot-noise power contribution
$N_{\text{s-ASE}}$	Signal–ASE beat-noise power contribution
$N_{\text{ASE-ASE}}$	ASE–ASE beat-noise power contribution
N_{th}	Receiver thermal-noise power contribution
N_{tot}	Total noise power at the receiver output
S	Detected electrical signal power
$S(1)$	Detected electrical signal power for logical “1”
$S(0)$	Detected electrical signal power for logical “0”
P_{in}	Average optical signal power at the amplifier input
P_{ASE}	Optical ASE power within bandwidth B_o
r	Extinction ratio of the NRZ signal
$\bar{P}_{\text{rec}}$	Receiver sensitivity

PCE = photo-current equivalent.

Derivation of the ASE-related beat noise terms

The ASE-related beat noise terms are derived in [101]. For simplicity, it is assumed that the optical amplifier is with unity coupling efficiency, uniform gain G , over an optical bandwidth B_o , and an input power of P_{in} at optical frequency ω_0 centered in the optical passband B_o .

The spontaneous emission power in the optical bandwidth B_o is given by:

$$P_{\text{sp}} = N_{\text{sp}}(G - 1)h\nu B_o. \quad (4.15)$$

The electric field E_{sp} , representing the spontaneous emission, is written as a sum of

cosine terms:

$$E_{sp}(t) = \sum_{k=-B_0/2\delta\nu}^{B_0/2\delta\nu} \sqrt{2N_{sp}(G-1)h\nu\delta\nu} \cdot \cos((\omega_0 + 2\pi k\delta\nu)t + \Phi_k) \quad (4.16)$$

where Φ_k is a random phase for each component of spontaneous emission. With

$$N_{sp}(G-1)h\nu = N_o \text{ and } \frac{B_o}{2\delta\nu} = M \quad (4.17)$$

the total electric field at the output of the amplifier is

$$E(t) = \sqrt{2GP_{in}} \cos(\omega_0 t) + \sum_{k=-M}^M \sqrt{2N_o\delta\nu} \cos((\omega_0 + 2\pi k\delta\nu)t + \Omega_k). \quad (4.18)$$

The photocurrent $i(t)$ generated by a unity quantum efficiency photodetector is proportional to the intensity:

$$\begin{aligned} i(t) = & GP_{in} \frac{e}{h\nu} \\ & + \frac{4e}{h\nu} \sum_{k=-M}^M \sqrt{GP_{in}N_o\delta\nu} \cos(\omega_0 t) \cos((\omega_0 + 2\pi k\delta\nu)t + \Phi_k) \\ & + \frac{2eN_o\delta\nu}{h\nu} \left[\sum_{k=-M}^M \cos((\omega_0 + 2\pi k\delta\nu)t + \Phi_k) \right]^2. \end{aligned} \quad (4.19)$$

The three terms in Eq. 4.19 represent, signal, signal–ASE beat noise, and ASE–ASE beat noise, respectively.

Examining the signal–ASE beat noise term first:

$$\begin{aligned} i_{s-ASE}(t) = & \frac{4e}{h\nu} \sum_{k=-M}^M \sqrt{GP_{in}N_o\delta\nu} \cos(\omega_0 t) \cos((\omega_0 + 2\pi k\delta\nu)t + \Phi_k) \\ = & \frac{2e}{h\nu} \sqrt{GP_{in}N_o\delta\nu} \sum_{k=-M}^M \cos(2\pi k\delta\nu t + \Phi_k). \end{aligned} \quad (4.20)$$

where terms $\sim \cos(2\omega_0 t)$ which average to zero have been neglected. For each frequency, $2\pi k\delta\nu$, in Eq. 4.20, the sum has two components but with a random phase. Therefore, the power spectrum of $i_{s-ASE}(t)$ is uniform in the frequency interval $0-B_0/2$ and has a density of:

$$N_{s-ASE} = \frac{4e^2}{(h\nu)^2} GP_{in}N_o \cdot \frac{1}{2} \cdot 2 = \frac{4e^2}{h\nu} P_{in}N_{sp}(G-1)G. \quad (4.21)$$

In term of the ASE–ASE beat noise, from Eq. 4.19 we have

$$\begin{aligned}
 i_{\text{ASE-ASE}}(t) &= 2N_o \frac{\delta\nu e}{h\nu} \left[\sum_{k=-M}^M \cos((\omega_o + 2\pi k\delta\nu)t + \Phi_k) \right]^2 \\
 &= 2N_o \frac{\delta\nu e}{h\nu} \left[\sum_{k=-M}^M \cos(\beta_k) \sum_{j=-M}^M \cos(\beta_j) \right]
 \end{aligned} \tag{4.22}$$

where

$$\begin{aligned}
 \beta_k &= (\omega_o + 2\pi k\delta\nu)t + \Phi_k, \\
 \beta_j &= (\omega_o + j2\pi\delta\nu)t + \Phi_j.
 \end{aligned} \tag{4.23}$$

Eq. 4.22 can be written:

$$\begin{aligned}
 i_{\text{ASE-ASE}}(t) &= 2N_o \frac{\delta\nu e}{h\nu} \sum_{k=-M}^M \sum_{j=-M}^M \frac{1}{2} \cos(\beta_k - \beta_j) \\
 &\quad + \frac{1}{2} \cos(\beta_k + \beta_j).
 \end{aligned} \tag{4.24}$$

The terms $\sim \cos(\beta_k + \beta_j)$ have frequencies $\sim 2\omega_0$ and average to zero. Rewriting Eq. 4.24 gives:

$$\begin{aligned}
 i_{\text{ASE-ASE}}(t) &= \frac{N_o \delta\nu e}{h\nu} \sum_{k=0}^{2M} \sum_{j=0}^{2M} \\
 &\quad \cdot \cos((k - j)2\pi\delta\nu t + \Phi_k - \Phi_j).
 \end{aligned} \tag{4.25}$$

The dc term is obtained for $k = j$ and there are $2M$ such terms:

$$I_{\text{ASE}}^{\text{dc}} = \frac{e}{h\nu} N_o \delta\nu 2M = N_{\text{sp}}(G - 1)eB_o. \tag{4.26}$$

Organizing the terms in Eq. 4.25 according to their frequencies we get:

<u>frequency</u>	<u># terms</u>	
$-(2M - 1)\delta\nu$	1	
$\vdots$	$\vdots$	
$-l\delta\nu$	$2M - l$	
$\vdots$	$\vdots$	
$-\delta\nu$	$2M - 1$	
$\delta\nu$	$2M - 1$	
$\vdots$	$\vdots$	
$l\delta\nu$	$2M - l$	
$\vdots$	$\vdots$	
$(2M - 1)\delta\nu$	1	

(4.27)

The terms with same absolute frequency but of opposite sign add in phase. Therefore, the power spectrum of the ASE–ASE beat noise extends from 0 to B_0 with a triangular shape and a power density near dc of

$$N_{\text{ASE-ASE}} = \frac{2^2 N_o^2 \delta \nu e^2}{(h\nu)^2} \left(\frac{B_o}{\delta \nu} - 1 \right) \cdot \frac{1}{2} = 2N_{\text{sp}}^2 (G - 1)^2 e^2 B_o. \quad (4.28)$$

4.2.4 Sensitivity simulation of a preamplified receiver

Based on the noise mechanisms discussed above, a theoretical sensitivity analysis of a preamplified receiver is carried out. The simulation assumes a 32 Gbit/s NRZ modulation format at the wavelength of 1.55 μm . For this data rate, the corresponding electrical bandwidth is taken as $B_e = 16$ GHz, corresponding to 0.5 times the bit rate. The optical amplifier parameters are adopted from a previously reported micro-transfer-printed III–V-on-silicon C-band SOA demonstrated by B. Haq *et al.* [103]. The simulated power coupling efficiencies between the silicon and III–V waveguides are $\eta_{\text{in}} = \eta_{\text{out}} = 0.93$.

The spontaneous emission factor N_{sp} is related to the SOA noise figure F_n by

$$F_n = 2N_{\text{sp}} \frac{G - 1}{G} \approx 2N_{\text{sp}}, \quad (4.29)$$

where G denotes the optical gain. For a partially coupled SOA, in which the optical mode is distributed over the hybrid Si/III–V waveguide in the gain section—as is the case for the SOA considered in this chapter—a noise figure of 7.0 dB is reported at a low on-chip input power of -24 dBm. This corresponds to a spontaneous emission factor of $N_{\text{sp}} = 2.5$.

The optical loss between the SOA and the photodiode is mainly attributed to the optical filter and is taken to be 0.66 dB for the ring filter used in the device, corresponding to a transmission factor of $L = 0.86$. In addition, a baseline receiver sensitivity of -9.5 dBm at a bit-error rate (BER) of 10^{-12} is assumed, based on large-signal measurements performed on a reference germanium photodiode.

The extinction ratio r of the modulated signal is assumed to be 20 dB, consistent with the performance of the MZM modulator used in the experiments.

Using the parameters defined above, the receiver sensitivity is calculated as a function of the amplifier gain, as shown in Fig. 4.3. At low amplifier gains, the receiver operates in the thermal-noise-limited regime, and the sensitivity therefore improves by approximately 1 dB for every decibel of gain. As the gain increases, signal–spontaneous and spontaneous–spontaneous beat noise become dominant, causing the sensitivity improvement to gradually saturate. Beyond a certain gain

level of 30 dB, further increases in gain no longer result in a noticeable sensitivity enhancement.

Figure 4.3 also illustrates the impact of the optical filter bandwidth on the receiver sensitivity. The ultimate sensitivity limit is achieved when the optical bandwidth satisfies $B_o = 2B_e = 32$ GHz, corresponding to $B_o = 0.26$ nm at a wavelength of 1.55 μm . Under these conditions, the sensitivity reaches a value of -32.8 dBm. For the optical filter implemented in the device discussed in this chapter, the bandwidth is 1.45 nm, which yields a sensitivity nearly identical to the best-case scenario.

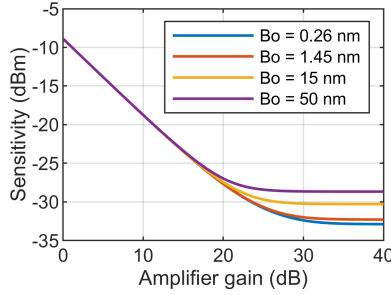


Figure 4.3: Simulated sensitivity of a preamplified receiver versus amplifier gain.

Calculated for $B_e = 16$ GHz, $N_{sp} = 2.5$, $\eta_{in} = \eta_{out} = 0.93$, $L = 0.86$, $r = 100$, $\lambda = 1.55$ μm , and a base receiver sensitivity of -9.5 dBm for BER of 10^{-12} .

The corresponding power penalty is further evaluated as a function of the optical filter bandwidth for different amplifier gain levels, as shown in Fig. 4.4. The power penalty is defined as the increase in receiver sensitivity relative to the sensitivity limit at a given gain. At low gain, the receiver remains thermal-noise-limited, and the penalty is largely independent of ASE-related beat noise and, consequently, of the optical filter bandwidth. At higher gain levels, ASE-related beat noise becomes the dominant noise contribution, and reducing the optical filter bandwidth becomes increasingly effective in improving the receiver sensitivity and thus reducing the power penalty.

Finally, Fig. 4.5 shows the simulated sensitivity as a function of the spontaneous emission factor N_{sp} for amplifier gains of 14, 20, and 35 dB. At low gain, the impact of spontaneous emission is weak, and the sensitivity is primarily limited by receiver thermal noise, resulting in only a minor dependence on N_{sp} . In contrast, at high gain, ASE-related beat noise dominates, and the use of a low-noise amplifier with a reduced spontaneous emission factor becomes critical for achieving optimal receiver sensitivity.

Overall, these simulations show that the sensitivity of a preamplified receiver is

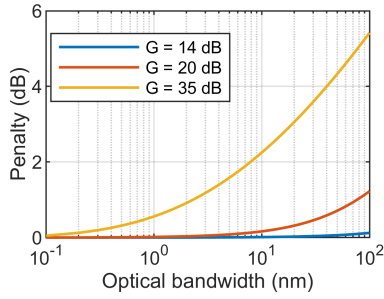


Figure 4.4: Simulated sensitivity penalty of a preamplified receiver versus optical filter bandwidth, using the same amplifier parameters as in Fig. 4.3.

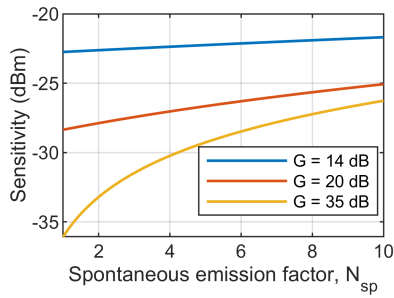


Figure 4.5: Simulated sensitivity of a preamplified receiver versus the spontaneous emission factor N_{sp} of the amplifier, using the same amplifier parameters as in Fig. 4.3.

fundamentally limited by thermal noise at low gain and by ASE-related beat noise at high gain. Consequently, both the optical filter bandwidth and the SOA noise figure play a critical role in determining the ultimate receiver sensitivity in high-gain operation.

4.3 Heterogeneous III–V-on-Si SOAs

Heterogeneous III–V-on-Si semiconductor optical amplifiers (SOAs) provide on-chip optical gain by combining III–V active materials with silicon photonic waveguides. This approach compensates for the lack of optical gain in silicon while preserving the scalability and integration density of silicon photonics.

III–V-on-Si SOAs provide compact, on-chip optical amplification and are essential building blocks for optical interconnects, optical I/O systems, and large-scale integrated photonic circuits. Their performance directly impacts system-level metrics such as link budget, receiver sensitivity, and energy efficiency.

4.3.1 Figures of merit

The performance of an SOA is characterized by several key figures of merit. The small-signal optical gain G characterizes the amplification provided by the SOA in the unsaturated regime. It is defined as the ratio between output and input optical power:

$$G = \frac{P_{\text{out}}}{P_{\text{in}}}. \quad (4.30)$$

In decibel units:

$$G_{\text{dB}} = 10 \log_{10}(G). \quad (4.31)$$

A sufficiently high gain is required to compensate on-chip and coupling losses and to suppress receiver thermal noise in pre-amplified configurations.

At the wavelength of maximum optical gain, the SOA gain factor G varies with the input power P_{in} as:

$$G = G_0 \frac{1 + P_{\text{in}}/P_s}{1 + G_0 P_{\text{in}}/P_s}, \quad (4.32)$$

where P_s is the material gain saturation power, which characterizes the intrinsic saturation behavior of the gain medium.

The input 3-dB saturation power $P_{\text{in},s}$ is defined as the input power at which the gain is reduced by 3 dB from its unsaturated value, i.e., $G = G_0/2$. From Eq. 4.32,

this yields

$$P_{\text{in},s} = \frac{P_s}{G_0 - 2}. \quad (4.33)$$

In addition to input saturation, SOAs are often characterized by the saturation output power P_{sat} , defined as the output power at which the gain is reduced by 3 dB from its small-signal value. A commonly used simplified model expresses the gain as a function of the output power P_{out} as

$$G = \frac{G_0}{1 + P_{\text{out}}/P_{\text{sat}}}, \quad (4.34)$$

where P_{out} is the SOA output power.

The noise figure F_n characterizes the noise added by the SOA relative to an ideal noiseless amplifier. It is defined as the ratio between the input and output SNRs,

$$F_n = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}}. \quad (4.35)$$

The noise figure of the SOA can be calculated from the recorded spectrum attributed to Signal-ASE beat noise.

$$F_n = \frac{2\lambda^3}{Gc^2h} \frac{P_{\text{ASE}}}{\delta\lambda} + \frac{1}{G}. \quad (4.36)$$

The on-chip P_{ASE} is measured in a wavelength range of $\delta\lambda$ for a given input power using the OSA.

The wall-plug efficiency (WPE) of the SOA is defined as the ratio between the net optical power gain and the electrical power consumed by the gain section, and is given by

$$\text{WPE} = \frac{P_{\text{out}} - P_{\text{in}}}{I_{\text{gain}} V_{\text{gain}}} \times 100\%. \quad (4.37)$$

where P_{out} and P_{in} denote the output and input optical powers, respectively, and I_{gain} and V_{gain} are the bias current and voltage applied to the SOA gain section.

4.3.2 Review of previous work

Depending on the integration strategy, previous demonstrations of heterogeneous III–V-on-silicon semiconductor optical amplifiers (SOAs) can be broadly classified into three categories: flip-chip bonded III–V SOAs, die-to-wafer or wafer-to-wafer bonded III–V SOAs, and micro-transfer-printed III–V-on-silicon SOAs.

Flip-chip bonding is a hybrid integration approach in which prefabricated III–V SOA dies are attached onto silicon photonic circuits with high alignment accuracy.

A lateral alignment accuracy within $\pm 1 \mu\text{m}$ can be achieved, while in the vertical direction the alignment of waveguide heights can be controlled within $\pm 0.5 \mu\text{m}$ by precisely defining the thickness of the individual layers in both the SOA and silicon photonics chips. As a result, a total excess coupling loss below 2.2 dB has been reported. Using this approach, Fujitsu demonstrated in-line optical amplification on silicon photonics platforms, achieving net on-chip gains exceeding 15 dB for a single SOA and approximately 9.5 dB net gain in a 4×4 silicon photonic switch, enabling effective loss compensation in large-scale circuits [104]. While flip-chip bonding benefits from mature III–V processing and the use of known-good dies, its scalability is limited by the alignment complexity and the relatively large footprint.

Die-to-wafer and wafer-to-wafer bonding techniques integrate III–V gain material onto silicon wafers prior to device definition, enabling compact III–V-on-silicon devices with lithographically defined alignment and efficient optical coupling between SOAs and silicon photonic waveguides. Using direct bonding, Davenport *et al.* reported SOAs exhibiting a small-signal gain of 25.5 dB and an input saturation power of 4.25 dBm, with a 3-dB gain bandwidth of 65 nm [105]. Adhesive bonding using divinylsiloxane-benzocyclobutene (DVS-BCB) has also enabled high-performance devices. Van Gasse *et al.* demonstrated a BCB-bonded III–V-on-silicon SOA achieving a small-signal gain of 27 dB and a saturation output power exceeding 17 dBm [106]. Although these approaches provide excellent optical performance, they typically require III–V processing on silicon wafers, which increases process complexity and poses challenges for compatibility with existing silicon photonics foundries.

Micro-transfer printing is another heterogeneous integration technique that enables the parallel transfer of fully processed III–V SOA thin films, referred to as “coupons”, onto silicon photonic wafers. Recently demonstrated micro-transfer-printed III–V-on-silicon SOAs exhibit on-chip gains exceeding 15 dB and saturation output powers above 10 mW in the C-band [103]. Owing to its compatibility with back-end silicon photonics processing and its scalability for wafer-level manufacturing [22, 23], micro-transfer printing provides an attractive route for integrating optical gain into large-scale silicon photonic circuits. The work presented in this thesis follows this integration approach.

4.4 Receiver design and simulation

This section presents the design of a C-band pre-amplified receiver implemented on the imec’s silicon photonics platform and enhanced by the heterogeneous integration of an InP-based SOA using micro-transfer printing technology. A schematic cross-section of the receiver is shown in Fig. 4.6. By placing an SOA in front of the

photodetector, optical amplification is achieved prior to photodetection, leading to an improved receiver sensitivity.

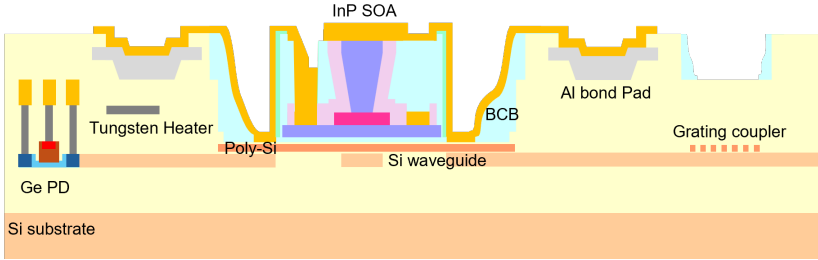


Figure 4.6: Schematic cross-section of the C-band pre-amplified receiver with transfer-printed InP SOA on imec's iSiPP200 silicon photonics platform.

The receiver is realized on imec's iSiPP200 silicon photonics platform, which provides a comprehensive and mature set of building blocks for high-speed optical interconnects. The platform offers low-loss silicon waveguides optimized for C-band operation, together with passive components such as grating couplers, power splitters, and wavelength-selective filters.

In addition to passive photonic components, the iSiPP200 platform integrates high-speed germanium photodiodes (Ge PDs) [76]. A schematic and a cross-sectional TEM image of a vertical p-i-n photodiode (VPIN) are shown in Fig. 4.7(a) and (b), respectively.

The photodiode performance is summarized in Fig. 4.8, demonstrating performance comparable to the baseline iSiPP50G platform. The RF S_{21} response of the Ge photodiode, shown in Fig. 4.8(a), exhibits a 3-dB bandwidth exceeding 50 GHz. The measured responsivity in both the C- and O-bands is close to the target value of 0.9 A/W and remains above the lower specification limit of 0.6 A/W. In addition, the dark current is below 25 nA and 150 nA at bias voltages of -1 V and -2 V, respectively.

Metal interconnect layers together with aluminum bond pads provide electrical access to the integrated devices. Thermal tuning functionality is implemented using tungsten resistive heaters, enabling precise control of the optical phase and coupling conditions within the photonic circuit.

The GDS layout of the imec iSiPP200 tape-out design is shown in Fig. 4.9. This design fully exploits the capabilities of the advanced silicon photonics platform by adopting a range of process design kit (PDK) components, including C-band grating couplers, a 50 GHz germanium photodiode (Ge PD), aluminum bond pads, and

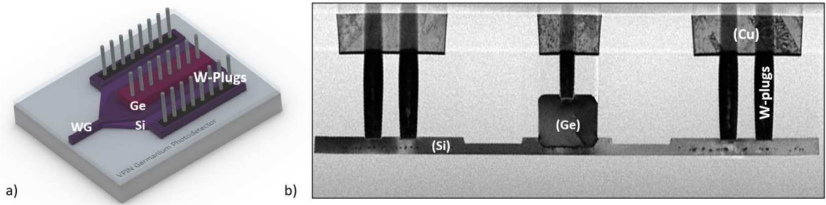


Figure 4.7: (a) Schematic of the 50-GHz vertical p-i-n germanium photodiode (VPIN) implemented on the iSiPP200 platform. (b) TEM cross-section image of the VPIN. Reproduced from [76].

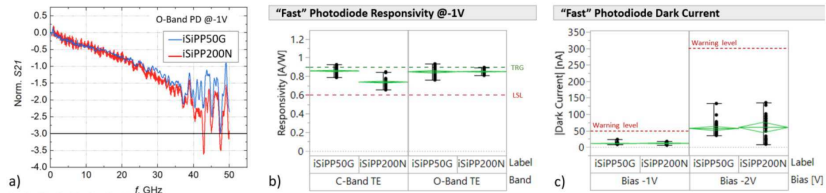


Figure 4.8: Performance comparison between iSiPP50G and iSiPP200 photodiodes. (a) RF S_{21} response of the Ge photodiodes at a bias voltage of -1 V. (b) Photodiode responsivity measured at a bias voltage of -1 V. (c) Dark current of the photodiodes at bias voltages of -1 V and -2 V. Reproduced from [76].

single-mode silicon strip waveguides optimized for C-band operation. A tunable ring filter is implemented between the SOA and the Ge PD using integrated tungsten resistive heaters, enabling thermal tuning of the optical response. For SOA micro-transfer printing, alignment markers are placed around the target integration region to facilitate accurate positioning of the SOA coupon. At the SOA integration site, an opening is etched into the back-end oxide following the LPASS definition of the process flow, creating a partially opened recess above the silicon waveguide. This region is subsequently further processed to fully open the back-end, thereby providing direct access to the silicon waveguide surface for SOA transfer printing.

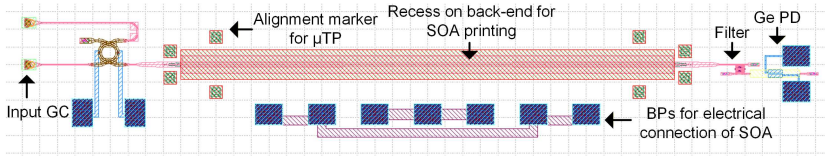


Figure 4.9: GDS layout of the imec iSiPP200 tape-out design for the C-band pre-amplified receiver.

To enable optical pre-amplification on the silicon photonics platform, an InP-based SOA is heterogeneously integrated onto the silicon photonic circuit using micro-transfer printing technology. The epitaxial layer structure of the SOA employed in this work is summarized in Table 4.2. The device is realized on a III–V heterostructure grown on an InP substrate and incorporates a multi-quantum-well (MQW) active region optimized for optical gain in the C-band.

Two MQW zone variants are available in the epitaxial design, targeting photoluminescence peaks around 1500 nm and 1550 nm, respectively, which correspond to laser emission wavelengths near 1525 nm and 1575 nm. In this work, the longer-wavelength variant is selected.

The MQW active region is embedded within AlGaInAs separate confinement heterostructure (SCH) layers to ensure strong optical confinement and efficient carrier transport. Electrical injection is provided by p-type and n-type cladding layers based on InP and GaInAsP. In addition, sacrificial AlInAs and GaInAs layers are incorporated in the epitaxial stack to facilitate device release and transfer during the micro-transfer printing process.

As illustrated in Fig. 4.6, the back-end oxide is locally opened to allow the InP SOA coupon to be printed on top of the silicon waveguide. A 160 nm polycrystalline silicon (poly-Si) layer is introduced on top of the silicon waveguide, resulting in an effective total silicon thickness of 375 nm. This intermediate poly-Si layer enables efficient optical mode coupling between the silicon waveguide and the transfer-

Table 4.2: III–V SOA epitaxial layer stack comprising two multi-quantum-well (MQW) zone variants designed to achieve photoluminescence (PL) peaks around 1500 nm and 1550 nm.

Layer	Layer type	Material	Thickness [nm]	Doping level [cm^{-3}]	Dopant
26	Cap P	InP	100	$\sim 1 \times 10^{19}$	Zn
25	Contact P	GaInAs (lattice matched)	200	$\sim 2.5 \times 10^{19}$	Zn
24	Transition P	GaInAsP ($\lambda_g = 1170$ nm)	20	$\sim 6 \times 10^{18}$	Zn
23	Cladding P	InP	1000	$1\text{--}2 \times 10^{18}$	Zn
22	Cladding P	InP	500	$\sim 5 \times 10^{17}$	Zn
21	Etch stop	GaInAsP ($\lambda_g = 1170$ nm)	25	$\sim 5 \times 10^{17}$	Zn
20	Transition	(Al _{0.9} Ga _{0.1}) _{0.47} In _{0.53} As	25	–	–
19	SCH	(Al _{0.7} Ga _{0.3}) _{0.47} In _{0.53} As	25	–	–
8×6	Barrier	(Al _{0.45} Ga _{0.65}) _{0.51} In _{0.49} As	10	–	–
7×6	Well	(Al _{0.25–0.20} Ga _{0.75–0.80}) _{0.3} In _{0.7} As	6	–	–
6	Barrier	(Al _{0.45} Ga _{0.65}) _{0.51} In _{0.49} As	10	–	–
5	SCH	(Al _{0.7} Ga _{0.3}) _{0.47} In _{0.53} As	25	–	–
4	Transition	(Al _{0.9} Ga _{0.1}) _{0.47} In _{0.53} As	25	1×10^{18}	Si
3	Cladding N	InP	200	2×10^{18}	Si
2	Sacrificial	GaInAs (lattice matched)	50	nid	–
1	Sacrificial	AlInAs (lattice matched)	500	$\sim 1 \times 10^{18}$	Si
0	Buffer layer	InP	150	nid	–

printed InP SOA through a partially coupled adiabatic taper structure. Robust integration is ensured by using a benzocyclobutene (BCB) bonding layer. The p- and n-type contacts of the SOA are connected to neighboring aluminum bond pads through the metallization layers of the silicon photonics platform, allowing electrical redistribution and straightforward interfacing with external driving circuitry.

4.4.1 Partially coupled Si–III–V adiabatic taper

To enable efficient optical coupling between the silicon photonic circuit and the transfer-printed InP SOA, a partially coupled Si–III–V adiabatic taper structure is employed. A schematic illustration of the taper geometry and layer configuration is shown in Fig. 4.10. The coupling scheme is based on a vertically stacked waveguide system, consisting of a silicon strip waveguide, an intermediate polycrystalline silicon (poly-Si) layer, and the III–V waveguide of the SOA coupon.

The silicon waveguide has a thickness of 215 nm and a width of 0.45 μm . It is adiabatically widened to 0.8 μm over a 25 μm -long taper section. A 160 nm-thick poly-Si layer is introduced above the silicon waveguide, forming a composite Si/poly-Si waveguide with an effective thickness of 375 nm. This intermediate layer serves as a mode bridge between the silicon waveguide and the III–V active region, enabling efficient and smooth optical coupling from Si to III–V and subsequently back to Si.

The transition from the Si waveguide to the Si/poly-Si waveguide starts with a 0.17 μm -wide poly-Si tip placed on top of the silicon waveguide. This structure is then gradually expanded into a poly-Si slab above a 3 μm -wide silicon waveguide through a 100 μm -long adiabatic transition. Subsequently, a III–V taper is implemented above the Si/poly-Si waveguide, starting from a 0.6 μm -wide III–V tip. The multi-quantum well (MQW) layer and the p-InP layer are then gradually widened to 7 μm and 4 μm , respectively. The electric field intensity distributions of the fundamental TE mode at several key structural transition points are also shown in Fig. 4.10, illustrating the gradual transfer of the optical mode from the silicon waveguide into the MQW active region.

The electrical field magnitude of the full taper structure along the cross section is shown in Fig. 4.11, including the Si waveguide to Si/poly-Si waveguide taper and the III–V taper. The optical mode initially resides in the silicon waveguide and is partially transferred into the III–V waveguide through the Si-to-Si/poly-Si transition and the subsequent III–V taper section. The electric field intensity gradually decreases along the propagation direction owing to the expansion of the optical mode. A zoomed-in view of the III–V taper region is presented in Fig. 4.11, where the gradual redistribution of optical power into the MQW region can be

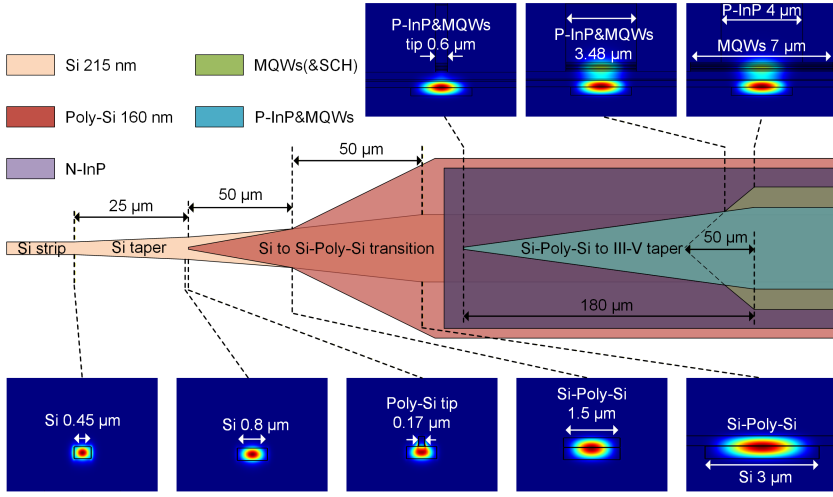


Figure 4.10: Schematic illustration of the partially coupled Si-III-V adiabatic taper, showing the evolution of the electric field intensity distribution of the fundamental TE mode along the taper. The SOA coupon design follows Ref. [107].

clearly observed.

As shown in Fig. 4.11(b), the simulated mode evolution indicates the presence of multimode excitation in the III-V waveguide amplifier. Such multimode excitation can induce ripple in the SOA gain curve and may therefore degrade the stability of the receiver performance. This effect can become more pronounced when there is lateral misalignment between the Si/poly-Si waveguide and the III-V taper during μ TP, since imperfect alignment can increase reflection and coupling to higher-order modes. To reduce multimode excitation, a longer and more adiabatic III-V taper is desirable. In addition, improving the μ TP alignment accuracy can further suppress reflection and unwanted higher-order-mode excitation, leading to a smoother SOA gain response.

To evaluate the alignment tolerance of the coupling scheme, the fundamental TE mode energy density distributions under different lateral misalignment conditions between the silicon waveguide and the III-V SOA coupon are simulated, as shown in Fig. 4.12. Even for lateral offsets up to $2\ \mu\text{m}$, the optical mode remains well confined within the MQW region, indicating a high degree of robustness against placement errors during the micro-transfer printing.

The quantitative impact of lateral misalignment on coupling performance is summarized in Fig. 4.13, which shows both the mode confinement factor in the MQWs

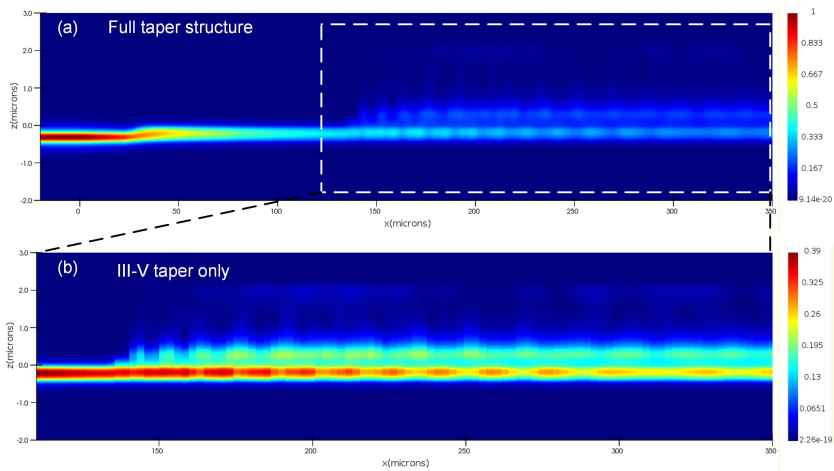


Figure 4.11: Electric field magnitude plots of (a) the full taper structure, including the Si waveguide to Si/poly-Si waveguide taper and the III-V taper, and (b) a zoomed-in view of the III-V taper along the cross section.

and the optical transmission of the Si–III–V taper. The mode confinement factor decreases gradually from approximately 12.4% at perfect alignment to about 10.9% at a misalignment of $2\ \mu\text{m}$. Meanwhile, the transmission remains above 92% across the entire misalignment range. These results demonstrate that the partially coupled adiabatic taper provides not only efficient optical coupling but also relaxed alignment tolerance.

4.4.2 Dual micro-ring resonator filter

The GDS layout of the dual micro-ring resonator (DMRR) filter is shown in Fig. 4.14. The device is implemented on a silicon-on-insulator (SOI) platform with a 211.4 nm thick silicon device layer. The access waveguides are tapered from $0.45\ \mu\text{m}$ to $0.5\ \mu\text{m}$ in width. The structure consists of two identical micro-rings with a straight coupling section of $9.4\ \mu\text{m}$ and an inner diameter of $9.05\ \mu\text{m}$ for the bent waveguide sections. The coupling gaps are 155 nm between the bus waveguides and the rings, and 290 nm between the two rings. For thermal tuning, tungsten micro-heaters are integrated on top of the micro-rings, enabling post-fabrication resonance alignment and dynamic wavelength tuning.

Figure 4.15 shows the simulation results of the directional couplers used in the DMRR filter. Figures 4.15(a) and (b) present the simulated optical power distri-

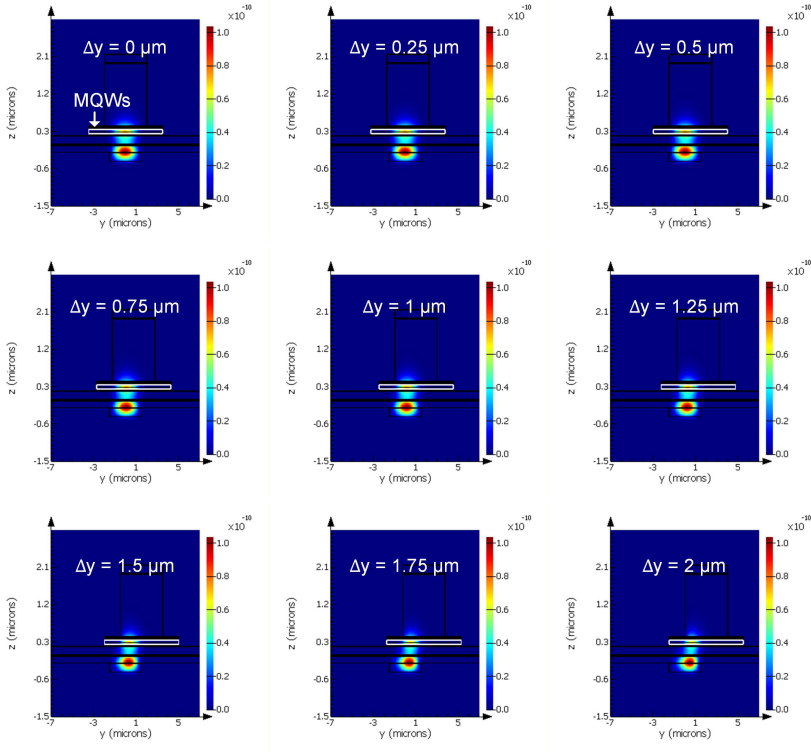


Figure 4.12: Fundamental TE mode energy density distributions for different lateral misalignment conditions.

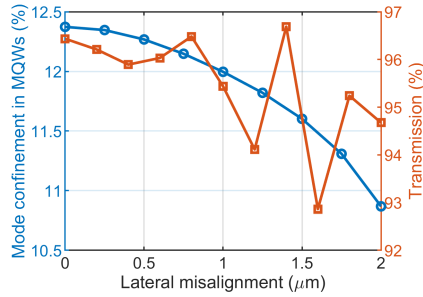


Figure 4.13: Dependence of the mode confinement in the MQWs and the transmission of the Si-III-V taper on the lateral misalignment between the silicon waveguide and the III-V SOA coupon.

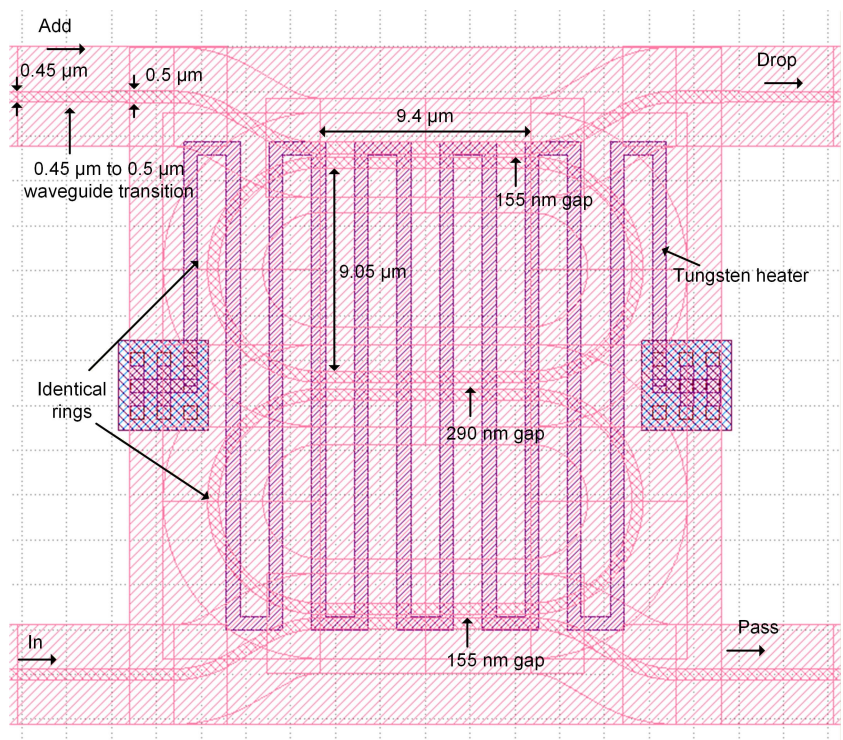


Figure 4.14: GDS layout of the dual micro-ring resonator filter.

butions when the fundamental transverse-electric (TE) mode is launched into the top-left port of the ring-to-ring directional coupler and the bus-waveguide-to-ring directional coupler, respectively, at a wavelength of 1550 nm. The results indicate weak coupling between the two rings, whereas a relatively stronger coupling is achieved between the bus waveguide and the ring.

The wavelength dependence of the coupling characteristics is summarized in Figs. 4.15(c) and (d), which show the cross-coupling coefficient κ and the corresponding power cross-coupling coefficient k as functions of wavelength for the ring-to-ring and bus-waveguide-to-ring directional couplers, respectively. Both couplers exhibit a moderate dependence on wavelength across the C-band. At a wavelength of 1550 nm, the extracted cross-coupling coefficients are 0.245 for the ring-to-ring directional coupler and 0.671 for the bus-waveguide-to-ring directional coupler. These values are used in the subsequent circuit-level simulations to model the filter response.

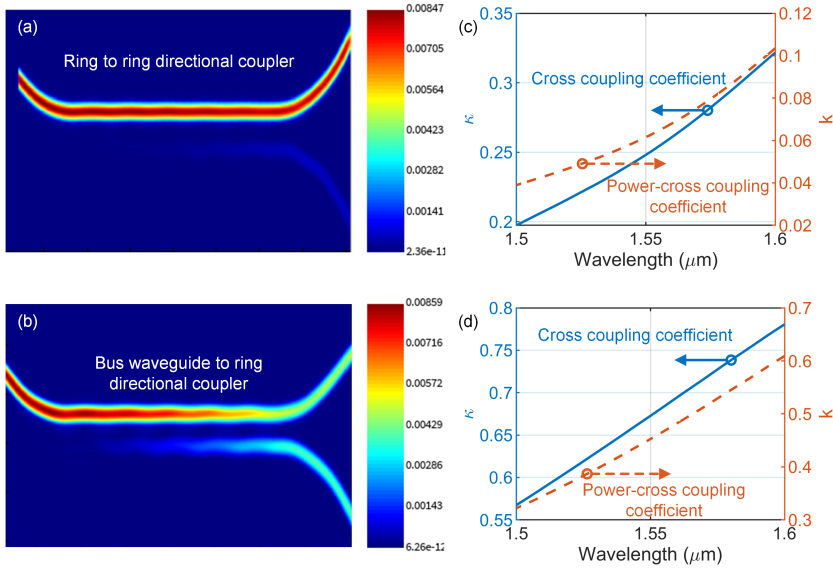


Figure 4.15: Simulation results of the directional couplers used in the dual micro-ring resonator filter. (a)–(b) Simulated optical power distributions when the fundamental TE mode is launched into the top-left port of the ring-to-ring directional coupler and the bus-waveguide-to-ring directional coupler at a wavelength of 1550 nm. (c)–(d) Wavelength dependence of the cross-coupling coefficient κ and the power cross-coupling coefficient k for the ring-to-ring and bus-waveguide-to-ring directional couplers, respectively.

Based on the extracted coupling parameters, a circuit-level simulation of the DMRR

filter is implemented in Ansys Interconnect, as shown in Fig. 4.16. The model consists of cascaded directional couplers and waveguide segments representing the two identical micro-rings and the bus waveguides. The optical path lengths of the ring sections are chosen to match the physical layout, while the coupling coefficients are set according to the electromagnetic simulations of the individual couplers.

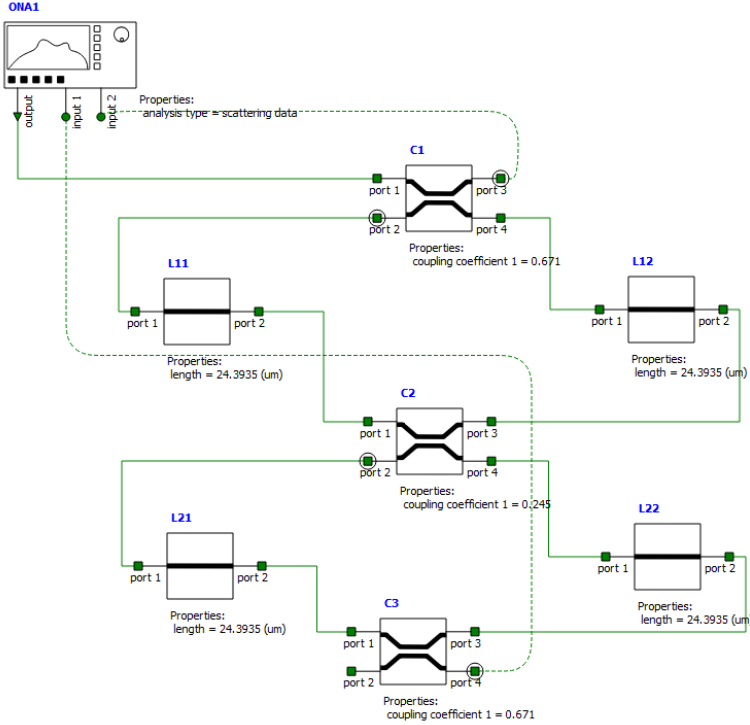


Figure 4.16: Simulation setup of the dual micro-ring resonator filter implemented in Ansys Interconnect.

The simulated transmission spectra at the pass and drop ports of the DMRR filter are presented in Fig. 4.17. At a wavelength of approximately 1550 nm, the drop-port spectrum shows an extinction ratio of 17 dB, a 3-dB bandwidth of 2.8 nm, and a free spectral range of 11.7 nm.

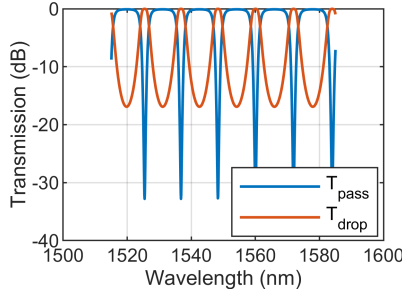


Figure 4.17: Simulated transmission spectra at the pass and drop ports of the dual micro-ring resonator filter.

Design considerations and tolerance of the dual micro-ring resonator filter

The dual micro-ring resonator filter (DMRR) consists of two identical coupled rings. The ring round-trip length is primarily determined by the required free spectral range (FSR), while the coupling coefficients are determined from directional-coupler simulations.

The bus-waveguide-to-ring coupling is chosen to be relatively strong, i.e., the filter operates in an over-coupled regime. This reduces the loaded- Q factor, increases the 3-dB bandwidth, and makes the filter less sensitive to small resonance shifts. A broader passband is also beneficial for high-speed signals, because it reduces the penalty caused by filter-induced amplitude distortion. In addition, the broader resonance makes it easier to align the two coupled rings during thermal tuning.

The ring-to-ring coupling coefficient mainly determines the passband shape and flatness. If the ring-to-ring coupling is too weak, the filter response becomes more sensitive to the resonance mismatch between the two rings and the passband flatness degrades. If the coupling is too strong, excessive resonance splitting can distort the passband. Therefore, the ring-to-ring coupling is selected to obtain a flat-band response with a sufficiently large 3-dB bandwidth and high extinction ratio.

In the implemented design, relatively long coupling sections are used. This allows the coupling gap to be made larger, which relaxes the fabrication requirement and makes the layout compatible with the design-rule constraints.

Fabrication tolerances affect the filter in two main ways. First, variations in the waveguide width, thickness, and coupling gap change the coupling strength. This changes the loaded- Q factor, 3-dB bandwidth, insertion loss, passband flatness, and extinction ratio. Second, variations in the ring length or effective index shift the

resonance wavelength. A common resonance shift of both rings can be compensated by thermal tuning. However, a differential resonance shift between the two rings cannot be fully corrected by a single heater. Such a mismatch can degrade the flat-top response, increase passband ripple, increase the drop-port insertion loss, and reduce the extinction ratio.

The present design uses a single heater to tune the coupled-ring filter. This approach is simple and robust, because both rings are tuned together and only one control signal is required. However, it does not allow independent compensation of fabrication-induced resonance mismatch between the two rings. Independent heaters on the individual rings would provide additional degrees of freedom and could improve the passband symmetry, reduce ripple, and optimize the drop-port insertion loss and extinction ratio. The drawback is increased layout complexity, larger electrical routing overhead, higher power consumption, and possible thermal crosstalk between the heaters. Therefore, there is a trade-off between filter optimization capability and system simplicity. For this proof-of-concept receiver, the single-heater design was selected because the low- Q , broad flat-band filter already provides sufficient tolerance and bandwidth for the demonstrated high-speed operation.

4.5 SOA integration on the iSiPP200 platform

4.5.1 SOA coupon fabrication

The InP SOAs used in this work were fabricated into coupons on a III–V source wafer prior to their heterogeneous integration onto the silicon photonics platform at III–V Lab. The overall fabrication flow has been reported in detail in [108]. Here, only the key steps relevant to this work are summarized.

As illustrated in Fig. 4.18, the fabrication starts from an InP epitaxial wafer incorporating a multi-quantum-well active region and a sacrificial release layer. The SOA devices are first defined through mesa etching, quantum well patterning, and formation of n-type electrical contacts, resulting in fully functional devices on the source wafer, except for the p-type contacts.

Following device definition, additional processing steps are carried out to enable micro-transfer printing. Engineered SiN_x tethers are introduced to mechanically anchor the SOAs to the source substrate while providing controlled breaking points during pick-up. The devices are then encapsulated with a thick BCB layer for planarization. Subsequently, the BCB is etched back to the top of the SOA mesa, and the SiN_x covering the contact regions is removed to allow p-type metal deposition.

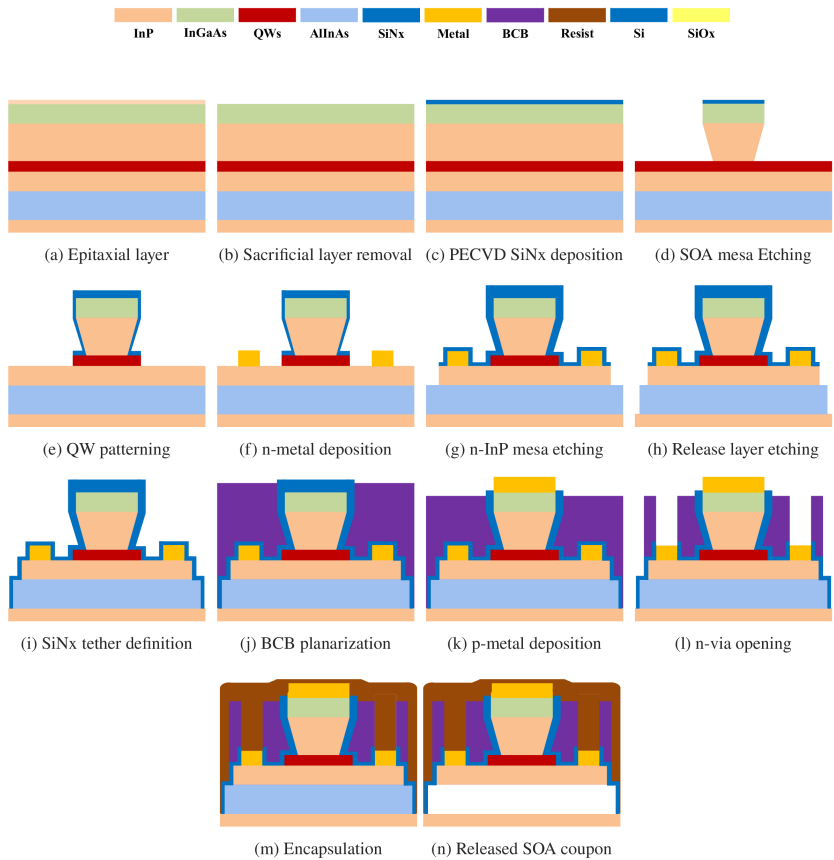


Figure 4.18: Process flow of SOA device fabrication on the source InP substrate. Reproduced from [108].

Prior to release, a layer of TI35E photoresist is spin-coated and patterned to encapsulate the devices and reinforce the tethers. Selective etching of the sacrificial release layer is then performed to suspend the SOAs, thereby forming transferable coupons.

After release, individual SOA coupons with a typical footprint of approximately $40\text{ }\mu\text{m}$ in width and $0.8\text{--}1.2\text{ mm}$ in length remain suspended on the III–V source wafer. As shown in Fig. 4.19, the coupons are arranged in dense arrays. These released SOA coupons serve as the starting point for the micro-transfer-printing-based integration process described in the following section.

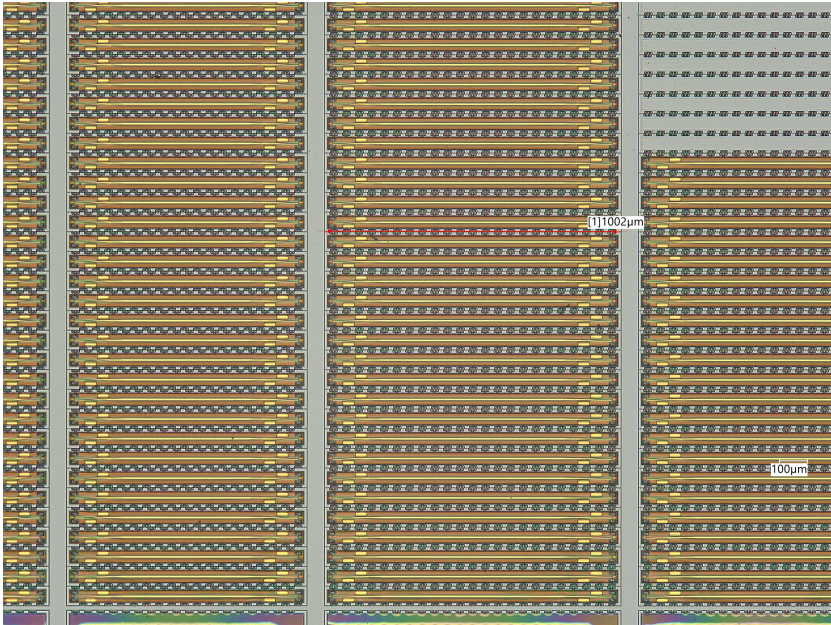


Figure 4.19: Microscope image of fabricated SOA coupons on the III–V source wafer after release, ready for micro-transfer printing.

4.5.2 Process flow for the micro-transfer-printing-based integration of InP SOAs on the iSiPP200 platform

The integration of InP SOAs onto the iSiPP200 silicon photonics platform is realized using a micro-transfer printing (μTP) approach that is fully compatible with the back-end processing of the silicon photonics wafer. The complete process flow is illustrated in Fig. 4.20.

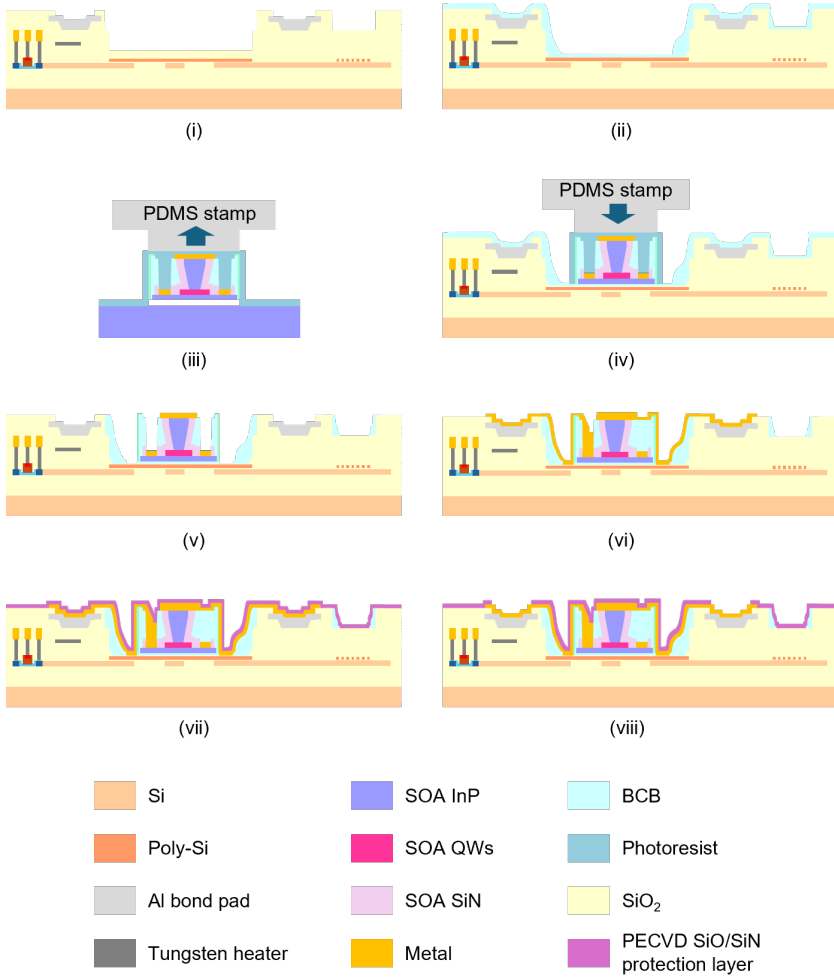


Figure 4.20: Process flow for the micro-transfer-printing-based integration of InP SOAs on the iSiPP200 platform. (i) Tape-out silicon photonics wafer. (ii) Removal of the remaining oxide on top of the poly-Si layer and spray coating of a uniform BCB bonding layer. (iii) Pick-up of an InP SOA coupon from the source wafer using a PDMS stamp. (iv) Alignment and micro-transfer printing of the SOA coupon onto the target silicon waveguide. (v) Removal of the photoresist on the printed coupon and thermal curing of the BCB bonding layer. (vi) Final metallization to define the electrical contacts to the SOA. (vii) Deposition of a PECVD SiO/SiN protection layer for mechanical reinforcement of the device against vibration-induced damage during dicing. (viii) Opening of contact vias through the protection layer to enable electrical access.

The process starts from a fully fabricated iSiPP200 tape-out wafer incorporating silicon waveguides, poly-Si coupling layers, tungsten heaters, grating couplers, high-speed Ge photodiodes, and electrical routing. In the SOA integration region, an opening is etched into the back-end-of-line (BEOL) stack according to the predefined LPASS layer in the tape-out, resulting in a recess of approximately $4\text{ }\mu\text{m}$. The remaining dielectric stack is then selectively removed to expose the underlying poly-Si layer, which enables efficient optical coupling between the silicon waveguide and the III–V gain section. This step is performed using an in-house fabrication process that combines reactive ion etching (RIE) and buffered oxide etching (BOE), yielding a total recess depth of approximately $6.5\text{--}7\text{ }\mu\text{m}$ and a residual surface topography below 30 nm . The remaining surface topography is located on the poly-Si layer and originates from imperfections in the tape-out process.

Following the recess opening, a BCB adhesive bonding layer is spray-coated onto the sample. Compared with conventional spin coating, spray coating provides a more uniform BCB thickness within the deep recess. Based on process optimization, a target BCB thickness of approximately $50\text{--}80\text{ nm}$ in the recessed region is employed to enhance surface adhesion for reliable transfer printing and to ensure stable bonding, while preserving efficient optical coupling between the silicon waveguide and the III–V SOA. A short reflow bake is applied prior to printing to further improve surface planarity and bonding uniformity.

The prepared silicon photonics sample is subsequently loaded onto a micro-transfer-printing tool as the printing target, while the pre-fabricated SOA coupon sample serves as the printing source. A PDMS stamp is used to pick up individual SOA coupons from the source substrate. Each SOA coupon, with a typical length of $0.8\text{--}1.2\text{ mm}$, is then precisely aligned to the target silicon waveguide under the microscope of the printing tool and printed into the recessed region on the silicon photonics wafer. The thin BCB layer acts as the adhesive interface between the SOA and the silicon substrate.

The alignment during SOA transfer printing is critical. Misalignment between the SOA coupon and the underlying coupling waveguide reduces the coupling efficiency and may increase optical discontinuities and internal reflections. This can lead to additional coupling loss, gain ripple, and reduced device-to-device reproducibility.

After printing, post-processing steps are performed to complete the bonding and device integration. The photoresist encapsulation on the SOA coupon is removed using an oxygen plasma dry etch, followed by a thermal curing step of the BCB layer to establish a mechanically stable and reliable bonding interface.

Subsequently, photolithography and RIE are employed to locally remove residual BCB from the Al bond pads. During the RIE process, etching residues can form on the Al surfaces. To ensure low-resistance electrical connections, a post-etch cleaning step using the etching-residue removal chemical IK73 is applied for several tens of seconds to a few minutes.

Final metallization is then carried out to define the p- and n-contacts of the SOA and to connect them to the neighboring bond pads on the silicon photonics. To ensure reliable electrical interconnection of the printed SOA on the iSiPP200 silicon photonics platform, several metallization schemes were evaluated with particular attention to metal coverage across the back-end oxide recess used for SOA integration. This recess introduces a vertical step of approximately $7\text{ }\mu\text{m}$. Table 4.3 summarizes the investigated metallization options, including different gold thickness distributions and deposition methods. Owing to the relatively large total gold thickness of $1\text{ }\mu\text{m}$, all evaluated schemes provide sufficient metal continuity for electrical routing, including the single-step Univex evaporation process. Hybrid approaches employing angled evaporation or a sputtered gold top layer were nevertheless considered to further enhance metal conformity along the back-end oxide sidewalls and improve process robustness.

To complement the schematic process flow shown in Fig. 4.20, optical microscope images of selected key integration stages are presented in Fig. 4.21. Figure 4.21(a) shows the tape-out silicon photonic integrated circuit of a pre-amplified receiver, in which the back-end-of-line stack is locally opened to expose the underlying Si/poly-Si coupling layer for SOA integration. After micro-transfer printing and BCB curing, the SOA is firmly bonded to the silicon photonics substrate, as shown in Fig. 4.21(b). The integrated SOA after final metallization, defining the electrical interconnections to the silicon photonics platform, is shown in Fig. 4.21(c). A close-up view of the SOA–silicon waveguide coupling region is presented in Fig. 4.21(d), confirming accurate alignment and intimate coupling between the III–V gain section and the underlying silicon waveguide.

After completion of the final metallization, the PIC can be characterized using electrical probing and optical fiber coupling through the metal bond pads and grating couplers, respectively. However, further dicing is required when edge couplers are employed or when the PIC is to be subsequently assembled with electronic components, such as modulator drivers or TIAs, on a printed circuit board (PCB). The mechanical vibration induced during the dicing process can lead to device failure; for instance, open-circuit behavior was observed in some SOAs after dicing.

To improve the mechanical robustness of the integrated devices during subsequent handling and dicing, a protective dielectric stack is deposited on top of the PIC using

Table 4.3: Metallization options for SOA integration on the iSiPP200 silicon photonics platform

Option	Adhesion Layer	Gold Thickness and Deposition Technique	Rationale / Process Note
1	40 nm Ti (evaporation)	1000 nm Au (Univex evaporation)	Single-step thick Au deposition; line-of-sight evaporation may result in limited coverage on high-aspect-ratio back-end oxide recess sidewalls ($\sim 7 \mu\text{m}$ step height).
2	40 nm Ti (evaporation)	200 nm Au (e-gun evaporation at 30° with wafer rotation) + 800 nm Au (Univex evaporation)	Angled and rotated e-gun deposition improves metal coverage on the back-end oxide recess sidewalls compared to normal-incidence evaporation.
3	40 nm Ti (evaporation)	800 nm Au (Univex evaporation) + 200 nm Au (Univex sputtering)	Sputtered Au top layer provides a more distributed particle flux, improving metal conformity and continuity along the back-end oxide recess sidewalls ($\sim 7 \mu\text{m}$ step height).

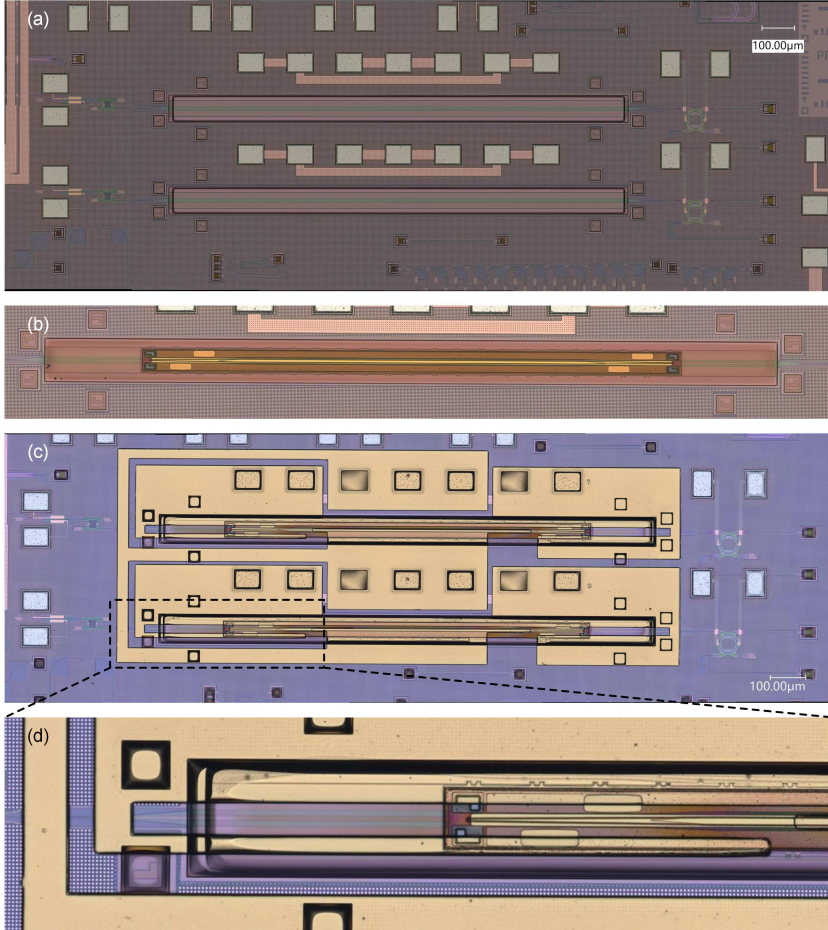


Figure 4.21: Optical microscope images illustrating key stages of the micro-transfer-printing-based integration of InP SOAs on the iSiPP200 platform: (a) tape-out silicon photonic integrated circuit of a pre-amplified receiver, showing the locally opened back-end region exposing the underlying Si/poly-Si coupling layer; (b) printed SOA after BCB curing and removal of the photoresist encapsulation; (c) integrated SOA after final metallization defining the electrical interconnections; (d) close-up view of the coupling region between the SOA and the silicon waveguide.

PECVD. This protection layer consists of a 1 μm -thick SiO_2 layer followed by a 200 nm SiN layer, providing sufficient mechanical reinforcement while maintaining balanced intrinsic film stress. The dielectric stack enhances the overall mechanical stability of the chip and mitigates vibration-induced damage during the dicing process.

Following the deposition of the protection layer, contact vias are opened by lithography and dry etching to enable electrical access for subsequent wire bonding. Prior to wire bonding, IK 73 is applied again to remove surface contamination and native oxides from the exposed aluminum bond pads, thereby improving bond quality and reliability.

The deposition of the SiO_2/SiN protection stack is performed in a PECVD chamber at a temperature of 270 $^\circ\text{C}$ and requires a total processing time of approximately 1 h 20 min. In addition to providing mechanical protection, the thermal exposure during this process induces an annealing effect on the metallization. As a consequence, a reduced differential resistance of the SOAs is observed, which directly contributes to better electrical efficiency and lower power consumption.

This behavior is clearly reflected in the measured I–V characteristics shown in Fig. 4.22(a). After PECVD processing, the device exhibits a lower operating voltage at a given injection current compared to the pre-PECVD case, indicating a reduced differential resistance. The extracted differential resistance, presented in Fig. 4.22(b), confirms this trend, showing a systematically lower dV/dI over the entire operating current range after PECVD. At an injection current of 120 mA, the device voltage is reduced from 2.2 V before PECVD to 1.7 V after PECVD, corresponding to a decrease in electrical power consumption from 264 mW to 204 mW, i.e., a power saving of approximately 60 mW (about 23%). Consistently, the differential resistance at 120 mA decreases from approximately 10 Ω to about 7 Ω . The presented characteristics are representative of measurements obtained from multiple devices.

This micro-transfer-printing-based integration process enables the heterogeneous integration of high-performance InP SOAs onto an advanced silicon photonics platform without modifying the front-end silicon photonics process, while maintaining excellent optical alignment, electrical performance, and mechanical stability.

4.6 Characterization and discussion

In this section, the characterization results of the key integrated components of the pre-amplified receiver are presented, including the high-speed germanium

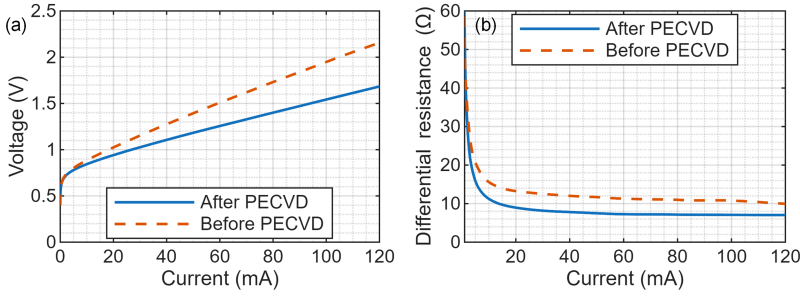


Figure 4.22: (a) Measured current–voltage (I – V) characteristics of a representative SOA before and after PECVD processing. (b) Differential resistance extracted from the I – V characteristics. The shown results are representative of multiple measured devices.

photodiode, the dual micro-ring resonator filter, and the heterogeneously integrated SOA. In addition, high-speed reception experiments of 30 Gbit/s NRZ signals are reported for different SOA gain conditions. During all measurements, the sample was mounted on a thermoelectric cooler (TEC) and maintained at a temperature of 20 °C.

4.6.1 Characterization of integrated components

Germanium photodiode

The germanium photodiode used in this work is provided by the imec iSiPP200 PDK, and its performance has been previously discussed in Section 4.4. For completeness, the static characteristics of the photodiode are characterized here using a reference Ge PD fabricated on the same tape-out wafer, including the current–voltage (I – V) characteristics and the responsivity in the C-band. The measured results are shown in Fig. 4.23(a) and (b), respectively. From the I – V characteristics, a low dark current of approximately 10 nA is observed at a reverse bias voltage of -2 V. At the same bias voltage, the Ge PD exhibits a responsivity of 1.2 A/W at a wavelength of 1550 nm, which is in good agreement with the value specified in the PDK documentation.

Dual micro-ring resonator filter

The design of the dual micro-ring resonator filter (DMRR) has been described in detail in Section 4.4.2. Figure 4.24 shows an optical microscope image of the

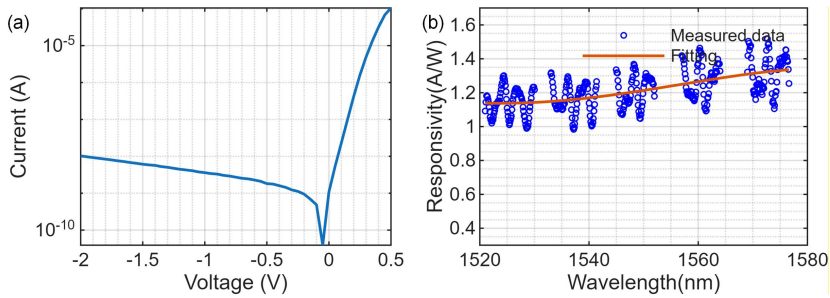


Figure 4.23: Static characteristics of a reference germanium photodiode: (a) measured current–voltage (I – V) characteristics; (b) measured responsivity over the C-band at a reverse bias of -2 V.

fabricated DMRR device.

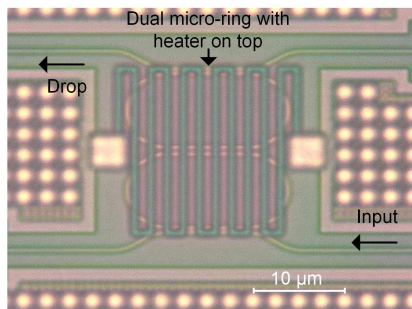


Figure 4.24: Optical microscope image of a dual micro-ring resonator filter.

The optical performance of the DMRR was characterized using a reference device fabricated on the same tape-out wafer. The measured transmission spectrum at the drop-port is shown in Fig. 4.25. Around a wavelength of $1550\ \text{nm}$, the device exhibits an insertion loss of $0.7\ \text{dB}$, a free spectral range (FSR) of $11.83\ \text{nm}$, a 3-dB bandwidth of $1.45\ \text{nm}$, and an extinction ratio exceeding $25\ \text{dB}$.

The thermal tuning characteristics of the reference DMRR using an integrated heater are presented in Fig. 4.26. Figures 4.26(a)–(g) show the measured drop-port transmission spectra for applied heater voltages of 0 , 1 , 2 , 3 , 4 , 5 , and $6\ \text{V}$, respectively. Although the absolute optical input power was not explicitly recorded, it was maintained constant throughout the wavelength and voltage sweeps. When a voltage of $6\ \text{V}$ is applied, the resonance wavelength can be tuned over more than one FSR.

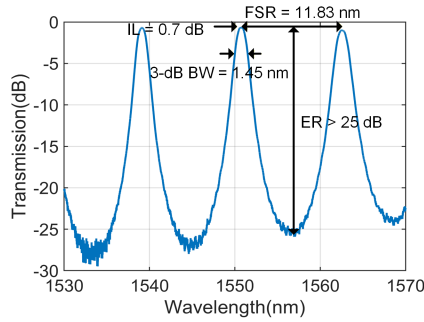


Figure 4.25: Measured drop-port transmission spectrum of a reference dual micro-ring resonator filter.

Figure 4.26(h) shows the current–voltage (I–V) characteristic of the heater. At an applied voltage of 6 V, the measured current is 16.4 mA, corresponding to a power consumption of 98.4 mW.

Semiconductor optical amplifier

The performance of the semiconductor optical amplifiers (SOAs) was further characterized. The current–voltage (I–V) characteristics have already been discussed in Section 4.5.2. This section focuses on the small-signal on-chip optical gain of the SOAs.

The optical output power after the SOA was monitored using the integrated Ge photodetector (PD), and the SOA gain was extracted from the measured photocurrent. The DMRR filter located between the SOA and the Ge PD was not thermally tuned, i.e., the integrated heater was not actuated during the measurement. Therefore, the intrinsic drop-port transmission spectrum in the C-band was first characterized to identify the resonance peak wavelengths. The SOA gain was then measured at these peak wavelengths to ensure maximum transmission to the Ge PD and accurate gain extraction.

Fig. 4.27 presents the small-signal on-chip gain of the SOA as a function of the bias current, measured at the resonance peak wavelengths of the DMRR filter. The three peak wavelengths are identified at 1551.6 nm, 1563.6 nm, and 1575.4 nm. At a bias current of 115 mA, the corresponding on-chip gains are 13.7 dB, 14.5 dB, and 14.6 dB, respectively. Among all the fabricated devices, the SOA presented here exhibits the highest on-chip gain.

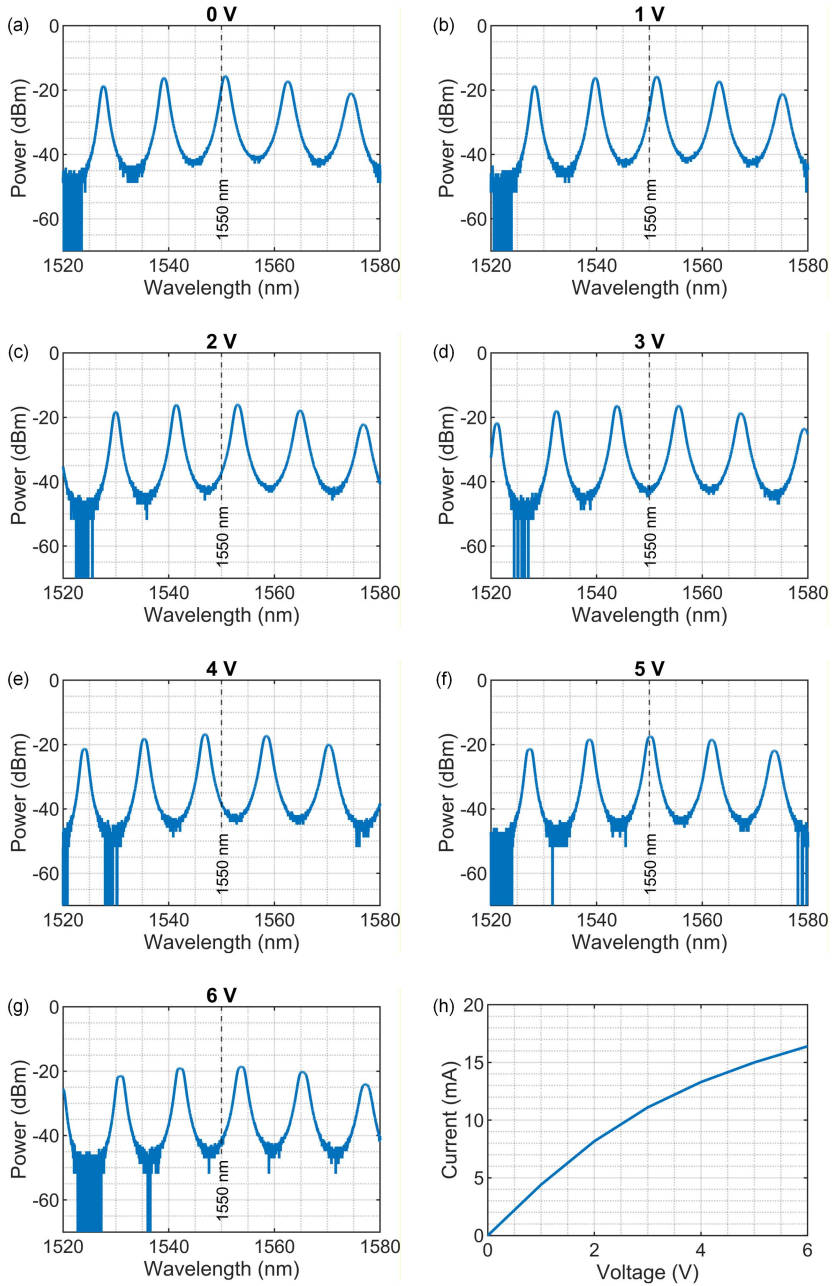


Figure 4.26: Thermal tuning behavior of the dual micro-ring resonator filter. (a)–(g) Measured drop-port transmission spectra for applied heater voltages of 0, 1, 2, 3, 4, 5, and 6 V, respectively. The optical input power was kept constant during the measurements. (h) Current–voltage (I – V) characteristic of the integrated heater.

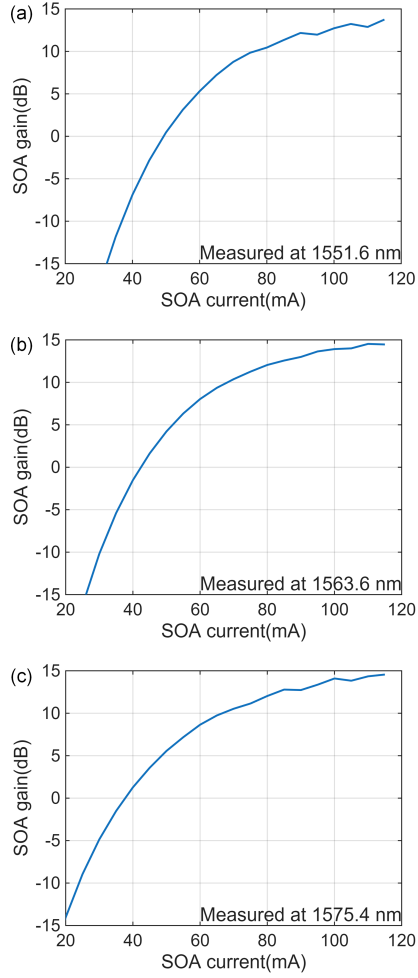


Figure 4.27: SOA small-signal on-chip gain as a function of the bias current, measured at the resonance peak wavelengths of the dual micro-ring resonator (DMRR) filter: (a) 1551.6 nm; (b) 1563.6 nm; (c) 1575.4 nm. The presented SOA exhibits the highest on-chip gain among all fabricated devices.

Discussion: limitations in SOA gain and noise figure

The SOA gain can be increased by increasing the optical confinement factor in the MQW region, increasing the injection current, or increasing the SOA length. However, these approaches introduce several trade-offs. A larger confinement factor increases the modal gain and improves the small-signal gain, but it also reduces the saturation output power and can enhance ASE. A longer SOA can provide higher gain, but at the cost of increased propagation loss, higher current consumption, and stronger self-heating. At high injection currents, thermal saturation and gain roll-off can further limit the achievable gain. In addition, taper loss, III–V waveguide propagation loss, and internal reflections directly reduce the net gain and can lead to gain ripple, instability, or parasitic lasing.

The trade-off between full coupling and partial coupling has been reported in micro-transfer-printed III–V-on-Si C-band SOAs [103], as summarized in Table 4.4. In a full-coupling design, the optical mode is fully transferred from the Si waveguide to the III–V waveguide, resulting in a higher confinement factor in the MQW region and therefore a higher small-signal gain. In contrast, in a partial-coupling design, part of the mode remains in the underlying Si waveguide, leading to a lower modal gain but improved saturation behavior and alignment tolerance. For example, B. Haq *et al.* reported a maximum small-signal gain of 23 dB and saturation power of 9.2 mW for a full-coupling SOA, compared with 17 dB and 15 mW for a partial-coupling SOA. Therefore, full coupling is attractive for maximizing small-signal gain, whereas partial coupling is beneficial when higher saturation power and more robust high-power operation are required.

The noise figure is also affected by the coupling scheme. Although the full-coupling SOA provides a higher small-signal gain, the stronger overlap with the MQW region can also increase the ASE coupled into the guided mode and make the device more susceptible to gain saturation. In the reported C-band micro-transfer-printed SOAs, the estimated on-chip noise figure of the full-coupling SOA was 8.6 dB at 1565 nm with an on-chip input power of -24 dBm, increasing to 9.54 dB at 0 dBm. In comparison, the partial-coupling SOA showed a lower noise figure of 7.0 dB at 1548 nm with an on-chip input power of -24 dBm, increasing to 8.6 dB at 0 dBm [103]. This comparison shows that the SOA noise figure is determined by a trade-off between modal gain, ASE generation, and saturation behavior.

Another possible route to reduce the SOA noise figure is to use a quantum-dot active region. Compared with quantum-well SOAs, quantum-dot SOAs can provide stronger carrier confinement and a reduced spontaneous emission factor, which may suppress ASE and enable a lower noise figure. However, their practical implementation also depends on the available material platform, emission wavelength,

Table 4.4: Comparison between full-coupling and partial-coupling SOA designs [103].

Design	Main advantage	Main limitation	Reported example
Full coupling	Higher optical confinement in the MQW region; higher small-signal gain	Lower saturation power; stronger sensitivity to ASE	23 dB small-signal gain; 9.2 mW saturation power
Partial coupling	Better saturation behavior and alignment tolerance	Lower modal gain and lower small-signal gain	17 dB small-signal gain; 15 mW saturation power

gain bandwidth, output saturation power, and compatibility with the heterogeneous integration process. In addition, passive loss, internal reflections, and thermal management should still be optimized to further improve the effective noise figure.

4.6.2 High-speed NRZ signal reception experiment

The high-speed data reception performance of the pre-amplified receiver was characterized through non-return-to-zero (NRZ) eye diagram measurements. Among all fabricated devices, one representative device was selected for this experiment.

Small-signal on-chip gain of the SOA in the reception experiment

During the measurement, the input laser wavelength was fixed at 1550.3 nm, corresponding to the resonance wavelength of the DMRR filter. The measured small-signal on-chip gain of the SOA at this wavelength is shown in Fig. 4.28. The transparency current of the SOA is approximately 54 mA. When biased at 95 mA, the SOA provides an on-chip gain of 8.1 dB. The SOA current was limited to 95 mA in the data-transmission experiment because the measured gain showed little further improvement at higher injection currents. This gain roll-over is likely attributed to increased self-heating at high current, which raises the active-region temperature and limits the material gain.

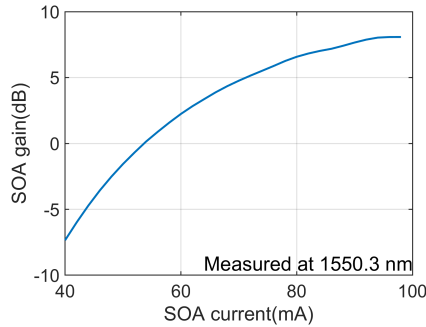


Figure 4.28: SOA gain of the device which was used in the eye diagram test, as a function of the bias current. Measured at the wavelength of 1550.3 nm, aligned with the resonance wavelength of the DMRR filter of the pre-amplified receiver.

Eye diagram experiment setup

Fig. 4.29 illustrates the experimental setup for the high-speed large-signal eye diagram measurement. A 30 Gbit/s non-return-to-zero (NRZ) signal with a pseudo-random binary sequence (PRBS) of length $2^7 - 1$ was generated at a wavelength of 1550.3 nm. The optical carrier was provided by a C-band tunable laser (Santec TSL-510) and modulated using a 40 Gbit/s Mach-Zehnder modulator (Photline MX-LN-40) packaged with an RF driver amplifier (Photline DR-DG-40). The electrical driving signal was generated by an arbitrary waveform generator (AWG, Keysight M9502A).

The modulated optical signal was amplified by an erbium-doped fiber amplifier (EDFA, Keopsys CEFA-C-HG-SM-50-B130-FA-FA) to compensate for the total link loss. A tunable optical filter was subsequently used to suppress amplified spontaneous emission (ASE) noise. A variable optical attenuator (VOA) was employed to control the optical power launched into the photonic integrated circuit (PIC). The signal was then split by a 50:50 optical splitter, with one branch directed to the PIC and the other to a power monitor.

On-chip, the optical signal was first amplified by the SOA and subsequently detected by the integrated Ge photodetector (PD). The SOA was biased using a Keithley source meter which was set to current mode. The Ge PD was electrically probed using a GS probe (MPI T40A-GS0100) connected to a bias-tee (SHF BT65R-A). A reverse bias of -2 V was applied to the Ge PD using a Keithley source meter. The generated RF signal was amplified by an RF amplifier (SHF S807) and finally measured using a sampling oscilloscope (Agilent DCA-X 86100D).

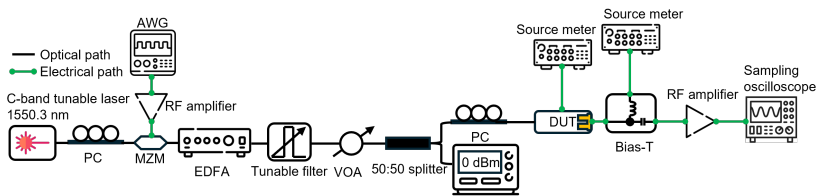


Figure 4.29: Experimental setup for the 30 Gbit/s large-signal NRZ eye diagram measurement of the pre-amplified receiver.

Discussion on eye diagrams and BER performance

The high-speed performance of the pre-amplified receiver operated at a Ge PD bias voltage of -2 V was evaluated and compared with that of a reference Ge PD without SOA pre-amplification, as shown in Fig. 4.30.

Figure 4.30(a) presents the measured 30 Gbit/s NRZ eye diagrams at a received optical power of -13.2 dBm. For the reference Ge PD, the eye diagram exhibits a signal-to-noise ratio (SNR) of 3.43. When the integrated SOA is biased at 62 mA, corresponding to an on-chip gain of 2.8 dB, the SNR improves to 5.95. By further increasing the SOA current to 95 mA (8.1 dB on-chip gain), the SNR increases to 7.95, indicating a significant enhancement in signal quality due to optical pre-amplification.

The bit-error-rate (BER) performance under different SOA bias currents is shown in Fig. 4.30(b). For the reference Ge PD, a received optical power of -10.5 dBm is required to achieve a BER of 10^{-9} . In contrast, when the SOA is biased at 95 mA (8.1 dB gain), the same BER is obtained at a received optical power of -17.5 dBm. This corresponds to a receiver sensitivity improvement of approximately 7 dB enabled by the integrated SOA.

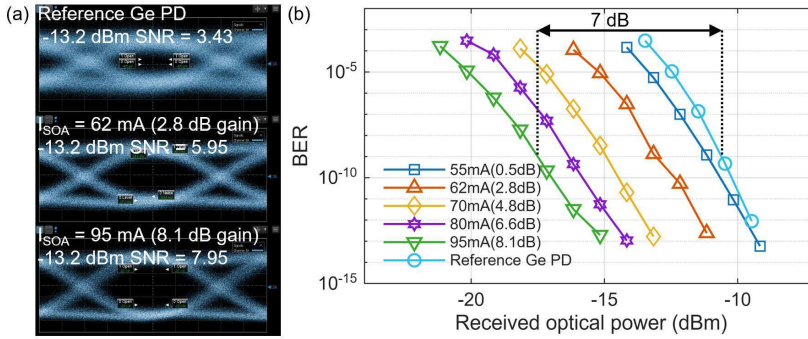


Figure 4.30: High-speed performance comparison between the pre-amplified receiver and a reference Ge PD at a PD bias voltage of -2 V. (a) Measured 30 Gbit/s NRZ eye diagrams at a received optical power of -13.2 dBm for different SOA bias currents. (b) Measured BER as a function of received optical power under different SOA bias currents.

4.7 Conclusion

We have demonstrated a C-band pre-amplified receiver on an advanced silicon photonics platform. By leveraging the μ TP technique, we integrated an InP SOA in front of a 50 GHz bandwidth Ge PD, implemented on a well-established silicon photonics platform. A dual micro-ring resonator filter, placed between the SOA and Ge PD, exhibits a 3-dB bandwidth of 1.45 nm, a low insertion loss of 0.7 dB, and an extinction ratio exceeding 25 dB, enabling effective suppression of SOA-generated ASE noise. The on-chip SOA can provide 8.1 dB optical gain at the wavelength of 1550.3 nm, which leads to a 7 dB sensitivity improvement at a BER of 10^{-9} for a 30 Gbit/s NRZ signal compared to a reference Ge PD.

5

Conclusion and outlook

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5.1 Conclusions

This thesis establishes micro-transfer printing (μ TP) as a scalable and versatile heterogeneous integration strategy for realizing high-performance optical receivers across multiple photonic platforms and wavelength ranges. By combining device engineering, photonic circuit design, and integration processing, this work demonstrates that μ TP is not only a flexible assembly technique, but a system-level enabler for advanced photonic integrated circuits.

The main contributions of this thesis are summarized as follows.

High-speed O-band photodiodes on silicon nitride

High-responsivity InGaAs/InP modified uni-traveling-carrier (MUTC) photodiodes were heterogeneously integrated onto LPCVD silicon nitride waveguides using micro-transfer printing. The demonstrated devices achieve a responsivity of 1 A/W

(corresponding to 95% quantum efficiency) at 1310 nm, a 3-dB bandwidth of 37 GHz, and error-free large-signal reception up to 40 Gbit/s (NRZ), without any form of equalization.

These results represent a high-speed photodetection solution on a silicon nitride platform, which intrinsically lacks efficient optical absorption at communication wavelengths. The analysis further shows that the device bandwidth is primarily limited by RC parasitics, rather than by the carrier transit-time of the epitaxial layer stack, providing a clear pathway toward further performance scaling through electrical optimization.

O-band multi-channel CWDM receiver

Building on the device-level demonstration, a 4×32 Gbit/s O-band CWDM receiver was realized on a silicon nitride platform. The system integrates FIR-based Mach-Zehnder lattice filters with micro-transfer-printed photodiodes, achieving multi-channel wavelength demultiplexing and parallel high-speed detection.

This work demonstrates the scalability of μ TP from single-device integration to system-level architectures. It further highlights the suitability of silicon nitride as a low-loss passive platform for wavelength-selective datacom receivers, enabling compact and energy-efficient WDM implementations.

C-band pre-amplified receiver on silicon photonics

To demonstrate platform versatility, InP-based semiconductor optical amplifier (SOA) coupons were integrated onto an advanced silicon photonics platform using μ TP. A C-band pre-amplified receiver architecture was experimentally validated, showing improved receiver sensitivity enabled by on-chip optical gain.

This result extends μ TP beyond photodetection toward the integration of active gain devices, and confirms its compatibility with foundry-based silicon photonics platforms. The demonstrated architecture provides a pathway toward compact, high-sensitivity receivers for telecom and photonic network-on-wafer systems.

Overall contribution

Collectively, this thesis demonstrates that micro-transfer printing enables a platform-agnostic and modular integration paradigm for photonic systems. In contrast to conventional bonding or monolithic approaches, μ TP decouples the fabrication of

high-performance III–V devices from passive photonic circuit processing, allowing independent optimization of each component.

This work shows that μ TP can:

- Integrate high-speed photodiodes on silicon nitride platforms,
- Enable scalable multi-channel WDM receiver architectures,
- Integrate optical gain devices on silicon photonics,
- Address both O-band datacom and C-band telecom applications.

These results establish μ TP as a key technology for future heterogeneous photonic integration, bridging the gap between material platforms and system-level functionality.

5.2 Outlook

While the results presented in this thesis demonstrate the versatility and scalability of μ TP-based integration, several important research directions remain open.

Device-level optimization

The bandwidth of the demonstrated photodiodes is currently limited by RC parasitics. Further improvements can be achieved through optimized contact engineering, reduction of pad capacitance, and improved metal routing design. In addition, tailoring the absorber thickness and mesa geometry offers opportunities to balance responsivity and speed.

For SOA-based receivers, future work should focus on gain saturation behavior, noise figure optimization, and thermal management, particularly for dense integration scenarios and high optical power operation.

Scaling to higher data rates

Future optical interconnect systems will require per-channel data rates exceeding 100 Gbit/s. Achieving this will require co-optimization of photonic devices and electronic interfaces, including impedance matching, packaging parasitics, and advanced modulation formats such as PAM4 or coherent detection.

Furthermore, increasing channel density in CWDM and DWDM systems will be essential to scale aggregate bandwidth toward terabit-per-second optical engines.

Photonics–electronics co-integration

As data rates continue to increase, the co-integration of photonics and electronics becomes a critical bottleneck. Micro-transfer printing enables deterministic placement of electronic chiplets in close proximity to photonic components, allowing very short electrical interconnections [11].

This capability opens the door to tightly integrated receiver front-ends, including multi-channel transimpedance amplifiers, modulator drivers, and digital signal processing units. Future developments may explore 2.5D and 3D integration schemes combining photonics, RF electronics, and advanced packaging technologies.

Manufacturing and reliability

For industrial adoption, challenges related to wafer-scale manufacturing and long-term reliability must be addressed. These include placement yield, alignment accuracy, thermal stability, and mechanical robustness of printed devices.

Advances in automated high-throughput μ TP processes, combined with integration into established packaging workflows, will be essential for transitioning this technology from research demonstrations to commercial photonic systems.

Final perspective

This thesis demonstrates that micro-transfer printing provides a powerful and scalable route toward heterogeneous photonic integration. By enabling deterministic integration of III–V active devices onto silicon-based platforms, μ TP supports the realization of compact, energy-efficient, and multifunctional optical receivers.

As computing and communication systems evolve toward chiplet-based and wafer-scale architectures, μ TP offers a compelling pathway to bridge photonics and electronics, enabling next-generation optical interconnects and communication infrastructures.

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