FACULTY OF ENGINEERING
AND ARCHITECTURE

# III-V on Silicon Lasers and Amplifiers Realized by Micro-Transfer Printing Integration Technology

Emadreza Soltanian

Doctoral dissertation submitted to obtain the academic degree of
Doctor of Photonics Engineering

**Supervisors**

Prof. Günther Roelkens, PhD - Jing Zhang, PhD

Department of Information Technology
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ISBN 978-94-93464-73-5
NUR 959, 965
Wettelijk depot: D/2025/10.500/133

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# Dankwoord

This thesis and all the work presented here were not possible without standing on the shoulders of many, including all the scientists and researchers who developed this field step by step, and of course all the support I received from my family, friends, teachers, and professors throughout my educational journey.

So my first expression of thankfulness goes to my supervisors, Prof. Gunther Roelkens and Dr. Jing Zhang. Gunther trusted me with this doctoral position and gave me a lot of support, space to grow, and room to learn through many rounds of trial and error. He is not only a great scientist and boss, but also a personal role model to me, showing that it is possible to excel technically while still being a kind and wonderful human being. He proved that it is possible to gather many bright and passionate scientists and support them to bloom, to extend scientific and technical boundaries, and to push the field forward.

Jing supported me step by step throughout my PhD and beyond, up to this very day. I cannot count how many times he helped me, especially during my first MPW run, when I received thousands of errors with only a few hours left to submit. And when was that? At the beginning of COVID. I also learned many practical fabrication steps from him, truly one of the best. All of this, combined with his humility, is a lesson I will carry with me. I will do my best to contribute to society and to the scientific community in the same spirit as these two amazing individuals.

I would also like to thank Prof. Bart Kuyken, who supported me for about six months as my backup supervisor, and who, together with Dr. Camiel Op de Beeck, helped significantly with the laser linewidth measurements. And a big thanks to Prof. Kasper Van Gasse for valuable insights and constructive discussions on high saturation power SOAs.

Next, I would like to thank the amazing PRG for always being a positive supporter. Of course, this positive attitude comes from Prof. Em. Roel Baets, who has integrated it into the identity of PRG. I remember one of my first presentations, when I received many technical questions, but at the end, Roel simply asked me what I thought about the field and its future. That was an eye-opening moment for me. It gave me confidence to develop my own way of thinking and to form a broader view of the field, even as a first year PhD student. After all, the PhD title essentially says that the holder is a philosopher in the field.

I could continue for days mentioning PRG stories, but I need to keep this acknowledgement short to avoid exceeding my technical thesis pages. So I briefly express my deep thankfulness to Prof. Wim Bogaerts, Prof. Dries Van Thourhout, Prof. Geert Morthier, and all other PRG professors for their scientific support and discussions. I also thank my Master supervisors, Dr. Kambiz Abedi and Dr. Kian Jafari, who prepared me well for this journey.

Every PhD and postdoc in PRG knows that behind our progress, there is a very kind and supportive team. Thank you to Ilse Van Royen, Ilse Meersman, Kristien De Meulder, Bert Coryn, and Peter Guns for administrative and logistical support. In the CR, I received tremendous help from Liesbet Van Landschoot, Muhammad Muneeb, Steven Verstuyft, Elif Ozceri Iyikanat, and Peter Geerinck.

When fabrication goes well and I get a tiny but shiny sample, I always go to the fourth floor to see if it actually shines. The champions of the Measurement Lab are always there to help, including Clemens Krickel, Hasan Salmanian, and in my first year, Jasper Jans. I also thank the MPW and IPKISS experts, Umar Khan, Ewoud Vissers, and Laurens Bogaerts. Sometimes I ask them silly questions like why my script does not run, and they immediately know that I need to run my IDE as administrator. You thought my OpenVPN was off? No, it was on.

Throughout the years, what kept us alive during the hard work was the positive atmosphere and the funny conversations in the office. Special thanks to the 150.032 group, from all the former officemates now continuing their journey elsewhere, including Alexandros Liles, Ali Raza, Meryem Benelajla, Biwei Pan, and the funniest of all, Irfan Ansari, and also former officemates on other floors like Clemens. And to the long term 150.032 members, Jing Zhang, Mattias Verstuft, and Chupao Lin. And of course to the current 150.032 members, Michele Zenari, Evangelia Delli, Tiernan McCauphery, Yu Xue, Yang Liu, Mouhamad Al Mahmoud, and Ye Chen. Thank you for all the small talks and positive energy in the office and during lunches. By the way, where is Manuel Manta Chapa?

Speaking of former PRG members, I also want to thank Javad Rahimi Vaskasi, Bahawal Haq, Camiel Op de Beeck, Mahmoud Shahin, Alejandro Diaz Tormo, Jeroen Goyvaerts, Artur Hermans, Stijn Cuyvers, Grigorij Muliuk, Hong Deng, Soren Dhoore, Gilles Feutmba, Xin Guo, Kamalpreet Kaur, Zhongtao Ouyang, Cenk Ibrahim Ozdemir, Abdul Rahim, Khannan Rajendran, Dennis Maes, Sulakshna Kumari, Anton Vaseliv, Haolan Zhao. All of you remind me that I joined PRG a long time ago and still had not defended. Time really flies.

I am truly grateful to all the current PRG members as well. I promise to only mention a few top of my head, Jasper De Witte, Yujie Guo, K. P. Nagarnajun, Ivo Tanghe, Dongbo Wang, Antonietta Parracino, Thomas Vervust, Max Kiewiet, He Li, Enes Lievens, Isaac Luntadila Lunfungula, Korneel Molkens, Stijn Poelman, Senbiao Qin, Luis Reis, Lukas Van Iseghem, Andualem Ali Yimam, and all the Toms (Vanackere, Vandekerckhove, Reep). And also IDLab friends, Nishant Singh, Joris Van Kerrebrouck, and Jakob Declercq. You can see clearly that I was not biased toward the uTP group. To add your name here, please see the pricing list at the end. Sorry, my intrusive thoughts won. Enough with the jokes.

As I mentioned earlier, Gunther and Bart gathered many bright and hardwor-

king colleagues in TRANSVERSE, and I am proud to be a member of it. Thank you to all the TRANSVERSE colleagues for the coherent efforts, including Jing Zhang, Sarah Uvin, Maximilien Billet, Laurens Bogaerts, Ali Uzun, Michele Zenari, Evangelia Delli, Elif Ozceri Iyikanat, Emiel Dieussaert, Tiernan McCauphery, Suzanne Bisschop, Philip Ekkels, Lam Tran, Margot Niels, and Ye Chen. I believe we can make an impact in the field, and we are going to.

I would also like to thank the WON team, especially Prof. Wladek Forysiak, Antonio Napoli, and Tatiana Kilina, for empowering all 14 PhD ESRs in this H2020 Marie Sklodowska Curie project. Thanks as well to Behnam Shariati, Rasoul Sadeghi Yamchi, Bruno Correia, Elliot London, Rafael Kraemer, Pratim Hazarika, Thyago Monteiro, Alex Donodin, and Gabriele Di Rosa for the great times during the WON training events.

If it was not for EU taxpayers and the brilliant minds who create and organize Horizon like and Marie Curie like programs to support scientists and develop science and technology, this thesis might have taken another decade. So thank you, even if I do not know you.

Thank you to wonderful Flanders, especially beautiful Gent, and its supportive people during difficult times, especially during COVID, who treated me, as a foreigner, as one of their own. And thank you for preserving such a fantastic city. Every time I walk from Sint Baafsplein to the Stadshal, to Klein Turkije, to Korenmarkt, and to the Graslei-Korenlei, my mind and energy get refreshed. I always feel that J. K. Rowling must have walked through here, and then everything started.

Now, to my friends who see our good and bad sides and still keep running with us through life, making its sweet and sour moments joyful. Thank you Javad Rahimi, Shahriar Nategh, Shima Arambash, Hossein SeyyedAghaei and his wonderful family, Javadoo, Pouya DeBoer, Behnam Madadnia, Arash Abyaz, Saeid Adeli, Amirreza Seraj, Pooya Poolad, Ali Hadizadeh, Saeed Misaghian, Mojtaba Abbasnejad (R.I.P.), Keyvan Keramatzadeh, Amin Samghani, Reza Jalali, Masoud Azarbeyg, Mohammad Kianfard, MohammadReza Narimani, Saber Neisi Minaei, and Mohammad Azizdoost.

If you are easy to cry, skip this part.

To my beloved family, who always supported me even during their own difficult times, even when they never had the same support they gave me. My dad, Iraj Soltanian, and my mom, Fatemeh Joulaei Jahani, from whom I learned the meaning of life. They are heroes to me, the embodiment of persistence, kindness, caring for others, and staying humble even in the toughest moments.

Thank you to my parents in law, Bakhtiar Kia and Nasrin Ahmad Khan Beigi, from whom I learned responsibility and giving others a chance for a better tomorrow.

Throughout my life I have mostly been a quiet and home staying person, but my wonderful siblings always shared their life experiences and showed me the real world through different phases. They mentored me in how to thrive and how to build positive connections with people. Thank you for taking care of me and making me a better person every day, Shafa, Captain Hossein, Mohsen, Sana, and

my siblings in law, Farzin Farshad, from whom I learned kindness and respect, Zahra, Hanna, Milad, Faeze, and Mehrdad. And thank you to the sweetest parts of life, my niblings, Matin, Yasi, and Selena. I miss you and I miss the nonsense games I created to keep your minds busy.

Finally, heartfelt thanks to my Knight, Dr. Ghazaleh Kia, my lovely wife, my best friend, and my partner in crime. I am always amazed and inspired by your hard work, persistence, your desire to make a positive impact, and your unlimited kindness that you spread to everyone. Thank you for making my life a valuable gift. I am proud of you and proud to be with you.

Thank you all for everything.

*Gent, December 2025*
*Emadreza Soltanian*

# Table of Contents

**Dankwoord** **i**

**Nederlandse samenvatting** **xxvii**

**English summary** **xxxiii**

**1 Introduction** **1-1**
1.1 Optical Fiber Network . . . . . 1-1
1.1.1 Optical Fiber Communication Links . . . . . 1-3
1.1.2 Optical Interconnects . . . . . 1-4
1.2 Integrated Photonics . . . . . 1-5
1.3 Silicon Photonics . . . . . 1-6
1.3.1 Introduction . . . . . 1-6
1.3.2 IMEC Silicon Photonics Platforms . . . . . 1-8
1.4 Integration Techniques for Silicon Photonics . . . . . 1-14
1.4.1 Hybrid Integration . . . . . 1-15
1.4.2 Heterogeneous Integration . . . . . 1-17
1.4.3 Micro-Transfer Printing Integration Method . . . . . 1-22
1.5 Thesis Outline and Attribution of Work . . . . . 1-27
1.6 Publications and Awards . . . . . 1-28
1.6.1 Publications in international peer reviewed journal papers 1-28
1.6.2 Publications in international conference proceedings . . . 1-30
1.6.3 Awards . . . . . 1-32
References . . . . . 1-33

**2 Ultra-wide Tunable Narrow-linewidth III-V on Si Laser** **2-1**
2.1 Aiming for ultra-wide tunable narrow-linewidth lasers . . . . . 2-2
2.1.1 OIF 400G-ZR Standard . . . . . 2-3
2.2 Design . . . . . 2-4
2.2.1 Building Blocks of a III-V-on-Si laser . . . . . 2-5
2.2.1.1 Si-Waveguide . . . . . 2-7
2.2.1.2 Grating Coupler . . . . . 2-8
2.2.1.3 Multi-mode-interfrometer (MMI) . . . . . 2-9
2.2.1.4 Pre-fabricated micro-transfer-printing compatible SOA . . . . . 2-11

2.2.1.5 Highly Reflective Filter . . . . . 2-18
2.2.2 Design of Tunable Narrow-Linewidth Laser . . . . . 2-20
2.2.2.1 Ring Resonator Based Filters . . . . . 2-20
2.2.2.2 Theory of Laser Linewidth . . . . . 2-23
2.2.2.3 Design of Laser's Filter and Passives . . . . . 2-27
2.2.3 Design of Ultra-Wide Tunable Narrow-Linewidth Laser . 2-29
2.3 Fabrication . . . . . 2-31
2.3.1 SOI Fabrication . . . . . 2-32
2.3.2 SOA Fabrication . . . . . 2-35
2.3.3 Integration and Post-Processing . . . . . 2-39
2.4 Characterization . . . . . 2-41
2.4.1 Laser Tunability . . . . . 2-42
2.4.2 Linewidth characterization . . . . . 2-43
2.4.2.1 Narrow-linewidth measurement methods . . . . 2-44
2.4.2.2 Linewidth measurement results of the fabricated lasers . . . . . 2-46
2.4.3 Comparison with State-of-the-Art . . . . . 2-47
2.5 Broader Application Demonstrators . . . . . 2-50
2.5.1 Biomedical Sensing Applications . . . . . 2-50
2.5.1.1 Heartbeat Monitoring . . . . . 2-50
2.5.1.2 Spectroscopy . . . . . 2-52
2.5.2 Gas Sensing . . . . . 2-52
2.5.3 Linewidth-Reduced Laser for Coherence-Critical Applications . . . . . 2-55
2.5.4 Programmable Photonics . . . . . 2-57
2.6 Conclusion . . . . . 2-59
References . . . . . 2-61

**3 Micro-Transfer Printing Compatible High Saturation Power SOA 3-1**
3.1 Aiming for $\mu$TP-compatible High Saturation Power SOA . . . . . 3-2
3.2 Design . . . . . 3-4
3.3 Fabrication . . . . . 3-8
3.3.1 SOI Fabrication . . . . . 3-9
3.3.2 SOA Fabrication . . . . . 3-10
3.3.3 Integration and Post-Processing . . . . . 3-12
3.4 Characterization . . . . . 3-15
3.5 Conclusion and Future Works . . . . . 3-18
References . . . . . 3-24

**4 Towards Wafer Scale $\mu$TP Integration 4-1**
4.1 Introduction . . . . . 4-2
4.2 Essential Tools and Processes for Wafer-Scale $\mu$TP Integration . . 4-3
4.2.1 Spray Coater – EVG®101 . . . . . 4-3
4.2.2 $\mu$TP Printer – ASMPT Amicra NANO . . . . . 4-6
4.3 Initial Demonstration of Wafer-Scale $\mu$TP . . . . . 4-7

4.3.1 BCB Spray Coating Optimization on Blank Si Wafers . . 4-9
4.3.2 Demonstration of Wafer-Scale $\mu$TP of IIIV on Si . . . . . 4-10
4.4 Conclusion and Future Work . . . . . 4-13
References . . . . . 4-15

**5 Conclusion and Outlook** **5-1**
5.1 Key Contributions . . . . . 5-2
5.2 Towards an Ecosystem for Wafer-Scale $\mu$TP Integration . . . . . 5-3

# List of Figures

1 Demonstratie van ultra-breed afstembare III-V-op-Si-lasers met smalle lijnbreedte, geïntegreerd op IMEC 400nm+ platform. (a) Schematische weergave van de laserarchitectuur met Vernier-filters gebaseerd op microringresonatoren en Sagnac-lusspiegels voor enkelmodige werking en lijnbreedtereductie. Een dubbele laserconfiguratie maakt afstemming mogelijk buiten de versterkingsbandbreedte van individuele SOA's. (b) Close-up van de transfer-geprinte SOA met finale metallisatie. (c) Gemeten afstembereik van meer dan 110 nm over het gecombineerde laserspectrum. (d) Lijnbreedtemetingen met de OEwaves OE4000 bevestigen Lorentz-profielen ruim onder de 400G-ZR-drempel van 500 kHz. . . . . xxviii

2 Demonstratie van een nieuw hybride III-V-op-Si tapervormig ontwerp voor SOA's met hoge verzadigingsvermogens. (a) Schematische weergave van de getaperde SOA-structuur met een geleidelijk verbredende actieve regio en siliciumgolfgeleider om de optische opstelling te optimaliseren en het verzadigingsvermogen te verhogen. (b) Microscopisch beeld van de transfer-geprinte SOA op een E-beam rapid prototyping siliciumstaal. (c) SEM-dwarsdoorsnede van de taperpunt en $\mu$TP-uitlijningsmarkeringen. (d) Gemeten on-chip versterking van 8,36 dB en uitgangsvermogen versus toenemend ingangssignaal, waaruit een verzadigingsvermogen van 18,4 dBm wordt afgeleid, wat de effectiviteit van de getaperde SOA als booster-versterker bevestigt. . . . . xxix

3 Demonstratoren die de veelzijdigheid van het III-V-op-Si laserplatform buiten telecomtoepassingen aantonen. (a) µLens-gemonteerde laser-PIC gebruikt voor biomedische sensing via hartslagmonitoring door transmissie via de oorlel. (b) Hybride III-V-op-SiN laser met lijnbreedtes onder de 25 kHz voor toepassingen waarbij coherentie cruciaal is, zoals LiDAR. (c) Verpakte SiPh-laser met geïntegreerde golflengtemonitoring en vergrendeling voor gassensing. (d) Programmeerbare fotonische chip met dynamische herconfigureerbaarheid, die de brede inzethbaarheid van het geïntegreerde laser- en versterkerplatform illustreert. . . . . xxx

4 Overgang van chipniveau naar waferniveau $\mu$TP-integratie binnen de Transverse pilotlijn. (a) Overzicht van $\mu$TP-integratie op wafer-schaal. (b) Demonstratie van $\mu$TP-integratie op wafer-schaal van III-V-coupons op een 200 mm SiPh-wafer, met submicron uitlijningsprecisie en een printopbrengst van 100%. . . . . xxxi

5 Demonstration of ultra-wide tunable narrow-linewidth III-V-on-Si lasers integrated on IMEC 400nm+ platform. (a) Schematic of the laser architecture featuring Vernier filters based on microring resonators and Sagnac loop mirrors for single-mode operation and linewidth reduction. A dual-laser configuration enables tuning beyond the gain bandwidth of individual SOAs. (b) Close-up of transfer-printed SOA with final metallization. (c) Measured tuning range exceeding 110 nm across the combined laser spectrum. (d) Linewidth characterization using OEwaves OE4000 confirms Lorentzian linewidths well below the 400G-ZR threshold of 500 kHz. . . . . xxxiv

6 Demonstration of a novel hybrid III-V-on-Si tapered design for high saturation power SOAs. (a) Schematic of the tapered SOA structure with a gradually widening active region and silicon waveguide to optimize optical confinement and increase saturation power. (b) Microscope image of the transfer-printed SOA on an E-beam rapid prototyping silicon sample. (c) SEM cross-sectional view of the taper tip and $\mu$TP alignment markers. (d) Measured on-chip gain of 8.36 dB and output power versus increasing input power, leading to extraction of a saturation output power of 18.4 dBm, validating the tapered SOA as an effective booster amplifier. xxxv

7 Demonstrators showcasing the versatility of the III-V-on-Si laser platform beyond telecom applications. (a) µLens-mounted laser PIC used for biomedical sensing via heartbeat monitoring through earlobe transmission. (b) Hybrid III-V-on-SiN laser achieving linewidths below 25 kHz for coherence-critical applications such as LiDAR. (c) Packaged SiPh laser with integrated wavelength monitoring and locking for gas sensing. (d) Programmable photonic chip with dynamic reconfiguration capabilities, illustrating the adaptability of the integrated laser and amplifier platform. . . . . xxxvi

8 Overgang van chipniveau naar waferniveau $\mu$TP-integratie binnen de Transverse pilotlijn. (a) Overzicht van $\mu$TP-integratie op wafer-schaal. (b) Demonstratie van $\mu$TP-integratie op wafer-schaal van III-V-coupons op een 200 mm SiPh-wafer, met submicron uitlijningsprecisie en een printopbrengst van 100%. . . . . xxxvii

1.1 Global Internet user growth (Cisco) [5]. . . . . 1-2
1.2 Global device and connection growth (Cisco) [5]. . . . . 1-2
1.3 Submarine optical fiber connections. Reproduced from [8]. . . . . 1-3

1.4 Schematics of an optical communication link [12]. . . . . 1-4
1.5 Three levels of optical networks with different reach of the fibre-optic link. Reproduced from [13]. . . . . 1-4
1.6 Attenuation spectrum of optical fiber. Reproduced from [26]. . . . 1-5
1.7 Silicon photonic die forecast by application (Yole Group) [65]. . . 1-8
1.8 Si Photonics-based transceiver forecast 2018-2024 (Yole Group) [68]. . . . . 1-9
1.9 Silicon photonics value chain for optical communication (Yole Group) [69]. . . . . 1-9
1.10 Energy band diagrams and major carrier transition processes in InP (direct bandgap) and silicon crystals (indirect bandgap) [70]. . 1-10
1.11 Multi-project-wafer concept [71]. . . . . 1-10
1.12 Process Design Kit concept, imec iSiPP toolbox [72]. . . . . 1-11
1.13 IMEC Si-400 nm Platform (Size proportions are not preserved for illustrative clarity). . . . . 1-12
1.14 IMEC Passives+ platform (Size proportions are not preserved for illustrative clarity). . . . . 1-12
1.15 IMEC 400nm+ Platform (Size proportions are not preserved for illustrative clarity). . . . . 1-13
1.16 IMEC iSiPP50G Platform [74]. . . . . 1-14
1.17 A simple schematic of the hybrid integration technique. A gain chip is placed next to a Si PIC where both chips are mounted on a separate common substrate [19]. . . . . 1-15
1.18 A side-view SEM image of PWB, connecting an InP DFB laser chip to a waveguide on a SiP chip [84]. . . . . 1-16
1.19 Schematic view of a butt-coupled III-V chip to a SiN extended cavity [87]. . . . . 1-16
1.20 Schematic view of flip-chip of a single device onto a SiPh wafer. Prior to the integration process, the devices are diced on the native substrate [97]. . . . . 1-17
1.21 Schematics of wafer bonding technology [12]. . . . . 1-18
1.22 Schematic process flow for multiple-die-to-wafer bonding. Reproduced from [16, 106]. . . . . 1-19
1.23 Schematic of Hetero-Epitaxial growth, where III-V materials such as GaAs are grown as nanoridges on a silicon target wafer [97]. . . 1-20
1.24 Process flow schematic of regrowth on a bonding template III-V-on-Si integration [119]. . . . . 1-20
1.25 Schematic of $\mu$TP-based integration in a parallel manner on 200 mm or 300 mm Si photonic wafers [16]. . . . . 1-22
1.26 Schematics of the separation energy dependencies on the peeling speed. When the peeling speed is lower than the critical speed printing will occur. When it is higher, pick-up will occur. Typically, for inorganic semiconductor devices, the device-substrate separation energies are a lot higher (blue dashed-line) [12, 97, 129]. 1-23
1.27 The main concept of the transfer printing process [12, 124]. . . . . 1-24

1.28 Release process schematic [12, 131]. . . . . 1-25
1.29 The $\mu$TP-100 system [132]. . . . . 1-26
1.30 Schematics of the lab-scale transfer printing machine [132]. . . . . 1-26

2.1 Basic Schematic of a Laser. . . . . 2-6
2.2 Basic Schematic of a hybrid laser. . . . . 2-6
2.3 Basic Schematic of a heterogeneous laser. . . . . 2-6
2.4 Schematic cross-section of IMEC 400nm+ pltaform's WWG (left) and RWG (right). The scale is not kept for a better representation. 2-7
2.5 Effective Index vs. the Core width of WWG at 1550 nm. . . . . 2-8
2.6 Effective Index vs. the Core width of RWG at 1550 nm. . . . . 2-8
2.7 Fundamental mode profile at 1550 nm with WWG width of 350 nm (left), and 450 nm (right) to maximize the confinement in the Si core or minimizing the sidewall loss. . . . . 2-8
2.8 (a): Measured transmission spectra for a set of waveguides with different length, (b): Calculated propagation loss of the fundamental TE mode in 650 nm wide rib waveguide [15]. . . . . 2-9
2.9 The screenshot of the GDS layout of the IMEC 400nm+ PDK grating coupler (left), and it's insertion loss spectrum (right). . . . . 2-10
2.10 The schematic layout design of the 50/50 1x2 MMI based on IMEC 400nm+ RWG, The mode profile, transmission spectrum, and coupling percentage vs. the core length of the MMI. . . . . 2-10
2.11 The schematic layout design of the 50/50 2x2 MMI based on IMEC 400nm+ RWG, transmission spectrum and coupling percentage vs. the core length of the MMI. . . . . 2-11
2.12 Schematic layout of a tunable Sagnac loop mirror formed by connecting two 50/50 MMIs. In the default state (no phase shift), the structure reflects all input light back to the input waveguide due to destructive interference at the output. By applying a phase shift via a heater on one of the MZI arms, the reflection/out-coupling ratio can be tuned. The tuning range spans from 0% to 100% out-coupling. . . . . 2-11
2.13 Schematic layout of a cross-section of the III-V-on-Si laser (left), and the intensity profile of the fundamental optical mode in the hybrid III-V/Si waveguide (right) [15]. . . . . 2-13
2.14 Simulated optical mode conversion over the adiabatic taper structure [15]. . . . . 2-13
2.15 Schematics and FIB cross-sections illustrating the design of the full-coupling and partial-coupling III-V-on-Si SOAs [23]. . . . . 2-14
2.16 The simulated coupling efficiency of the adiabatic taper structures for the partial and full-coupling designs versus the lateral misalignment: Si-400 nm (left), iSiPP50G (right) [23]. . . . . 2-14
2.17 Schematic illustration and simulated mode profile of the ISIPP50G waveguide cross-section with integrated SOA [23]. . . . . 2-15

2.18 Schematic illustrating the design of the DFB laser, the cross-section view of the adiabatic taper and the side view of the DFB grating [23].2-15
2.19 Design schematic of full-coupling and partial-coupling DBR lasers. The cross-section in the gain section is also illustrated [23]. . . . . 2-15
2.20 (left) Calculated power coupling between full-coupling III-V adiabatic taper design and Si waveguide of width 3.0 $\mu$m, 2.0 $\mu$m and 1.5 $\mu$m, (right) Calculated coupling efficiency against the rotational misalignment between III-V adiabatic taper and Si waveguide [23]. . . . . 2-16
2.21 The change in confinement factor in QWs with the misalignment variation for 3.0 $\mu$m and 5.0 $\mu$m Si waveguide width, insets illustrate the mode profile at zero and 2.0 $\mu$m misalignment [23]. . . . 2-16
2.22 (a) Calculated coupling efficiency for variation in a) adiabatic III-V taper width, (b) n-InP thickness, (c) QW width and (d) BCB thickness [23]. . . . . 2-17
2.23 Schematic (Top) and layout design (Bottom) of this work's SOA. . 2-17
2.24 Simulated optical coupling from the III–V to silicon. (a) Optical intensity distribution showing mode coupling between the silicon waveguide and III–V layers. (b) Impact of $\mu$TP misalignment on mode confinement and transmission efficiency [27]. . . . . 2-18
2.25 Schematic (Top) and layout design (Bottom) of this work's SOA. . 2-19
2.26 Schematic of an add-drop ring resonator with two bus waveguides and a ring waveguide. . . . . 2-21
2.27 Transmission to the through port and drop port of an add-drop ring resonator, as a function of wavelength. . . . . 2-22
2.28 Vernier filter schematic (left), Transmission to the drop port of the vernier filter, as a function of wavelength. . . . . 2-23
2.29 The spectral line shape of the laser optical field exhibits a Gaussian-like profile near the peak and transitions to a Lorentzian-like profile at the tails. Axes are presented in logarithmic scale. Representation from [38]. . . . . 2-24
2.30 A schematic illustration of the power spectral density (PSD) of frequency noise as a function of Fourier frequency, highlighting the various noise contributions typically present in hybrid-integrated diode lasers, each indicated with different colors [28, 38]. . . . . 2-26
2.31 A schematic layout of the external cavity design of the widely tunable narrow-linewidth III-V-on-Si laser. . . . . 2-27
2.32 An MZI added in series to a Vernier filter to double the total FSR. In this configuration, the arm's length difference of MZI needs to be chosen so the MZI's FSR be twice the Vernier's FSR. . . . . 2-30
2.33 3D schematic layout of the dual-laser configuration. For simplicity, just one pair of electrical connections to a heater is shown. . . 2-31
2.34 Dual-Laser GDS Mask. . . . . 2-32
2.35 Schematics of the IMEC 400nm+ SOI cross-section with the integrated metal layers and back-end stack. . . . . 2-33

2.36 Fabricated design on a 200 mm SiPh wafer based on the IMEC 400nm+ platform through an internal MPW run. . . . . 2-33
2.37 Opening recess patterning by photolithography using Ti35E photoresist. . . . . 2-34
2.38 Cross-sectional SEM image of the waveguide inside a recess after back-end etch-back by RIE. . . . . 2-34
2.39 Microscope image of the over-etched Si-waveguide inside a recess after back-end etch-back by RIE. . . . . 2-34
2.40 Schematic cross-section overview after completion of back-end recess opening by BHF etching (top). Microscope image of the processed sample and its scanned profile (bottom), showing the Si-waveguide is exposed after BHF etching. . . . . 2-35
2.41 Schematic cross-section overview after BCB spray-coating over the recess. . . . . 2-35
2.42 Photoluminescence spectra and wafer map of the III-V SOA epitaxial layer stacks with MQW variants, achieving photoluminescence peaks at 1500 nm and 1550 nm, reported by III-V Lab. . . . 2-37
2.43 Process flow of SOA device fabrication on the source InP substrate. 2-38
2.44 A fabricated InP coupon source: a) Side-view SEM image, b) Top-view microscope image. . . . . 2-39
2.45 Schematic presentation of the photomask used for patterning the release layer and encapsulating the device, along with a close-up view of the tether design [23]. . . . . 2-39
2.46 Process flow of PIC preparation for $\mu$TP, micro-transfer printing and post processing. . . . . 2-40
2.47 (a) Stitched microscope image of the combined widely tunable lasers. (b) Micro-transfer-printed III-V amplifier in the recess (after final metallization). . . . . 2-41
2.48 Schematic layout of the laser characterization setup. . . . . 2-42
2.49 Tuning spectrum of Dual-Laser A (300 nm ring gap). Fine tuning in steps of 100 pm was performed over a 4 nm range, equivalent to the FSR of one ring. . . . . 2-43
2.50 Tuning spectrum of Dual-Laser B (200 nm ring gap). Fine tuning was done in 10 steps over a 4 nm range, matching the ring FSR. . 2-43
2.51 Principle of optical beat notes [49]. . . . . 2-45
2.52 Beat note with a reference laser [49]. . . . . 2-45
2.53 Delayed self-homodyne detection [49]. . . . . 2-46
2.54 Delayed self-heterodyne detection [49]. . . . . 2-46
2.55 OEwaves HI-Q® LASER LINEWIDTH/PHASE NOISE ANALYZER [57, 59]. . . . . 2-47

2.56 Measured Lorentzian linewidth of the Dual-Laser A (ring gap = 300 nm) across its tuning range, obtained using the OEwaves OE4000 Optical Phase Noise Test System. All measured linewidths remain well below the 400G-ZR standard linewidth threshold mask (500 kHz), demonstrating the laser's suitability for advanced coherent applications. . . . . 2-48

2.57 Frequency noise power spectral density of Laser 1 (ring gap = 300 nm), measured using the OEwaves OE4000 Optical Phase Noise Test System. The laser was biased at 120 mA and operated at a wavelength of 1530 nm. The measured noise remains well below the 400G-ZR linewidth threshold mask, indicating suitability for coherent optical communication standards. . . . . 2-48

2.58 $\mu$Lens mounting process flow by CSEM (Top Left) [67], along with the schematic cross-section view of the PIC with a micro-transfer-printed laser and a $\mu$Lens (Top Right). Microscope top view image of the mounted $\mu$Lens on a PIC (Bottom Right), with a side view SEM image (Bottom Left). . . . . 2-51

2.59 PCB layout by VTT (Top Left). Two Laser dies mounted and wire-bonded to the PCB (Top Right). Two prototype configurations as fiber-based and wireless wearable Hyperspectral sensors with the time-resolved measurements of heartbeat through the earlobe. . . 2-51

2.60 (a) Microscope image of the PIC with three $\mu$TP lasers. (b) Absorption peak of biological substances [71]. (c) Previously demonstrated tuning spectrum within the range of 1500-1600 nm [72]. (d) Extended tunability range of more than 60 nm within the range of 1640-1710 nm [27]. . . . . 2-53

2.61 Schematic layout of a SiPh PIC integrating two $\mu$TP-based lasers, a tunable optical switch (combiner), and a wavelength monitoring and locking system composed of a micro-ring resonator (MRR) and a photodiode (PD). . . . . 2-54

2.62 Block diagram illustrating the concept of the on-chip wavelength monitoring and locking system. A portion of the laser output is coupled to an MRR whose resonance is swept via a heater. When the MRR's resonance matches the laser wavelength, the signal is dropped to the PD and converted into an electrical signal for feedback control. . . . . 2-54

2.63 Packaged SiPh laser PIC using PHIX assembly technology. The 3D schematic illustrates the alignment of the fiber array (FA) to the PIC while the chip is wirebonded to the PCB. The microscope image shows the PIC surface, including gold metallization atop the SOA regions to redistribute electrical connections to the bond pads. 2-55

2.64 Narrow-Linewidth III–V/SiN laser [81]. (a) Taper design with simulated mode evolution from SiN to InP. (b) Photonic circuit with $\mu$TP-integrated gain, tunable Sagnac loop mirror, MRRs, and phase control. (c) Output spectrum showing 54 nm tuning range. (d) Linewidths $<$25 kHz across the wavelength tuning range, suitable for coherence-critical applications. . . . . 2-56
2.65 (a) Conceptual schematic of the fully integrated programmable photonic engine, highlighting its modular building blocks: $\mu$TP-integrated lasers and SOAs, high-speed modulators, optical switches, tunable couplers, phase shifters, and tap monitors, all interfaced via a fiber array unit. (b) Packaged photonic engine mounted on a PCB with integrated DC, RF, and thermal control interfaces. The SiPh chip, containing all active and passive components, is wire-bonded for external interfacing and control [82]. . . . . 2-58
2.66 (a) Microscope image of the fabricated iSiPP50G photonic engine chip with labeled components: $\mu$TP-integrated tunable lasers, SOAs, high-speed modulators, programmable filter, detectors, and grating couplers. (b–c) Optical spectra demonstrating wide tunability of the on-chip lasers across 1507–1598 nm. (d) Phase noise comparison between the $\mu$TP laser and a commercial Syntune laser, showing competitive noise performance. (e) Time-domain power stability trace of the $\mu$TP-integrated laser output, confirming suitability for coherent signal processing applications [82]. . . . . 2-59

3.1 A comparison of optical mode profile confinement in the QWs of SOAs based on III-V and hybrid III-V-on-Si structures. By incorporating the underlying Si waveguide and making it wider, the confinement in the QWs reduces as the mode gets pushed down into the Si waveguide. . . . . 3-5
3.2 The proposed tapering scheme for the III-V-on-Si integrated SOA to increase the optical saturation power level, while maintaining enough optical gain. . . . . 3-6
3.3 The modified tapering scheme for the III-V-on-Si integrated SOA to increase the optical saturation power level, while maintaining sufficient optical gain, reducing side wall interactions, and enhancing the tolerance to lateral misalignment. . . . . 3-7
3.4 Simulation of the hybrid optical modes in the proposed amplifier using Ansys Lumerical MODE. (a) Perspective of the simulated tapered hybrid SOA. Top-view and side-view of the propagation over the SOA are shown in (b) and (c), respectively. Optical mode profiles from the narrowest to the widest part of the tapered SOA waveguide is shown in (e)-(i), excluding the coupling tapers to the single-mode Si waveguides. . . . . 3-8
3.5 The GDS mask prepared for the fabrication of the proposed InP-based SOA coupons. . . . . 3-9

3.6 The GDS mask prepared for patterning the Si waveguide circuits by e-beam lithography. . . . . 3-9
3.7 The GDS mask showing the InP based SOA coupon on top of the Si waveguide with the final metal on top. . . . . 3-10
3.8 Waveguide circuit fabrication steps. . . . . 3-11
3.9 The microscope image of the fabricated waveguide circuit. . . . . 3-11
3.10 InP-based SOA coupon fabrication steps. . . . . 3-12
3.11 FIB cross-section images of the fabricated InP SOA coupons. Places where the FIB images were taken are marked on the top left microscope image which shows a top-view of the SOA coupons. . . 3-12
3.12 Side view SEM images of the taper and the electrical isolation island of the SOA coupons. . . . . 3-13
3.13 Side view SEM images of the encapsulated SOA coupons after release, showing the suspended coupons on their tethers as well as the breakage point of the remaining tethers after pickup. . . . . 3-13
3.14 Process flow of micro-transfer printing and post processing. . . . . 3-14
3.15 Microscope image of a printed SOA coupon on the Si waveguide. 3-14
3.16 Microscope image of a printed array of SOA coupons on the SiPh chip with the final metallization on top to complete the circuit. . . 3-14
3.17 Measurement setup of the integrated high saturation power SOA. . 3-15
3.18 On-chip gain as a function of wavelength, while the waveguide-coupled input power is 2.0 dBm and the pump currents of the left and right sides are 114/130 mA and 140 mA, respectively. . . . . 3-16
3.19 The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves. The pump currents of the left and right sides are 114 mA and 140 mA, respectively. . . . . 3-17
3.20 The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves. The pump currents of the left and right sides are 130 mA and 140 mA, respectively. . . . . 3-17
3.21 The measured wall-plug efficiency of the SOAs as a function of the on-chip optical input power. . . . . 3-18
3.22 Comparison of this work against state of the art references [17, 23]. The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves. . 3-19
3.23 Schematic illustration of an alternative SOA design utilizing a tapered silicon waveguide. Transitions between the silicon and hybrid waveguides, which are not shown here, are designed to be adiabatic. At the output, the wider silicon waveguide is gradually tapered back to a single-mode waveguide [14]. . . . . 3-20

3.24 Schematic illustration of the coherent beam combining SOA configuration (top). Screenshot of the GDS layout of the proposed III-V-on-Si integrated circuit (bottom). . . . . 3-21
3.25 Microscope image of the wire-bonded sample of coherent beam combining SOA configuration to PCB. . . . . 3-22
3.26 Wire-bonded sample of coherent beam combining SOA configuration to PCB on a measurement setup. . . . . 3-22
3.27 Double-Ridge SOA configuration, providing the laser's gain and booster SOAs into a single encapsulated coupon [31]. . . . . 3-23

4.1 Wafer-scale $\mu$TP integration schematic. . . . . 4-2
4.2 PhotonixFAB value chain, to establish a European photonics device value chain and initial industrial manufacturing capabilities, providing a path to scalable high-volume manufacturing for innovative product developers [4]. . . . . 4-4
4.3 EVG®101 spray coater installed at Ghent University cleanroom for wafer-scale thin-film BCB deposition. . . . . 4-5
4.4 Spray coating scheme, mentioning the important controllable parameters of EVG101. . . . . 4-6
4.5 ASMPT Amicra Nano printer installed at Ghent University Cleanroom for wafer-scale $\mu$TP. . . . . 4-7
4.6 ASMPT Amicra Nano printer with opened door showing source chuck, target chuck, and the transfer head . . . . . 4-8
4.7 (Left) 1st layer of 100 nm BCB spray coated on a blank Si wafer, (Middle) 2nd layer of 100 nm BCB spray coated on the same wafer to reach 200 nm of BCB in total. (Right) One time of spray coating less diluted BCB on a blank Si wafer to reach 200 nm of thickness. 4-10
4.8 Full layout of the 200 mm SiPh wafer, highlighting a zoomed-in view of a representative reticle used for $\mu$TP integration. Each block within the reticle consists of standardized SOA/FP laser building blocks from the $\mu$TP-PDK, featuring tunable design parameters such as cavity and coupon lengths, waveguide bend radius, and directional coupler splitting ratio, configurable for both C-band and O-band operation. . . . . 4-11
4.9 Printed coupons on the SOA (left) and FP laser (right) blocks using wafer-scale printer. . . . . 4-11
4.10 The 3D optical microscope reconstruction of an InP SOA coupon printed on a Si waveguide using a wafer-scale printer, showing the sub-micron alignment precision. . . . . 4-12
4.11 Implementation of metallized donut-shape $\mu$TP alignment markers on the coupons to ensure high alignment precision. A zoomed-in view, illustrating the way of lateral misalignment measurement. . . 4-13

# List of Tables


1.1 Various waveguide platforms, advantages and disadvantages. . . . 1-7

2.1 Integrated laser's requirements extracted from the optical specifications of a 400G-ZR transmitter [6]. . . . . 2-4
2.2 IMEC 400nm+ RWG specifications extracted from the simulations and measurements. . . . . 2-9
2.3 C-band microring resonator parameters. . . . . 2-28
2.4 L-band microring resonator parameters. . . . . 2-28
2.5 Relationship between the gap of the constituent rings and the estimated Vernier Q-factor and Vernier Linewidth Reduction Factor (LRF) for C-band and L-band. . . . . 2-29
2.6 III-V SOA epitaxial layer stacks, with MQW variants achieving photoluminescence peaks at 1500 nm and 1550 nm. . . . . 2-36
2.7 Comparison of key performance metrics for widely tunable narrow-linewidth integrated lasers. . . . . 2-49

3.1 Comparison of Hybrid III-V-on-Si SOAs . . . . . 3-19

# List of Acronyms

## A

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| AWG | Arrayed Waveguide Grating |

## B

| | |
|---|---|
| BER | Bit Error Rate |

## C

| | |
|---|---|
| C-Band | Conventional Band (1530–1565 nm) |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| CW | Continuous Wave |

## D

| | |
|---|---|
| DBR | Distributed Bragg Reflector |
| DFB | Distributed Feedback |
| DSP | Digital Signal Processing |
| DUT | Device Under Test |

## E

| | |
|---|---|
| EDA | Electronic Design Automation |

| | |
|---|---|
| EDFA | Erbium-Doped Fiber Amplifier |
| EPFL | École Polytechnique Fédérale de Lausanne |
| EPI | Epitaxial Layer |

## F

| | |
|---|---|
| FBG | Fiber Bragg Grating |
| FP | Fabry–Pérot |
| FMCW | Frequency-Modulated Continuous-Wave |
| FSR | Free Spectral Range |
| FWHM | Full Width at Half Maximum |

## G

| | |
|---|---|
| GC | Grating Coupler |
| GBW | Gain Bandwidth |

## I

| | |
|---|---|
| III–V | Compound semiconductors from group III and V |
| IL | Insertion Loss |
| IMEC | Interuniversity Microelectronics Centre |
| InP | Indium Phosphide |

## L

| | |
|---|---|
| LASER | Light Amplification by Stimulated Emission of Radiation |
| LiDAR | Light Detection and Ranging |
| L-Band | Long Band (1565–1625 nm) |

## M

| | |
|---|---|
| MFD | Mode Field Diameter |

| | |
|---|---|
| MIR | Mid-Infrared |
| MRR | Microring Resonator |
| $\mu$TP | Micro-Transfer Printing |
| MZI | Mach–Zehnder Interferometer |

## N

| | |
|---|---|
| n-InP | n-doped Indium Phosphide |
| NRZ | Non-Return-to-Zero |

## O

| | |
|---|---|
| OE | Optoelectronic |
| OFDR | Optical Frequency-Domain Reflectometry |
| OIF | Optical Internetworking Forum |
| OSA | Optical Spectrum Analyzer |

## P

| | |
|---|---|
| PD | Photodiode |
| PDK | Process Design Kit |
| PIC | Photonic Integrated Circuit |
| p-InP | p-doped Indium Phosphide |
| PL | Photoluminescence |
| PLL | Phase Locked Loop |
| PSD | Power Spectral Density |

## Q

| | |
|---|---|
| Q-factor | Quality Factor |
| QW | Quantum Well |

## R

| | |
|---|---|
| R&D | Research and Development |
| RF | Radio Frequency |
| RIN | Relative Intensity Noise |

## S

| | |
|---|---|
| Si | Silicon |
| SiN | Silicon Nitride |
| SiPh | Silicon Photonics |
| SMSR | Side Mode Suppression Ratio |
| SMF | Single Mode Fiber |
| SOA | Semiconductor Optical Amplifier |
| ST | Schawlow–Townes |
| SNR | Signal to Noise Ratio |

## T

| | |
|---|---|
| TEC | Thermoelectric Cooler |
| TL | Tunable Laser |
| TO | Thermo-Optic |
| TRL | Technology Readiness Level |

## U

| | |
|---|---|
| UGent | Ghent University |

## V

| | |
|---|---|
| VCSEL | Vertical-Cavity Surface-Emitting Laser |

## W

| | |
|---|---|
| WDM | Wavelength-Division Multiplexing |

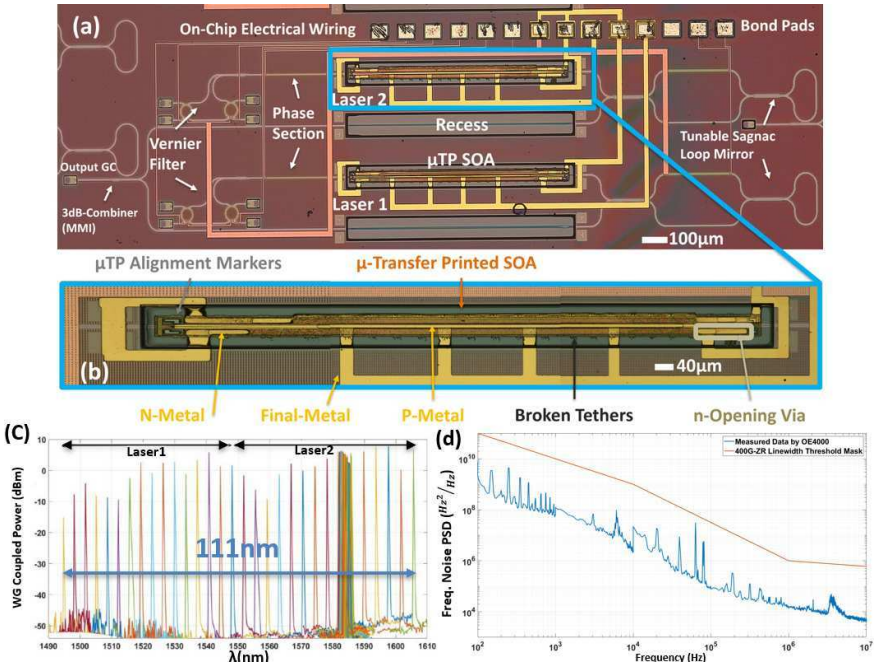
# Nederlandse samenvatting –Summary in Dutch–

Dit proefschrift presenteert een diepgaand onderzoek naar de ontwikkeling van III-V-op-silicium lasers met smalle lijnbreedte en brede afstembaarheid, evenals halfgeleider optische versterkers (SOA's) met hoge verzadigingsvermogen, gerealiseerd via micro-transferdruk ($\mu$TP) integratietechnologie. Het werk speelt in op de groeiende vraag naar schaalbare, hoogpresterende fotonische geïntegreerde schakelingen (PICs) door gebruik te maken van de veelzijdigheid en precisie van $\mu$TP om III-V versterkingsmaterialen op siliciumfotonica (SiPh) platformen te integreren. Het bouwt voort op een sterke basis van eerder onderzoek binnen de Photonics Research Group (PRG), waarbij bestaande concepten en architecturen worden uitgebreid tot oplossingen die breed inzetbaar zijn voor verschillende toepassingen en platformen. Het proefschrift begint met het schetsen van de evolutie van optische communicatienetwerken, waarbij de verschuiving van koperverbindingen naar breedbandige, verliesarme optische vezelsystemen wordt benadrukt. Door de exponentiële groei van dataverkeer, aangedreven door cloud computing, videostreaming en AI-workloads, is de behoefte aan compacte, energie-efficiënte en snelle fotonische oplossingen steeds urgenter geworden. Siliciumfotonica, compatibel met CMOS-productieprocessen, biedt een veelbelovend platform voor schaalbare integratie, maar mist intrinsieke lichtbronnen vanwege de indirecte bandstructuur van silicium.

Om deze beperking te overwinnen, onderzoekt het proefschrift verschillende integratietechnieken voor het introduceren van III-V materialen op SiPh platformen, waaronder hybride, heterogene en micro-transferdruk methoden. Van deze technieken blijkt $\mu$TP bijzonder krachtig te zijn, doordat het selectieve en schaalbare integratie van vooraf gefabriceerde III-V componenten op silicium mogelijk maakt met submicron-nauwkeurigheid. Het $\mu$TP-proces wordt gedetailleerd beschreven, inclusief de principes van kinetisch geschakelde adhesie, het losmaken van componenten door het breken van de verankering, en het gebruik van PDMS-stempels voor overdracht.

De kernbijdrage van dit proefschrift is het ontwerp en de demonstratie van III-V-op-Si lasers met een ultra-brede afstembaarheid en smalle lijnbreedte. Deze lasers zijn geïntegreerd op IMEC 400nm+ platform via $\mu$TP van vooraf gefabriceerde SOA's, gebaseerd op eerder werk van de PRG en met een laserarchitectuur die bewust is ontworpen om compatibel en eenvoudig aanpasbaar te zijn voor diverse toepassingen en platformen. De laserarchitectuur omvat Vernier-gefilterde

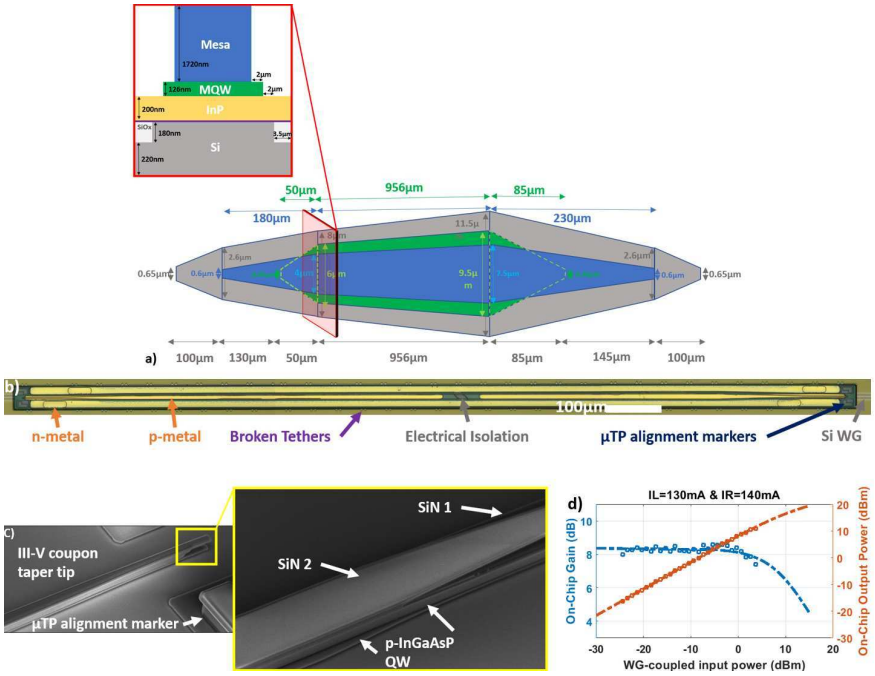
micro-ring resonatoren en Sagnac-loop spiegels om enkelmodige werking en lijnbreedtereductie te realiseren. Een dubbele laserconfiguratie wordt geïntroduceerd om het afstembereik uit te breiden voorbij de versterkingsbandbreedte van individuele SOA's, wat resulteert in een gecombineerd afstembereik van meer dan 110 nm. Lijnbreedtemetingen met de OEwaves OE4000 bevestigen Lorentz-profielen ruim onder de 400G-ZR standaarddrempel van 500 kHz, met waarden tussen 13 en 170 kHz over het volledige afstembereik.




*Figuur 1: Demonstratie van ultra-breed afstembare III-V-op-Si-lasers met smalle lijnbreedte, geïntegreerd op IMEC 400nm+ platform. (a) Schematische weergave van de laserarchitectuur met Vernier-filters gebaseerd op microringresonatoren en Sagnac-lusspiegels voor enkelmodige werking en lijnbreedtereductie. Een dubbele laserconfiguratie maakt afstemming mogelijk buiten de versterkingsbandbreedte van individuele SOA's. (b) Close-up van de transfer-geprinte SOA met finale metallisatie. (c) Gemeten afstembereik van meer dan 110 nm over het gecombineerde laserspectrum. (d) Lijnbreedtemetingen met de OEwaves OE4000 bevestigen Lorentz-profielen ruim onder de 400G-ZR-drempel van 500 kHz.*

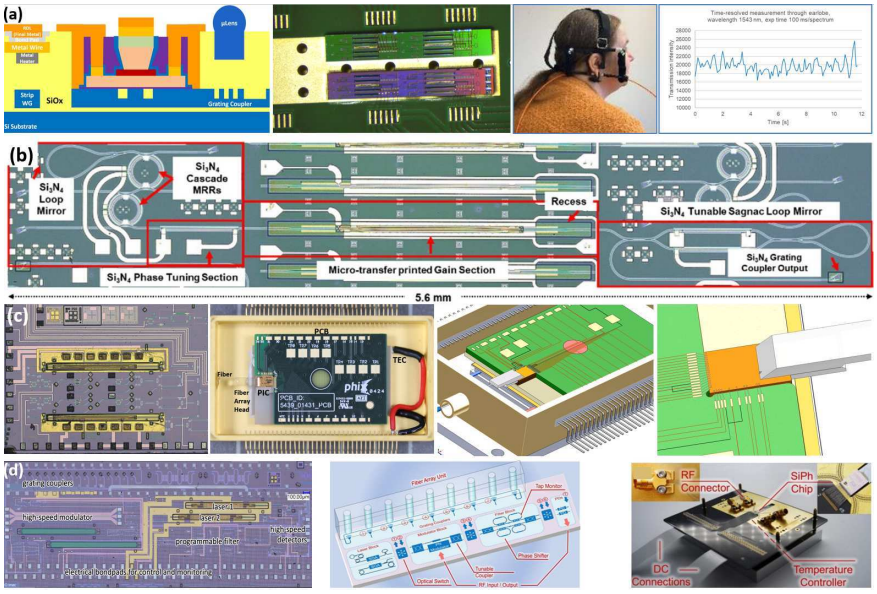
Om het uitgangsvermogen van de laser verder te verhogen, wordt een nieuw taps toelopend SOA-ontwerp voorgesteld en gerealiseerd. Deze hybride III-V-op-Si versterker heeft een geleidelijk verbredende actieve regio en siliciumgolfgeleider, waardoor de confinementfactor en doorsnede worden geoptimaliseerd om het verzadigingsvermogen te verhogen terwijl de versterking behouden blijft. Analyse van de experimentele resultaten berekent een uitgangsverzadigingsvermogen van

18,4 dBm en een wall-plug efficiëntie van 3,5%, wat de effectiviteit van het taps toelopende SOA-ontwerp als versterker bevestigt.




*Figuur 2: Demonstratie van een nieuw hybride III-V-op-Si tapervormig ontwerp voor SOA's met hoge verzadigingsvermogens. (a) Schematische weergave van de getaperde SOA-structuur met een geleidelijk verbredende actieve regio en siliciumgolfgeleider om de optische opstelling te optimaliseren en het verzadigingsvermogen te verhogen. (b) Microscopisch beeld van de transfer-geprinte SOA op een E-beam rapid prototyping siliciumstaal. (c) SEM-dwarsdoorsnede van de taperpunt en µTP-uitlijningsmarkeringen. (d) Gemeten on-chip versterking van 8,36 dB en uitgangsvermogen versus toenemend ingangssignaal, waaruit een verzadigingsvermogen van 18,4 dBm wordt afgeleid, wat de effectiviteit van de getaperde SOA als booster-versterker bevestigt.*

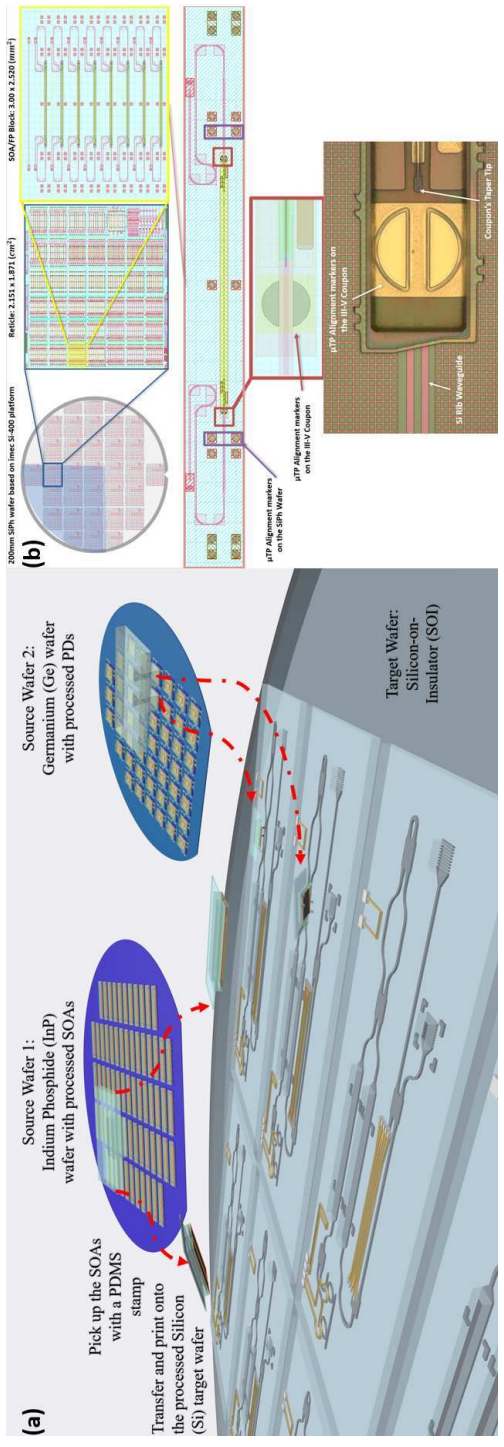
Naast telecomtoepassingen toont het proefschrift verschillende demonstrators die het laserplatform aanpassen voor biomedische sensing, spectroscopie, gasdetectie, programmeerbare fotonica en toepassingen met hoge coherentie-eisen. Zo wordt een µLens-gemonteerde laser-PIC gebruikt voor hartslagmonitoring via transmissie door de oorlel, terwijl een chip met meerdere geïntegreerde SOA's een uitgebreid afstembereik bereikt voor SWIR-spectroscopie. Een verpakte SiPh-laser met geïntegreerde golflengtemonitoring en vergrendeling wordt gedemonstreerd voor gasdetectie, en een hybride III-V-op-SiN laser bereikt lijnbreedtes onder de 25 kHz voor toepassingen zoals LiDAR. De programmeerbare fotonische chip, met dynamische herconfigureerbaarheid, illustreert verder de veelzijdigheid van het geïntegreerde laser- en versterkerplatform.




*Figuur 3: Demonstratoren die de veelzijdigheid van het III-V-op-Si laserplatform buiten telecomtoepassingen aantonen. (a) μLens-gemonteerde laser-PIC gebruikt voor biomedische sensing via hartslagmonitoring door transmissie via de oorlel. (b) Hybride III-V-op-SiN laser met lijnbreedtes onder de 25 kHz voor toepassingen waarbij coherentie cruciaal is, zoals LiDAR. (c) Verpakte SiPh-laser met geïntegreerde golflengtemonitoring en vergrendeling voor gassensing. (d) Programmeerbare fotonische chip met dynamische herconfigureerbaarheid, die de brede inzethbaarheid van het geïntegreerde laser- en versterkerplatform illustreert.*

Het laatste deel van het proefschrift behandelt de overgang van chip- naar wafer-niveau $\mu$TP-integratie. Dit werk werd uitgevoerd binnen de Transverse pilotlijn, waar essentiële tools zoals de EVG®101 spray coater voor uniforme BCB-depositie en de ASMPT Amicra NANO printer voor geautomatiseerde $\mu$TP werden geïntroduceerd. Een reeks ontwerpstudies werd uitgevoerd om de uniformiteit van de BCB-dikte te optimaliseren, wat de basis vormt voor wafer-scale $\mu$TP. De eerste wafer-niveau $\mu$TP-integratie van III-V componenten op een 200 mm SiPh wafer werd gedemonstreerd binnen deze pilotlijn, met submicron uitlijningsnauwkeurigheid en een printopbrengst van 100%.

Tot slot bevestigt dit proefschrift micro-transferdruk als een schaalbare en produceerbare technologie voor heterogene fotonische integratie. Het levert een volledig kader, van ontwerp en fabricage van componenten tot systeemdemonstraties en pilootlijnontwikkeling, en positioneert $\mu$TP als een sleuteltechnologie voor de volgende generatie fotonische systemen.




*Figuur 4: Overgang van chipniveau naar waferniveau µTP-integratie binnen de Transverse pilotlijn. (a) Overzicht van µTP-integratie op wafer-schaal. (b) Demonstratie van µTP-integratie op wafer-schaal van III-V-coupons op een 200 mm SiPh-wafer, met submicron uitlijningsprecisie en een printopbrengst van 100%.*

# English summary

This thesis presents a comprehensive investigation into the development of narrow-linewidth, widely tunable III-V-on-silicon lasers and high-saturation-power semiconductor optical amplifiers (SOAs), realized through micro-transfer printing ($\mu$TP) integration technology. The work addresses the growing demand for scalable, high-performance photonic integrated circuits (PICs) by leveraging the versatility and precision of $\mu$TP to integrate III-V gain materials onto silicon photonics (SiPh) platforms. It builds upon a strong foundation of previous research within the Photonics Research Group (PRG), extending earlier concepts and architectures to create solutions that are broadly adaptable across different applications and platforms.

The thesis begins by contextualizing the evolution of optical communication networks, emphasizing the shift from copper-based interconnects to high-bandwidth, low-loss optical fiber systems. With the exponential growth of data traffic driven by cloud computing, video streaming, and AI workloads, the need for compact, energy-efficient, and high-speed photonic solutions has become critical. Silicon photonics, compatible with CMOS fabrication, offers a promising platform for scalable integration, but lacks native light sources due to silicon's indirect bandgap.

To overcome this limitation, the thesis explores various integration techniques for incorporating III-V materials onto SiPh platforms, including hybrid, heterogeneous, and micro-transfer printing methods. Among these, $\mu$TP emerges as a particularly powerful approach, enabling the selective and scalable integration of pre-fabricated III-V devices onto silicon with sub-micron alignment precision. The $\mu$TP process is described in detail, including the principles of kinetically switched adhesion, device release via tethering, and the use of PDMS stamps for transfer.

The core contribution of the thesis is the design and demonstration of ultra-wide tunable narrow-linewidth III-V-on-Si lasers. These lasers are integrated on IMEC 400nm+ silicon photonics platform using $\mu$TP of pre-fabricated SOAs, based on previous works from the PRG and with a laser architecture intentionally designed to be compatible and easily adaptable for a variety of applications and platforms. The laser architecture incorporates Vernier-filtered microring resonators and Sagnac loop mirrors to achieve single-mode operation and linewidth reduction. A dual-laser configuration is introduced to extend the tuning range beyond the gain bandwidth of individual SOAs, resulting in a combined tuning span of over 110 nm. Linewidth measurements using OEwaves OE4000 confirm Lorentzian linewidths well below the 400G-ZR standard threshold of 500 kHz, with values as low as 13 to 170 kHz across the tuning range.

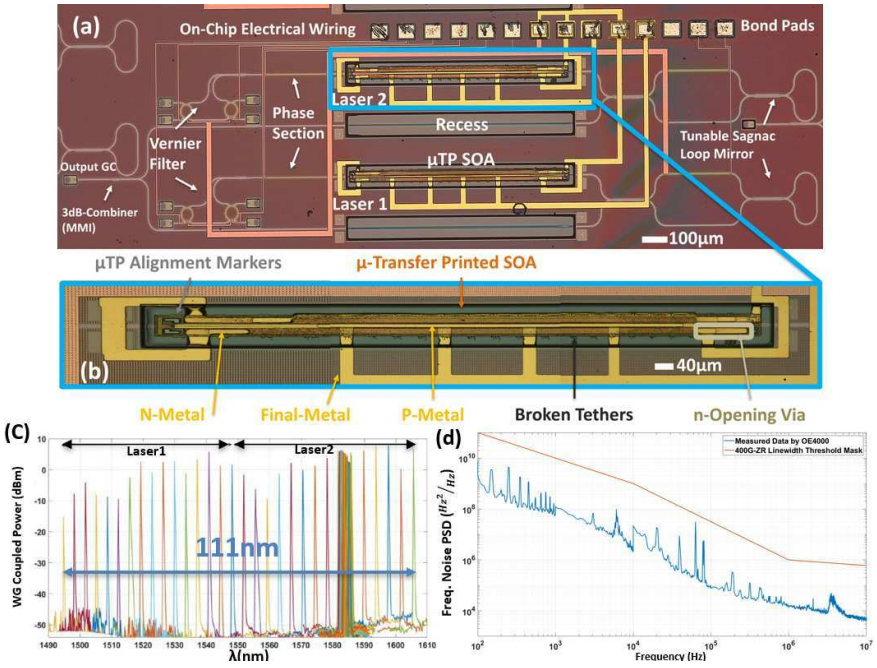



*Figure 5: Demonstration of ultra-wide tunable narrow-linewidth III-V-on-Si lasers integrated on IMEC 400nm+ platform. (a) Schematic of the laser architecture featuring Vernier filters based on microring resonators and Sagnac loop mirrors for single-mode operation and linewidth reduction. A dual-laser configuration enables tuning beyond the gain bandwidth of individual SOAs. (b) Close-up of transfer-printed SOA with final metallization. (c) Measured tuning range exceeding 110 nm across the combined laser spectrum. (d) Linewidth characterization using OEwaves OE4000 confirms Lorentzian linewidths well below the 400G-ZR threshold of 500 kHz.*

To further enhance the laser's output power, a novel tapered SOA design is proposed and realized. This hybrid III-V-on-Si amplifier features a gradually widening active region and silicon waveguide, optimizing the confinement factor and cross-sectional area to increase saturation power while maintaining gain. Analysis of the experimental results calculates an output saturation power of 18.4 dBm and a wall-plug efficiency of 3.5%, confirming the effectiveness of the tapered SOA design as a booster amplifier.

Beyond telecom applications, the thesis showcases several demonstrators that adapt the laser platform for biomedical sensing, spectroscopy, gas detection, programmable photonics, and coherence-critical systems. For example, a µLens-mounted laser PIC is used for heartbeat monitoring via earlobe transmission, while a multi-SOA integrated chip achieves extended tunability for SWIR spectroscopy. A packaged SiPh laser with integrated wavelength monitoring and locking is demonstrated for gas sensing, and a hybrid III-V-on-SiN laser achieves linewidths below

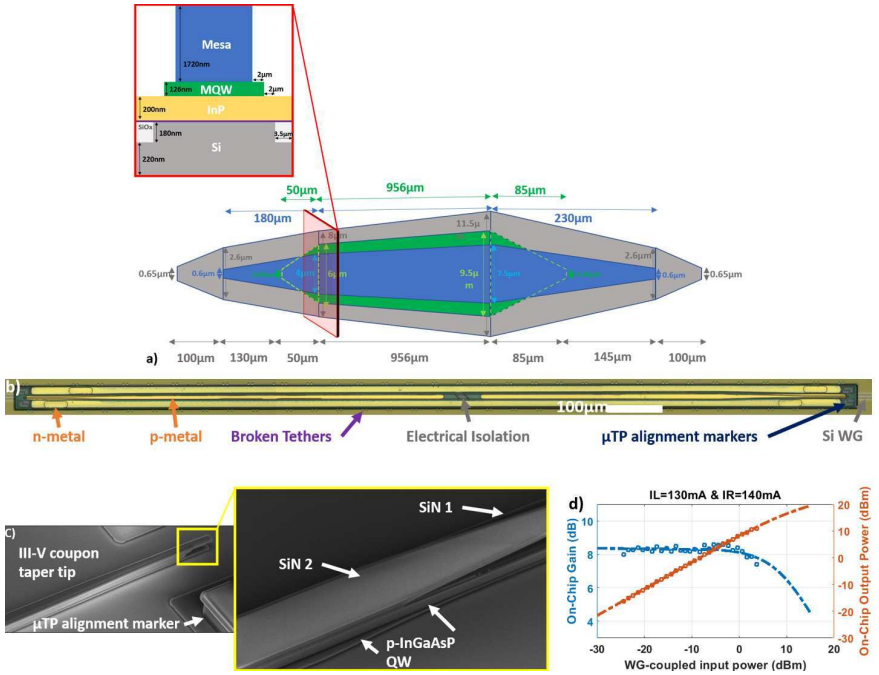



*Figure 6: Demonstration of a novel hybrid III-V-on-Si tapered design for high saturation power SOAs. (a) Schematic of the tapered SOA structure with a gradually widening active region and silicon waveguide to optimize optical confinement and increase saturation power. (b) Microscope image of the transfer-printed SOA on an E-beam rapid prototyping silicon sample. (c) SEM cross-sectional view of the taper tip and µTP alignment markers. (d) Measured on-chip gain of 8.36 dB and output power versus increasing input power, leading to extraction of a saturation output power of 18.4 dBm, validating the tapered SOA as an effective booster amplifier.*

25 kHz for applications such as LiDAR. The programmable photonic chip, featuring dynamic reconfiguration capabilities, further illustrates the versatility of the integrated laser and amplifier platform.

The final part of the thesis addresses the transition from chip-level to wafer-level $\mu$TP integration. This work was carried out within the Transverse pilot line, where essential tools such as the EVG®101 spray coater for uniform BCB deposition and the ASMPT Amicra NANO printer for automated $\mu$TP were introduced. A series of design experiments was conducted to optimize BCB thickness uniformity, forming the basis for wafer-scale $\mu$TP. The first wafer-scale $\mu$TP integration of III-V coupons onto a 200 mm SiPh wafer was demonstrated within this pilot line, achieving sub-micron alignment precision and 100% printing yield.

In conclusion, this thesis establishes micro-transfer printing as a scalable and manufacturable technology for heterogeneous photonic integration. It delivers a complete framework, from device design and fabrication to system-level demon-

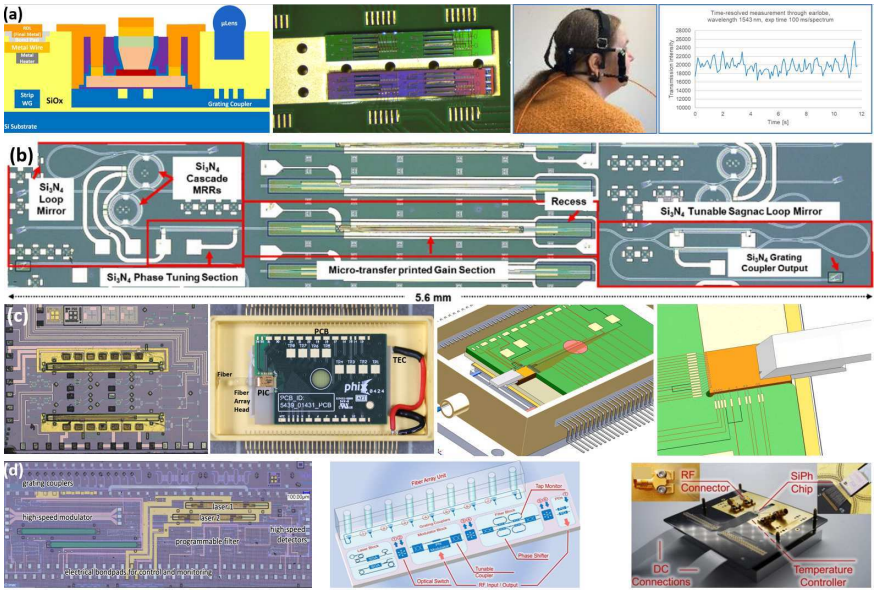



*Figure 7: Demonstrators showcasing the versatility of the III-V-on-Si laser platform beyond telecom applications. (a) μLens-mounted laser PIC used for biomedical sensing via heartbeat monitoring through earlobe transmission. (b) Hybrid III-V-on-SiN laser achieving linewidths below 25 kHz for coherence-critical applications such as LiDAR. (c) Packaged SiPh laser with integrated wavelength monitoring and locking for gas sensing. (d) Programmable photonic chip with dynamic reconfiguration capabilities, illustrating the adaptability of the integrated laser and amplifier platform.*

strations and pilot-line development, positioning $\mu$TP as a key enabler for next-generation photonic systems.

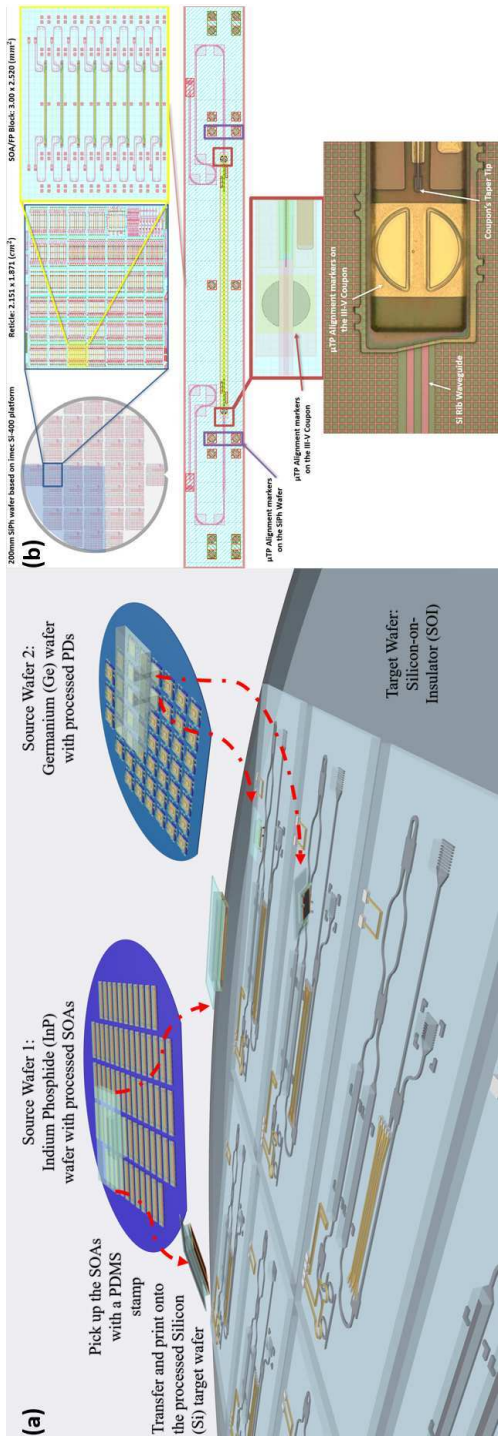



*Figure 8: Overgang van chipniveau naar waferniveau µTP-integratie binnen de Transverse pilotlijn. (a) Overzicht van µTP-integratie op wafer-schaal. (b) Demonstratie van µTP-integratie op wafer-schaal van III-V-coupons op een 200 mm SiPh-wafer, met submicron uitlijningsprecisie en een printopbrengst van 100%.*

# 1 Introduction

This thesis explores research conducted in the realm of silicon photonics, specifically concentrating on the integration of lasers and semiconductor optical amplifiers. The initial chapter provides a comprehensive review of optical communication links and the rationale behind the transition to integrated photonics, with a particular emphasis on silicon photonics. Subsequently, the current state of integration techniques, research objectives, and an overview of the thesis structure are presented.

## 1.1 Optical Fiber Network

The commencement of fiber-optic communications marked a pivotal moment with the creation of the first low-loss optical fibers and the successful demonstration of laser operations at room temperature. In 1976, Bell Laboratories conducted the initial experimental data transmission at a bit rate of 44.736 Mbps [1]. Subsequent advancements in technologies like wavelength-division multiplexing (WDM) and time-division multiplexing (TDM), coupled with significant enhancements in optical fiber capacity, resulted in achieving over 2 Pbps data transmission through a single fiber [2].

Concurrently, in the 1980s, the Internet became publicly accessible as the World Wide Web (WWW) [3]. With the recent surge in social network platforms (e.g., Facebook, Instagram), cloud computing (e.g., Amazon Web Service), video-on-demand services (e.g., YouTube, Netflix), and particularly following the global

lockdown due to the Covid-19 pandemic, the utilization of online communication services (Zoom, Microsoft Teams, etc.) propelled world data traffic to approximately 292.8 Exabytes (EB) per month by 2022. To contextualize the internet boom from 2018 to 2022, this figure stood at 77.1 EB per month in 2017 [4].

Cisco's reported compound annual growth rates (CAGR) of 6 percent for internet users and 10 percent for devices, as illustrated in Fig. 1.1 and Fig. 1.2, respectively [5], attest to the remarkable expansion. This growth owes much to the evolution of optical fiber technology, which facilitated the shift from lossy electrical copper connections to low-loss, high-bandwidth optical fiber networks. This transition enabled intercontinental connectivity and data-stream multiplexing [6]. Figure 1.3 portrays the deployment of fiber optic cables at the bottom of seas and oceans, where more than 600 cables, with a cumulative length exceeding 1.4 million kilometers, have been laid [7, 8].

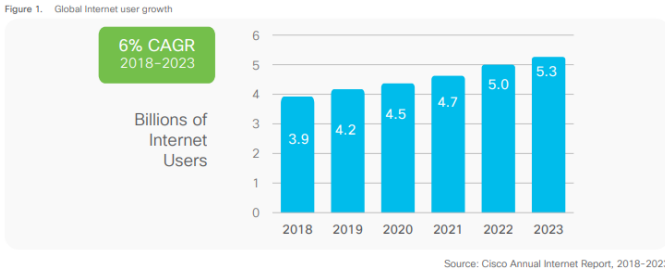



*Figure 1.1: Global Internet user growth (Cisco) [5].*

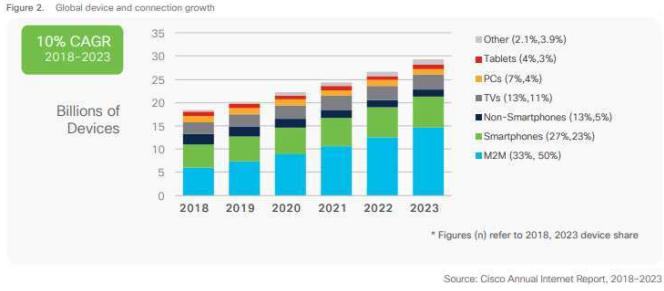



*Figure 1.2: Global device and connection growth (Cisco) [5].*

Nevertheless, as data rates soared, accommodating data transfer within other network spaces, such as data centers, presented new challenges. Efficient and high-speed communication between servers inside a data center emerged as a focal point for research.

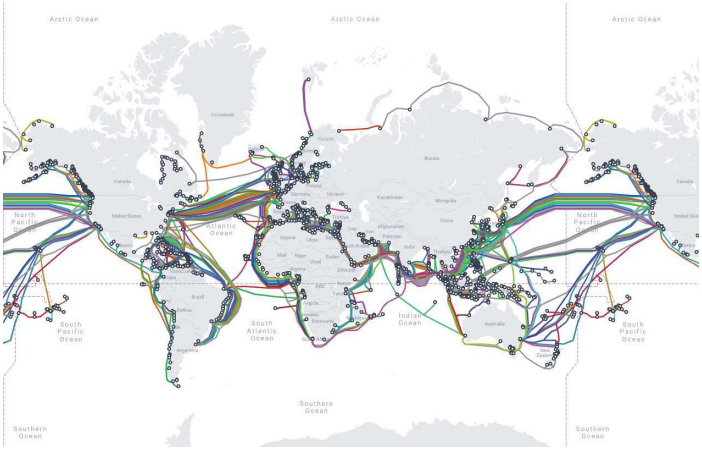


*Figure 1.3: Submarine optical fiber connections. Reproduced from [8].*

### 1.1.1 Optical Fiber Communication Links

Figure 1.4 illustrates a simplified optical communication link. The main components of the transmitter include a laser producing a continuous-wave optical signal at a specific wavelength ($\lambda$) and an external modulator that transforms this signal into a modulated digital bit sequence generated by a central processing unit (CPU). Alternatively, a high-speed directly-modulated laser (DML), can be employed without external modulators [9–11].

The modulated optical signal travels through the optical fiber over distances, like long haul (6000-12000 km), metro (100-1000 km), short-haul (20-100 km) and access networks ($<$20 km) as shown in Fig. 1.5. At the receiving end, the receiver comprises a photodiode, converting the optical signal back into the electrical domain. Typically, upon reaching the end of the optical fiber, the signal may be distorted and attenuated. To address this, amplifiers and equalizers restore the original shape of the transmitted signal. Subsequently, digital signal processing (DSP) is applied to further process the signal.

The primary role of optical fibers is to carry light containing data, making the most crucial features of these fibers their attenuation and dispersion. The predominant optical fiber in today's networks is the single-mode silica fiber. This type has a slender silica core with a diameter of approximately 9 µm (50 µm and 62.5 µm in case of multi-mode) and a cladding that is 125 µm thick, with a slightly lower refractive index [14, 15]. This fiber demonstrates low loss and nearly zero dispersion in the O-band, along with minimal loss (0.2 dB/km) in the C-band. Consequently, the O-band is commonly used for short-reach, and the C-band for long-reach optical networks [14–16].

The lasers in transmitters need to operate within the O-band or C-band, deter-

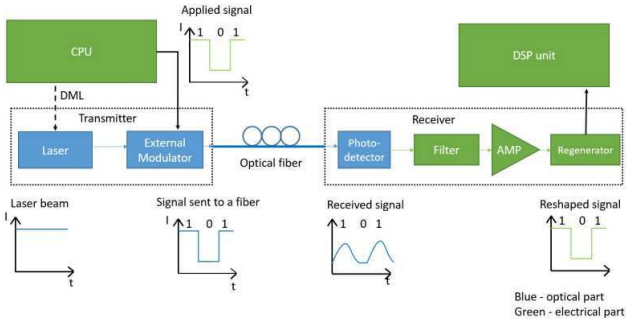



*Figure 1.4: Schematics of an optical communication link [12].*

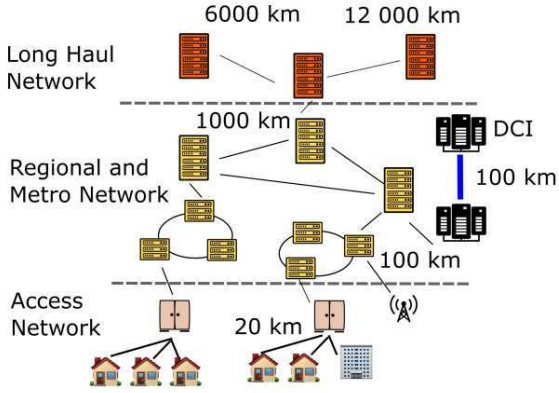



*Figure 1.5: Three levels of optical networks with different reach of the fibre-optic link. Reproduced from [13].*

mined by the fiber transmission windows as shown in Fig. 1.6. III-V semiconductors, such as InP [17] and GaAs [18], which have direct bandgaps, are well-suited for light emission. Various types of III-V lasers, chosen based on their characteristics and cost considerations, find application in optical transmitters. These include DFB lasers [13, 19], DBR lasers [20, 21], widely tunable and narrow linewidth lasers [22, 23], VCSELs [24, 25], and others.

### 1.1.2 Optical Interconnects

Optical interconnects offer advantages such as high bandwidth, low power consumption, and minimal latency compared to conventional copper interconnects used in electronics systems [27–30]. Currently, these solutions are being implemented for short-haul distances (up to 80 kilometers, connecting data centers) and

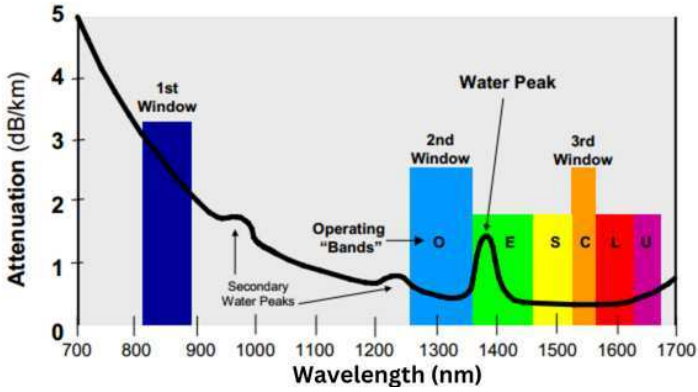



*Figure 1.6: Attenuation spectrum of optical fiber. Reproduced from [26].*

very-short-haul distances (up to 2 kilometers, within the data center, such as rack-to-rack, server to server, and board to board communication). However, the exploration of chip-to-chip or intra-chip optical interconnects is still in the research stage. Despite this, a comprehensive roadmap for an all-optical interconnect is already established, emphasizing strict criteria for high bandwidth and low power consumption [31]. These criteria not only address technical considerations but also play a crucial role in addressing environmental concerns, as increased electricity usage contributes to higher greenhouse gas emissions.

## 1.2 Integrated Photonics

The concept of integrated circuits (ICs) has played a pivotal role in the history of the electrical and electronics industry. By reducing the size of electronic components and integrating them into a compact circuit on a chip, the performance of the resulting electronic system has been greatly enhanced. Silicon (Si) has been the most important material for the electronics industry in recent history. The ability to fabricate very large-scale electronic integrated circuits with high throughput, high yield, and in large volumes based on complementary metal-oxide-semiconductor (CMOS) technology has made sophisticated high-tech gadgets, partially autonomous automobiles, state-of-the-art healthcare, and so on, both possible and affordable. This has significantly changed humans' lifestyles and improved their lives. Guided by Moore's law, semiconductor manufacturing technology has seen continuous improvements over the past six decades. Today, it's feasible to pack nearly 170 million transistors per square millimeter using the 3 nm CMOS technology node, which is the current state-of-the-art [32–34]. Currently, imec is developing a 2-nanometer node (2N) towards commercialization for industrial partners and has established its 20-year semiconductor roadmap toward

Angstrom nodes [35]. This miniaturization also yields other benefits, such as cost reduction, improved stability, and lower power consumption.

On the other hand, the invention of the laser by Maiman in 1960 marked a turning point in modern optics. A decade later, this led to the development of the first semiconductor laser capable of continuous wave output at room temperature [36, 37]. This pivotal accomplishment, coupled with advancements in low-loss optical fiber, paved the way for optical communication and spurred significant research interest in waveguide circuit technology.

Drawing inspiration from the success of integrated electronic circuits, S.E. Miller proposed the concept of integrated optics, the precursor to today's photonic integrated circuits (PICs), in 1969. This concept involves integrating various optical functions onto a single planar substrate and connecting them with low-loss waveguides [38]. Similar to integrated electronics, the miniaturization and integration of optical components on a single chip were later confirmed to be the only way to achieve high-performance, low-power, and low-cost optical systems.

Various waveguide platforms have been developed based on different material systems and manufacturing technologies such as Silica, Silicon-on-Insulator (SOI), III-V materials, Lithium Niobate, Polymer, etc. Each of these platforms has its own advantages and disadvantages, summerized in Table 1.1, determined by the properties of the materials used.

InP-based compound semiconductors and Si/Si3N4 photonic platforms are the dominant choices for today's photonic integrated circuits [16]. While the III-V platform allows complex circuits with a wide range of active optical functions, challenges in scaling InP wafer size and limited integration density hinder large-scale fabrication. In contrast, Si/Si3N4 photonics, with its potential for compact and sophisticated circuits, including CMOS compatibility, emerges as a competitive solution for the future. However, achieving elegant on-chip integrated optical sources remains a priority.

## 1.3 Silicon Photonics

### 1.3.1 Introduction

As electronic components shrink towards atomic dimensions, the electronics industry is adopting the "more than Moore" approach to enhance data center infrastructure integration. This means that future CMOS technology generations will need to not only reduce transistor sizes but also incorporate various integration technologies for innovative processing architectures [19], as it is included in imec's 20-year semiconductor roadmap [35]. Silicon, a common element found in sand, rocks, clays, and soils, is abundant on Earth and is a key component of the Earth's crust [54]. Its significance for Photonic Integrated Circuits (PICs) was

| Platform | Pros | Cons |
|---|---|---|
| Silica-on-Silicon | • Ultra low-loss waveguides [39]<br>• Fiber-matched waveguides [40]<br>• Possibility to integrate Er-doped optical sources & amplifiers | • Large bending radius (>2 mm)<br>• Less compact circuits<br>• Absence of electrically driven active components |
| Silicon-on-Insulator (SOI) | • Thick Si substrate for mechanical support<br>• Back-end layer with metal heaters [41]<br>• Transparency over 1.1-4 µm<br>• Low bending radius (>20 µm)<br>• Compact circuits and Low footprint<br>• Various efficient passive components<br>• Availability of modulators, photodiodes (PDs)<br>• CMOS compatible (scalable & low-cost) [42] | • Absence of lasers and amplifiers<br>• Two-photon absorption at Telecom wavelengths |
| Silicon Nitride (SiN) | • Ultra low-loss waveguides [43, 44]<br>• Transparency over visible and beyond [45, 46]<br>• Low thermal sensitivity<br>• No two-photon absorption at Telecom wavelengths | • Low thermal tuning ability<br>• Lower compactness [43, 44]<br>• Absence of lasers and amplifiers |
| III-V Semiconductors | • Availability of lasers and amplifiers in addition to the passives [47, 48]<br>• Availability of modulators and PDs | • Dedicated process line & flow<br>• Less maturity at scale & large volume production<br>• Costly material |
| Lithium Niobate ($LiNbO_3$) | • Large electro-optic coefficient<br>• Large acousto-optic coefficient<br>• Large piezoelectric coefficient<br>• Suitable for high-speed modulators [49]<br>• Low-loss [50] | • Large bending radius<br>• Less compact & Large footprint<br>• Mostly used for stand-alone devices |
| Polymers | • Various polymers have various transparency windows [51–53]<br>• Compatibility with various substrates<br>• Possibility to use for high-speed & low-voltage modulators<br>• Fabrication simplicity<br>• Low-cost material | • Less compactness<br>• Absence of lasers and amplifiers<br>• Reliability issues |

*Table 1.1: Various waveguide platforms, advantages and disadvantages.*

recognized when silicon waveguides and electro-optic effects were explored for telecommunication wavelengths [11]. Silicon Photonics (SiPh) technology, which allows photonic components to be integrated on a silicon substrate using CMOS fabrication technology, is crucial in this regard. Silicon-on-Insulator (SOI) is one of the most promising platforms in the SiPh field. The established CMOS electronics industry facilitates the cost-effective production of these photonic devices in large quantities. An SOI wafer consists of a silicon substrate (200-mm and 300-mm wafer sizes), a 1-3 µm thick thermally grown silicon oxide layer, and a silicon device layer (220 nm, 400 nm, 500 nm, or 3 µm thick) [9–11]. Its distinguishing feature is the high refractive index contrast between the Si and SiO2 layers, which allows for high optical confinement in Si-waveguides, sub-micrometer geometries, and tight bends with low loss. Over the years, passive optical functionalities with excellent small-footprint have been developed, including high confinement low-

loss waveguides [55, 56], waveguide bends with several micron radii [57], low-loss waveguide crossings [58], Bragg gratings [59], high Q-ring resonators [60], arrayed waveguide gratings [61], grating coupler structures [62], and more. By selectively doping silicon and growing germanium (Ge) epitaxially, active functionalities can be added to PICs, such as carrier-based modulators [63] and high-speed photodetectors [64]. These building blocks enable the creation of complex PICs for a wide range of applications, which in Fig. 1.7 SiPh's cumulative annual growth rate forecast by application is provided by Yole Group [65]. Silicon photonics has matured significantly, with numerous silicon optical transceivers now available on the market [64, 66, 67] with compound annual growth rate of 44.5% as forcasted in Fig. 1.8 [68] with a worldwide value-chain as depicted in Fig. 1.9 [69].

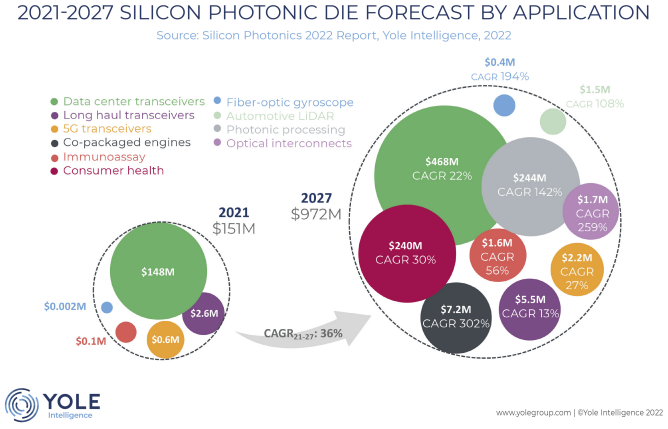



*Figure 1.7: Silicon photonic die forecast by application (Yole Group) [65].*

This progress would not have been possible without the development of Si photonics technology platforms in CMOS fabs. However, indirect bandgap structure makes it impossible to realize efficient light sources in silicon or germanium, as shown in Fig. 1.10. This leads to complicated assemblies of light sources with Si PICs, hindering further cost reduction of products [16]. Therefore, versatile and low-cost efficient integration of III-V materials onto SOI is required to realize efficient light sources at 1.3 or 1.55 µm [70].

### 1.3.2 IMEC Silicon Photonics Platforms

Multi-project-wafer (MPW) runs in photonic technology serve as a cost-effective solution for researchers, fabless research groups, and small companies to access advanced fabrication processes without bearing the entire manufacturing costs

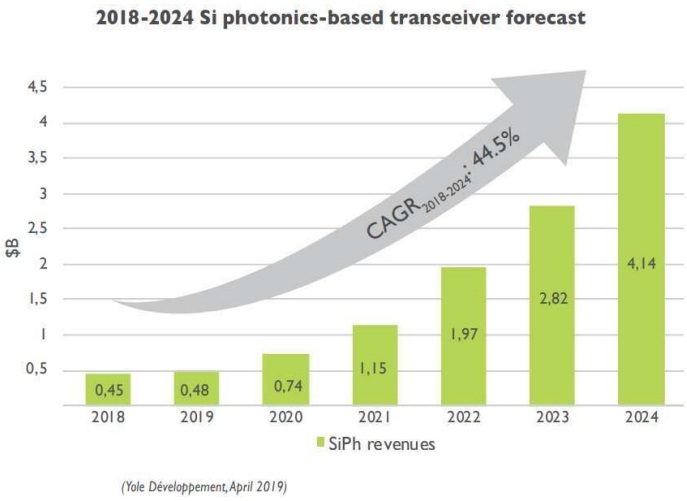



*Figure 1.8: Si Photonics-based transceiver forecast 2018-2024 (Yole Group) [68].*

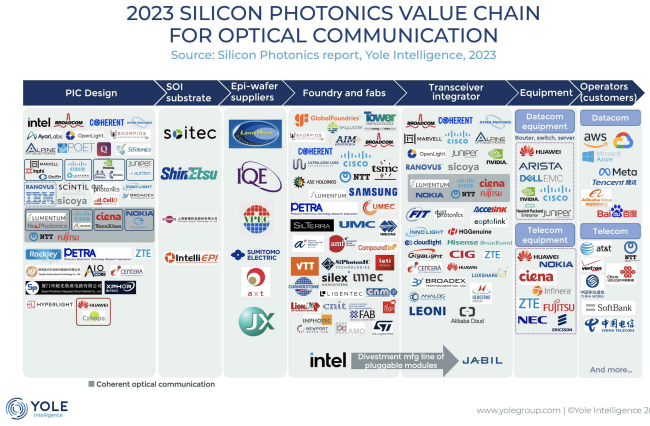



*Figure 1.9: Silicon photonics value chain for optical communication (Yole Group) [69].*

themselves. In an MPW run, multiple designs from different entities are fabricated together on a single wafer as shown in Fig. 1.11, sharing the production costs. This collaborative approach significantly reduces the financial burden, making it feasible for entities with limited resources to experiment with various designs, test new concepts, and validate prototypes.

The concept of MPW relies heavily on the availability of a process development kit (PDK), which essentially acts as a standardized set of design rules, models, and parameters provided by foundries such as imec, AMF, CEA-LETI, IHP,

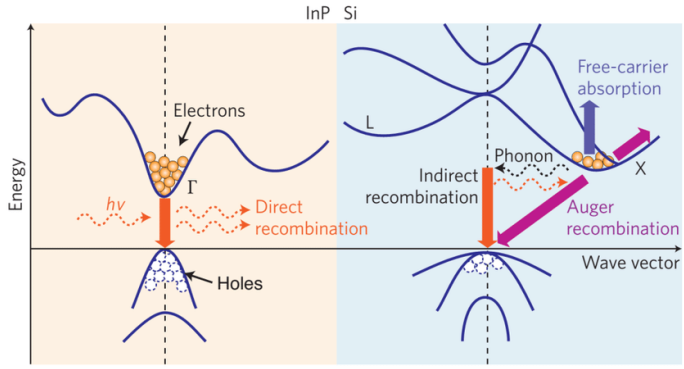



*Figure 1.10: Energy band diagrams and major carrier transition processes in InP (direct bandgap) and silicon crystals (indirect bandgap) [70].*

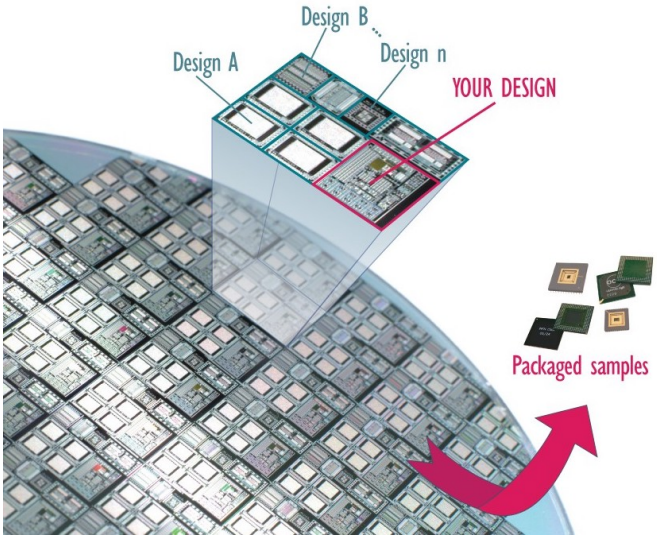



*Figure 1.11: Multi-project-wafer concept [71].*

LioniX, LIGENTEC, etc (See Fig. 1.9 representing worldwide SiPh foundries). These PDKs encapsulate the fabrication process details, allowing designers to develop their photonic integrated circuit (PIC) designs with confidence that they will be compatible with the foundry's fabrication process. By adhering to these standardized guidelines, designers can ensure successful fabrication during the MPW runs, streamlining the entire design-to-fabrication workflow. As an example, figure 1.12 shows imec's iSiPP PDK toolbox.

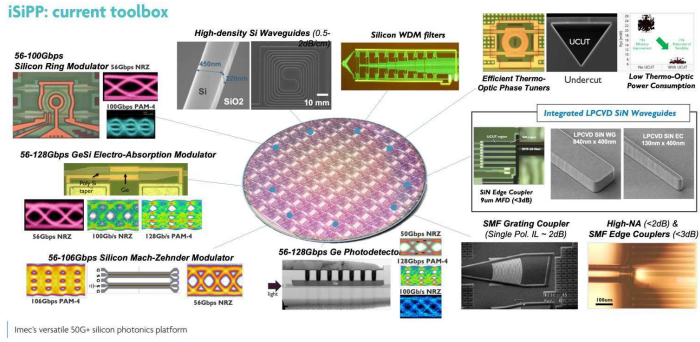



*Figure 1.12: Process Design Kit concept, imec iSiPP toolbox [72].*

Imec, a leading research and innovation hub in nanoelectronics and digital technologies, offers comprehensive PDKs tailored for MPW runs in photonic technologies [73, 74]. These PDKs enable designers to access cutting-edge fabrication processes and advanced materials, empowering them to innovate and explore new possibilities in photonics. Through imec's MPW services, researchers and companies can leverage shared resources, accelerate their development cycles, and bring their photonic designs to fruition more efficiently and economically. Access to imec's MPW services is feasible through EUROPRACTICE platform [75, 76].

EUROPRACTICE is a European consortium established by the European Commission in 1995 as a successor of EUROCHIP (1989-1995) to enhance European industrial competitiveness in the global market of semiconductor technologies [77]. It lowers the barriers for academia to exploit the latest technologies in their research, innovation, and the training of the large numbers of highly-skilled graduates demanded by industry. EUROPRACTICE offers affordable MPW services for ASICs, MEMS, photonics, microfluidics, and power electronics. Furthermore, it provides affordable access to a wide range of CAD tools, training courses, and state-of-the-art fabrication technologies. EUROPRACTICE supports academic institutions, spinouts, and small and medium-sized enterprises (SMEs) with IC prototyping services, system integration solutions, training activities, and possibilities for small volume production. It provides European SMEs and start-ups with a true one-stop shop that provides all required to design and fabricate semiconductor devices and systems in a supported cost-effective way with clear routes to prototype fabrication, commercialization, and volume production.

**IMEC Passive 400 nm (Si-400 nm)** The imec in-house SiPh passive platform, known as Si-400 nm, is based on 200 mm silicon wafers featuring a 2 µm buried oxide (BOX) layer and a 400 nm silicon top layer. A typical etch depth of 180 nm is applied to form rib waveguides. The Si-400 nm platform, illustrated in Fig.

1.13, supports a wide range of passive photonic components, including waveguides, directional couplers, and filters, making it well-suited for applications in telecommunications, data communications, and optical sensing.

Being CMOS-compatible, this platform enables high-density integration and cost-effective manufacturing. Its low-loss characteristics and high performance make it especially attractive for passive photonic circuits. At UGent-imec, the Photonics Research Group (PRG) extensively utilizes the Si-400 nm platform for the development of hybrid-integrated lasers and SOAs, leveraging the high-efficiency evanescent coupling enabled by this architecture [16, 78, 79].


*Figure 1.13: IMEC Si-400 nm Platform (Size proportions are not preserved for illustrative clarity).*

**IMEC Passives+ Platform** Building on the same 200 mm wafer infrastructure, the imec Passives+ platform incorporates more advanced capabilities through 193 nm lithography and multiple silicon etch depths. It features three etching options: a 70 nm shallow etch, a 150 nm socket etch, and a full 220 nm etch, enabling versatile photonic functionality integration on a single chip. In addition, a patterned poly-silicon (poly-Si) layer is included to enhance the efficiency of grating couplers for vertical coupling to optical fibers. The platform also offers flexible top-cladding options, including air cladding or a high-density plasma (HDP) oxide cladding. The latter undergoes chemical-mechanical polishing (CMP) to create a planar, no-topography side oxide cladding, beneficial for uniform device performance. A schematic overview is presented in Fig. 1.14 [12, 74].

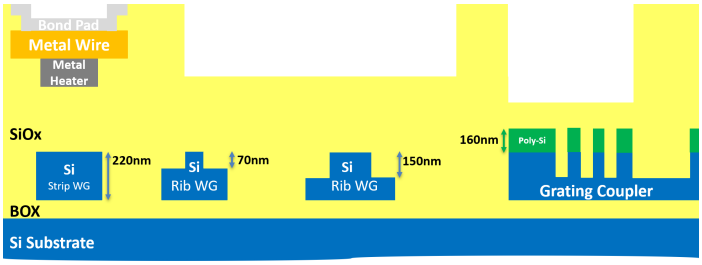



*Figure 1.14: IMEC Passives+ platform (Size proportions are not preserved for illustrative clarity).*

**IMEC 400nm+ Platform** The IMEC 400nm+ platform, shown in Fig. 1.15, is based on IMEC Si-400 nm technology and was originally developed for medical applications as part of the MedPhab project. It includes both partial 180 nm and full 400 nm silicon etching, along with backend processing that adds a 2 µm $SiO_x$ layer above the device layer. Metal heaters, electrical interconnects, and bondpads are integrated to enable electro-optical tunability.

In this work, we fabricate integrated lasers on this platform for several reasons:

- **Efficient coupling:** The 400 nm Si thickness enables high-efficiency evanescent coupling, consistent with the IMEC Si-400 nm platform.
- **Thermal tunability:** The backend processing of IMEC 400nm+ allows the incorporation of thermally tuned elements into the circuit.
- **Prototyping suitability:** The overall stack remains relatively simple, which results in shorter fabrication lead times compared to more complex platforms such as IMEC Passives+ and iSiPP50G. This makes it particularly suitable for prototyping.
- **Cross-platform compatibility:** Only minimal modifications (as described in Chapter 2, Section 2.2.1.4) are required to adapt the demonstrated laser and SOA for other SiPh platforms. Examples include adding a 160 nm poly-Si layer on top of the 220 nm Si waveguide in the IMEC iSiPP50G platform for efficient evanescent coupling, or adjusting the hybrid taper design for SiN platforms.

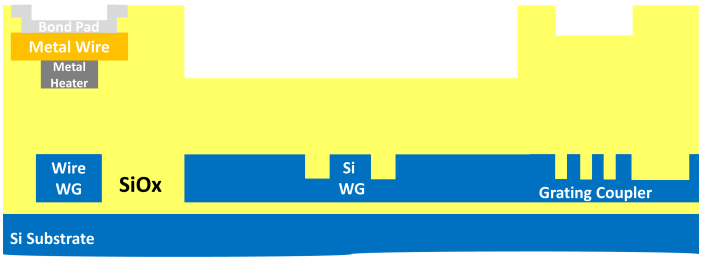



*Figure 1.15: IMEC 400nm+ Platform (Size proportions are not preserved for illustrative clarity).*

**IMEC iSiPP50G Platform** The iSiPP50G platform shown in Fig. 1.16, in addition to its passive silicon structures with various etching steps, provides four levels of p- and n-type doping, an extra poly-Si layer, a Ge epitaxial layer, and two tiers of metal interconnects (Metal 1 and Metal 2). By integrating a broad range of passive and active 50Gbd components into a single platform, it aims

to deliver cost-effective, high-performance 50Gb/s non-return-to-zero (NRZ) and 100Gb/s pulse-amplitude-modulation 4-level (PAM-4) optical link solutions for both telecom and datacom (see Fig. 1.12). Key elements like high-speed carrier-depletion Si modulators, Ge electro-absorption modulators, Ge photodetectors, efficient grating couplers, efficient edge couplers, and thermo-optic phase shifters have all passed reliability qualifications. The platform's versatility also allows for other integrated photonics applications, such as coherent LiDAR, bio-sensing, computing, and more [72, 74].

Imec provides specialized and adaptable silicon photonics prototyping and production services, tailored to the requirements of an individual partner, on both 200 mm and 300 mm wafers (known as iSiPP200 and iSiPP300) [72]. This service enhances the iSiPP50G offering with process customization options like low pressure chemical vapor deposition (LPCVD) SiN waveguides for high power handling and filter synthesis, silicon oxide nitride (SiON) edge couplers, local undercut (UCUT) for thermal insulation, among others. For additional optional modules on iSiPP200 and iSiPP300, refer to the imec platform services [72–74].

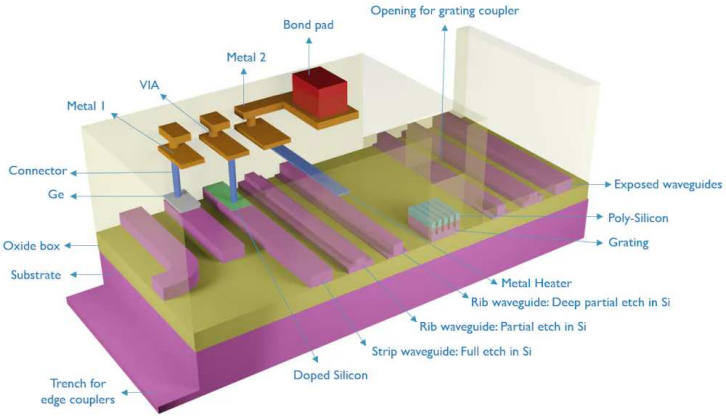



*Figure 1.16: IMEC iSiPP50G Platform [74].*

## 1.4 Integration Techniques for Silicon Photonics

While the SiPh platform may be perfect for the low-cost dense integration of large-scale PICs, its indirect band gap poses a challenge to incorporate efficient electrically-pumped laser sources and amplifiers. As mentioned earlier, III-V semiconductor materials have a direct bandgap, making them highly suitable for light emission, modulation, and detection. Furthermore, the emission of the III-V alloys can be adjusted by altering the composition of the alloys. Consequently,

over the past few years, substantial efforts have been dedicated to developing mature technologies for the cost-effective integration of III-V-on-Si lasers and other non-inherent functionalities on Si PIC. There are several integration strategies, which fall into two primary categories: Hybrid and Heterogeneous integration. Each approach has its own advantages and disadvantages, which we will discuss in the following sections.

### 1.4.1 Hybrid Integration

As depicted in Fig. 1.17, the hybrid integration method encompasses all integration techniques that involve the optical linkage of photonic device chips, like lasers, to a neighboring SiPh circuit. This method allows the high performance of the III-V gain chip to be preserved on its native substrate. Subsequently, we will discuss various techniques of hybrid integration.

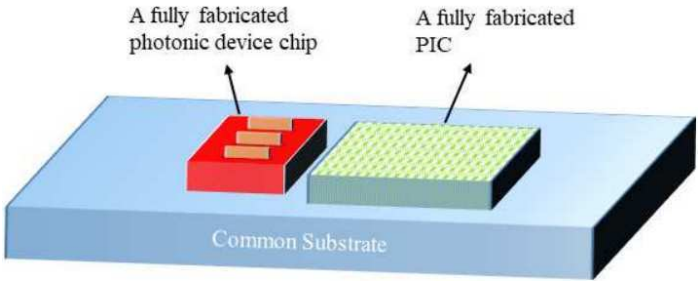



*Figure 1.17: A simple schematic of the hybrid integration technique. A gain chip is placed next to a Si PIC where both chips are mounted on a separate common substrate [19].*

**Photonic Wire Bonding** Photonic Wire Bonding (PWB) is an optical integration and packaging technique [80] that connects various optical components using free-form wires created by beam-shaping elements, resulting in low insertion loss [81, 82]. This connection can be established between two silicon photonics chips or from an independent component like a laser to a silicon photonics chip. Fig. 1.18 shows a scanning electron microscope (SEM) micrograph of a multi-chip assembly of passive silicon photonic waveguides with an InP DFB laser array using wire bonds. The process involves mounting the chips on a shared substrate, applying photoresist, using automated image recognition software for alignment, and then conducting a direct-write two-photon laser lithography [83]. Finally, the photonic wire bonds are encapsulated using a lower refractive index material. A low optical insertion loss of 0.4 dB per bond has been reported when connecting InP-based edge-emitting laser diodes to a passive silicon photonic circuit [84]. The technique

allows for high optical misalignment tolerance but doesn't scale well with a large number of optical interfaces [19].

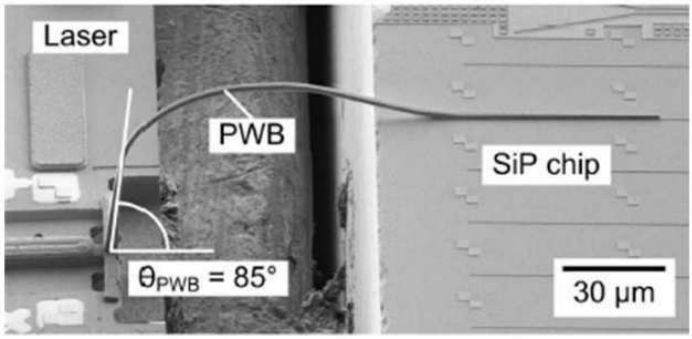



*Figure 1.18: A side-view SEM image of PWB, connecting an InP DFB laser chip to a waveguide on a SiP chip [84].*

**Butt-Coupling** This method involves coupling light between chips on the same plane, meaning the light beam is laterally coupled in or out between chips [19]. To achieve high coupling efficiencies (typically over 80%), high-quality facets must be created on all components involved, and the mode matching requirement must be fulfilled [85]. Figure 1.19 shows a schematic of a III-V chip butt-coupled to a SiN extended cavity. Lionix demonstrated up to 100 mW of on-chip optical power by butt-coupling multiple gain sections that share a common laser mirror [86].

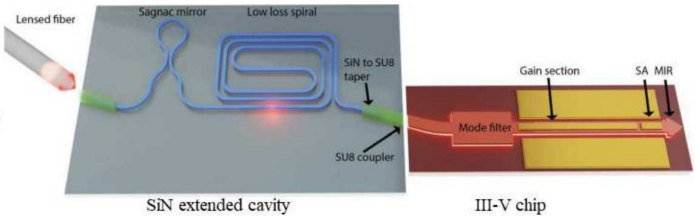



*Figure 1.19: Schematic view of a butt-coupled III-V chip to a SiN extended cavity [87].*

**Flip-Chip** Flip-chip bonding, shown in Fig. 1.20, a traditional integration method, has been extensively employed for assembling electronic ICs onto a substrate. The procedure entails depositing solder bumps on the bond pads of the desired chip, inverting the chip for alignment with the corresponding bond pads on the substrate, and then executing a reflow process to solidify the solder bumps for dependable electrical connections [16]. This method, first pioneered by IBM in the late 1960s and referred to as controlled collapse chip connection (C4) for microelectronic

assembly [19, 88], directly links face-down electrical or optical components as well as micro-electro-mechanical systems (MEMS) to the substrate using solder or conductive polymer bumps [89].

In the last two decades, flip-chip bonding has been widely used to incorporate III-V active components on SiPh platforms [19, 90–95]. The III-V active components are manufactured on their native substrate using established standard III-V processes and can be evaluated before integration on the SiPh circuits. The integration process involves depositing AuSn as a solder, aligning both the III-V component and the substrate, and performing face-to-face integration using a flip-chip bonder. The in-plane alignment is done within the alignment accuracy of the machine. Nowadays, bonders have better than 0.5 μm of alignment accuracy [96]. Vertical alignment is typically achieved using mechanical stops. Array flip-chip integration is also possible, using a proper design of the integration interface [92, 96].

The flip-chip integration method enables the utilization of the superior features of readily manufactured III-V devices such as lasers, amplifiers, and photodetectors, and allows for pretesting before assembly, which improves the compound yield. However, the die-per-die operation makes the integration process slow and expensive. Nevertheless, flip-chipping continues to be the most recognized technology for integrating semiconductor devices and chips [12, 16, 19, 78, 97].

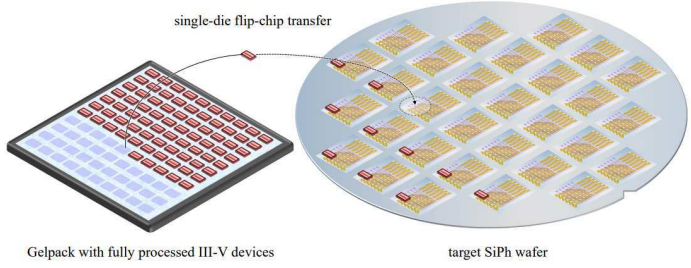



*Figure 1.20: Schematic view of flip-chip of a single device onto a SiPh wafer. Prior to the integration process, the devices are diced on the native substrate [97].*

### 1.4.2 Heterogeneous Integration

Heterogeneous integration is a process that involves the incorporation of a non-silicon element or thin layer onto a SiPh base. This differs from the hybrid integration method, as the III-V material is separated from its original substrate either prior to or following integration. Various methods of heterogeneous integration will be explored in the subsequent sections.

**Die- and Wafer-Bonding** The bonding of a III-V epitaxial layer structure onto a SOI platform is a prevalent heterogeneous integration technique. This process involves bonding an unprocessed III-V die or wafer to a pre-processed silicon photonics wafer (see Fig. 1.21), allowing for the integration of multiple dies or wafers with different functionalities on a single silicon photonics chip.

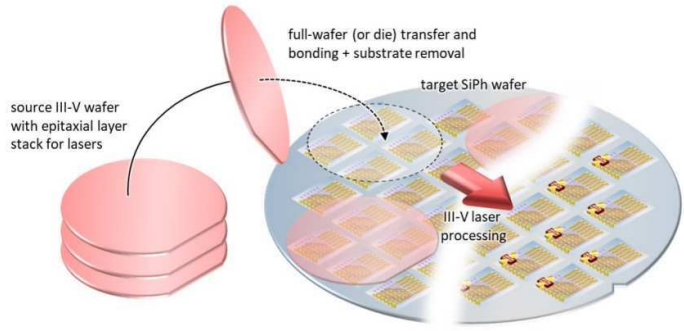



*Figure 1.21: Schematics of wafer bonding technology [12].*

Bonding techniques can be broadly classified into two categories: direct and adhesive bonding. Direct bonding involves the joining two surfaces directly by means of covalent bonds without any intermediate layers. However, this technique imposes stringent requirements, such as extremely high surface cleanliness [98, 99].

Adhesive bonding, on the other hand, uses an adhesive layer, typically DVS-BCB (divinylsiloxane-bis-benzocyclobutene), which mitigates these issues by planarizing the surface [100, 101]. This technique is highly tolerant to surface roughness and cleanliness, requires less surface preparation, and provides protection to the patterned features on the SOI. The annealing temperature required for a reliable bonding process is low (below 280°C). However, the low thermal conductivity of DVS-BCB compared to silicon and III-V materials can be a potential issue, especially in the integration of light sources [102, 103].

In addition to these, there are other bonding techniques such as molecular and metallic bonding. Molecular bonding involves the formation of a strong covalent bond between silicon and the III-V material using a thin film of a dielectric, resulting in a lower required annealing temperature and reduced surface roughness requirements [104]. Metallic bonding, which includes eutectic and thermocompression bonding, is typically used in the packaging of MEMS due to optical absorption and post-bonding fabrication limitations [105].

Instead of bonding two complete wafers, a die-to-wafer scheme can be employed where smaller III-V dies are bonded to allocated silicon dies on the target wafer, as shown in Fig. 1.22. This makes more efficient use of the costly III-V

material [97].

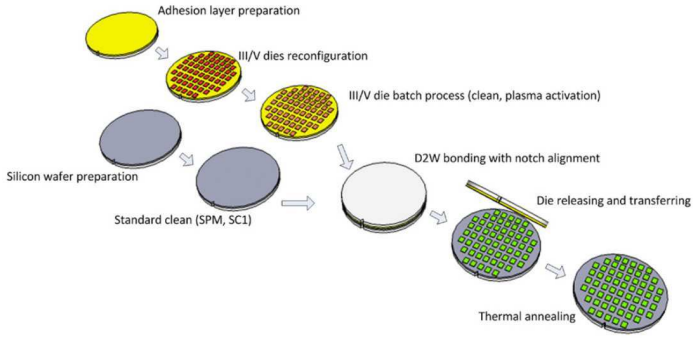



*Figure 1.22: Schematic process flow for multiple-die-to-wafer bonding. Reproduced from [16, 106].*

The molecular bonding technique has been largely developed at the University of California Santa-Barbara (UCSB) and CEA-LETI, while Ghent University pioneered the DVS-BCB adhesive bonding [101, 107]. The first membrane lasers on silicon waveguides were reported in 2006 [108, 109]. The molecular bonding integration method is currently commercialized by Intel in high volumes for telecom transceivers [110] and more recently by NexusPhotonics, who are wafer-bonding GaAs wafers onto SiNx photonic wafers for near-infrared and visible light applications [111].

**Epitaxial (Re-)growth of III-V on Silicon** Epitaxial III-V on silicon photonics aims to grow III-V crystals on a SOI wafer, a process that is complex due to the significant lattice mismatch between the III-V and silicon (8% between Si/InP), differences in thermal expansion coefficient, and the polar/non-polar interface [112]. Despite these challenges, solutions are being developed, such as aspect ratio trapping, where the III-V is grown in trenches on the Si wafer using metal-organic vapor phase epitaxy (MOVPE). This method allows for the growth of high-quality crystalline III-V material on top of the seeding layer, despite the initial high defect density [113].

Direct epitaxial growth, as shown in Fig. 1.23, is considered to be the ultimate solution for integrating III-V semiconductors on Si, but it is not yet mature enough for industrial use due to the challenges in growing high-quality, low threading dislocation density III-V layers on Si [78]. However, planar growth of III-V quantum dot stacks can be achieved by introducing intermediate layers like GaAs-on-V-grooved-Si (GoVS), a GaP buffer layer, or a dislocation filter layer. These approaches can significantly reduce the dislocation density [114–116].

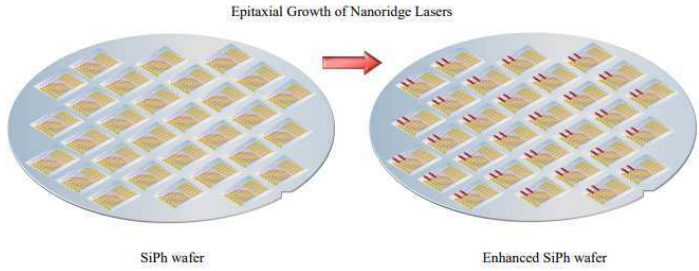



*Figure 1.23: Schematic of Hetero-Epitaxial growth, where III-V materials such as GaAs are grown as nanoridges on a silicon target wafer [97].*

In contrast to planar growth, selective-area growth (SAG) is an emerging technique for monolithically integrating III-V materials on Si without requiring thick buffer layers. In SAG, III-V materials are grown on patterned Si substrates masked by $SiO_2$, enabling controlled growth in the exposed regions and techniques such as directional heteroepitaxy, vertical/planar nanowires growth, and aspect ratio trapping to reduce the dislocation density [117].

Another recent method combines III-V wafer bonding and regrowth of the III-V active and/or passive layers (see Fig. 1.24), enabling co-integration of multiple III-V functional layers on SOI PICs. This method promises efficient coupling to the Si PICs, a low dislocation density, and scalable, cost-effective manufacturing. However, the thickness of the epitaxial layers grown istypically limited to 350 nm due to observed dislocations above this thickness [118], however recent research seems to be able to address this issue [119].

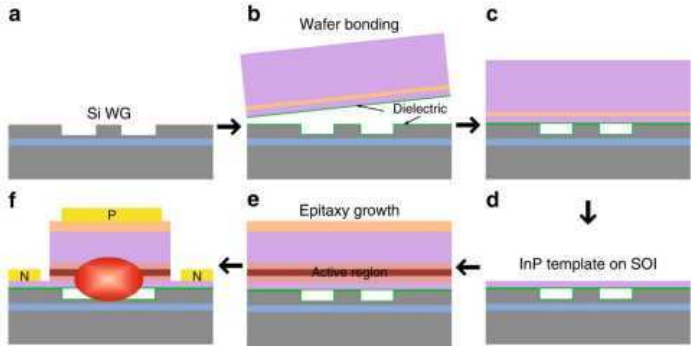



*Figure 1.24: Process flow schematic of regrowth on a bonding template III-V-on-Si integration [119].*

Ongoing efforts have led to recent demonstrations of InP and GaAs lasers epitaxially grown on Si [120, 121]. While direct III-V epitaxial growth is believed

to be the ultimate way to integrate light sources on a Si photonics platform, many difficulties must be overcome for it to become a mainstream approach [12, 78, 97].

**Micro-Transfer-Printing** Micro-transfer-printing ($\mu$TP), also known as transfer printing (TP), is a novel technique for heterogeneously integrating III-V devices on Si [122]. Developed by the Rogers group at the University of Illinois in 2004 [97, 123, 124], this technique allows for the manipulation of micrometer-sized thin film materials and devices. The process involves fabricating materials and devices in dense arrays on a source substrate, which can then be selectively picked using a polydimethylsiloxane (PDMS) stamp and printed on the target substrate [12, 16, 97, 122].

The technique offers several advantages. It enables area magnification, allowing devices densely integrated on a source wafer to be sparsely integrated on the target wafer [12, 122]. It is cost- and time-effective, with one printing cycle taking up to 45 seconds, thereby integrating tens to thousands of devices [16, 125]. Furthermore, $\mu$TP is a versatile technique that can be applied to virtually any thin-film device that can be released from its substrate [126].

$\mu$TP combines the advantages of flip-chip integration (pre-fabricating and pre-testing components on a source) and the wafer bonding technique (massively parallel integration) as shown in Fig. 1.25. Unlike flip-chipping, $\mu$TP allows for the simultaneous integration of arrays of devices, enabling a high throughput process [12]. Compared to wafer bonding, the silicon photonic process flow is not disturbed by the integration of the III-V devices, and the III-V processing can be done on the III-V source wafer [12]. Moreover, $\mu$TP allows for the intimate integration of different materials/devices on a single chip. This integration requires no modification of the Si photonics back-end process flow, except for a local back-end opening where the devices need to be integrated [16].

The technique is not limited to III-V device integration but can also be used for the integration of SiGe photodiodes and other Si-based devices [12]. It is a material-independent technique, allowing coupons from InP, GaAs, or GaSb material platforms to be picked up and printed on silicon or silicon nitride waveguide platforms to cover a much broader wavelength range [97].

Due to its versatility and potential for high-volume production of complex and ultra-compact PICs and electronic integrated circuits (EICs) at low cost, $\mu$TP has attracted a lot of attention in recent years [16]. It has been used for the wafer-scale integration of GaAs FP lasers on a Si substrate [127] and for the fabrication of micro-LED displays [128]. A more comprehensive examination of $\mu$TP is provided in section 1.4.3.

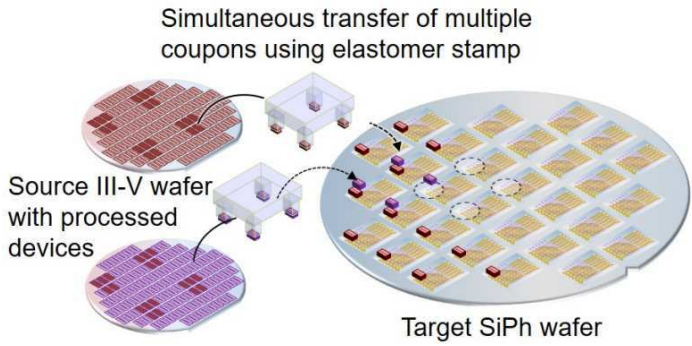



*Figure 1.25: Schematic of μTP-based integration in a parallel manner on 200 mm or 300 mm Si photonic wafers [16].*

### 1.4.3 Micro-Transfer Printing Integration Method

This section covers the operation principles of the transfer-printing integration method, followed by a short description of the general process flow of integrating III-V devices onto a silicon target. Afterwards, we look into the lab-scale printer apparatus housed in the UGent-imec cleanroom, which was employed for the integrations on sample scale conducted in this doctoral research.

**Operation principle** Micro-transfer-printing, a technology that allows prefabricated devices to be selectively picked from a source wafer and transferred to a target wafer while maintaining a constant pitch, relies on the use of an elastomeric PDMS rubber stamp [12]. The stamp is chosen for its high-resolution molding capabilities, chemical stability, non-toxicity, low mechanical stiffness, smooth surface, and viscoelastic properties [12, 16, 97]. These properties enable a kinetically switchable adhesion to the pre-fabricated devices (a.k.a. coupons) to be transferred [12].

The adhesion strength of the applied stamp to the surface of the film to be transferred (coupon) should be stronger than the adhesion of the film to the source substrate [12]. This is achieved by the PDMS exhibiting surface van der Waals forces with a relatively low surface energy, but the force can be high enough to pull the films from the source substrate [12, 16, 97].

The PDMS stamp material exhibits a viscoelastic effect, where the strength of the adhesion changes significantly with the peeling speed of the PDMS laminated with the film [12, 16, 97]. This is referred to as kinetically switched adhesion: fast separations lead to strong adhesion between the stamp and the device, while slow separations lead to weak adhesion [12, 16, 97].

The process of micro-transfer-printing is summarized as follows: When the PDMS stamp is applied to a patterned device or device array and one quickly peels

the stamp in the vertical direction, the forces are strong and the device is able to attach to the bottom of the PDMS stamp [12, 16]. If the picked device is laminated against the target substrate with different separation energy of film/substrate ($G_{FS}$) and one slowly peels the PDMS stamp vertically, the forces between the stamp and the device are weak [12, 16]. Hence, they attach to the target substrate and printing occurs [12, 16].

$$G(v) = G_0 \left(1 + \left(\frac{v}{v_0}\right)^n\right) \tag{1.1}$$

The separation energy of the PDMS ($G_{PDMS}$) dependency on the peeling velocity $v$ of equation 1.1 is displayed in Figure 1.26 [12, 97]. By equating the separation energy of the PDMS to the constant separation energy of the film/substrate interface ($G_{PDMS} = G_{FS}$, or the red dashed-line on Fig. 1.26) and plugging it into equation 1.1, the critical velocity can be extracted [12, 16, 97].

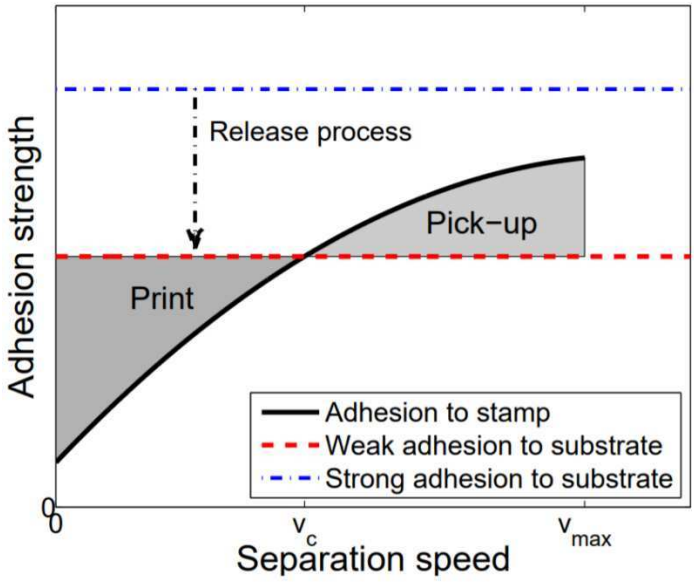



*Figure 1.26: Schematics of the separation energy dependencies on the peeling speed. When the peeling speed is lower than the critical speed printing will occur. When it is higher, pick-up will occur. Typically, for inorganic semiconductor devices, the device-substrate separation energies are a lot higher (blue dashed-line) [12, 97, 129].*

$$v_c = v_0 \left(\frac{G_{FC} - G_0}{G_0}\right)^{\frac{1}{n}} \tag{1.2}$$

This implies that in principle for each single material, a critical peeling velocity $v_c$ is present [12, 16, 97]. If it is exceeded by a PDMS peeling speed v, the film attaches to the PDMS stamp and film pick-up occurs [12, 16, 97]. Conversely, printing will occur once the peeling speed v of the PDMS stamp is lower than the critical speed of the specific material interface [12, 16, 97], as shown schematically in Fig. 1.27.

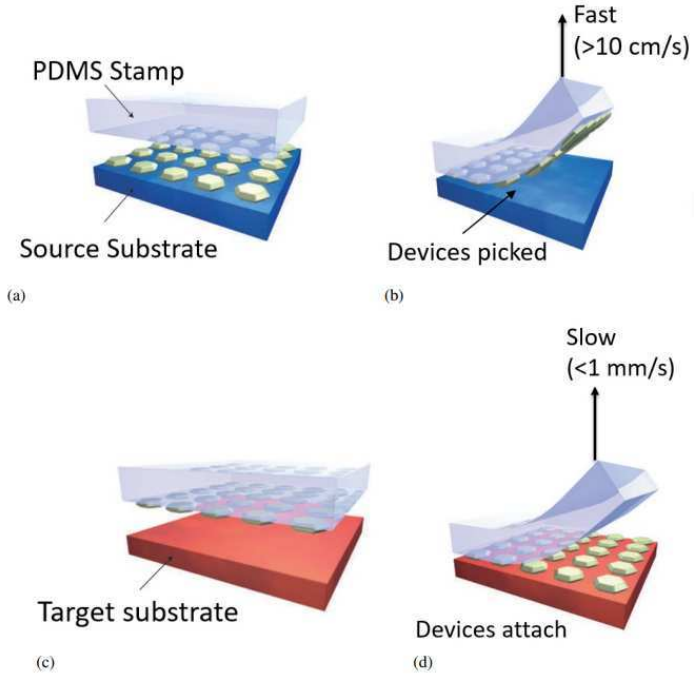



*Figure 1.27: The main concept of the transfer printing process [12, 124].*

**General Process-Flow of Micro-Transfer Printing Integration** The situation outlined in Figure 1.26 is not as simple as it seems, particularly when dealing with semiconductor materials like Si, Ge, InP, etc. Their separation energies are located significantly higher on the energy scale (represented by the blue dashed-line in Figure 1.26). As a result, the physical peeling speeds of the PDMS are insufficient to lift the device or film.

Hence, a crucial technological step of releasing the devices is required to facilitate the transfer printing of semiconductor devices that are loosely anchored to the substrate [130].

Figure 1.28 illustrates the general release process. It is vital to select the right layer stack with the release layer sandwiched between the device layer and the

substrate (Figure 1.28(a)). Subsequently, the device layer and the release layer are patterned (Figure 1.28(b)), and a layer that can anchor the device to the source substrate through tethers is formed (Figure 1.28(c)). The release layer is then underetched, turning devices into free-hanging membranes (coupons) anchored to the substrate by the tethers (Figure 1.28(d)). When the PDMS stamp touches the released coupons and quickly moves upwards, the tethers break at the weakest points, allowing it to pick up the released coupon. The success of transfer printing hinges on the development of the release process and the proper tethering of the coupons [12].

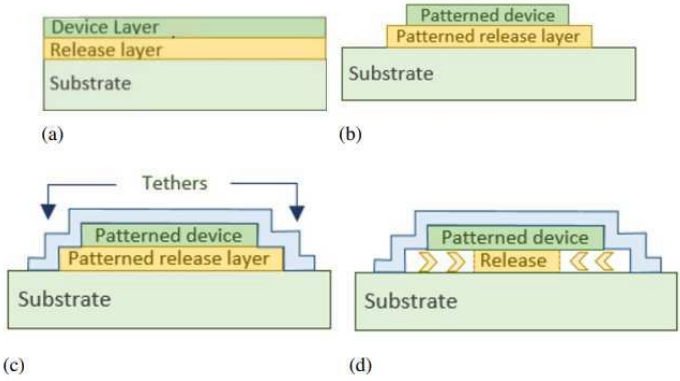



*Figure 1.28: Release process schematic [12, 131].*

**Lab-Scale Transfer-Printer: $\mu$TP-100** The uTP-100, a laboratory-scale printing system produced by X-Celeprint Ltd, was extensively utilized in this PhD research. As depicted in Fig. 1.29, the system is composed of three main components: an electrical cabinet, a user interface, and a transfer printing machine. The electrical cabinet, which houses the printer's main alternating current (AC) power supply, a CPU, a temperature controller, and the vacuum, serves as the primary processing unit.

Figure 1.30 illustrates the transfer printing machine's design. The source and target substrates are positioned side by side on the sample vacuum chucks. A cleaning pad for the PDMS stamp (double-sided scotch tape) is located at the back (not visible in the figure). The machine's upper section, the head, is equipped with a camera plus to an objective on top (with 5× and 10× magnification lenses available) and an upside-down PDMS on-glass mount secured by the vacuum chuck. The camera and the entire head can move independently in the Z-direction.

The transfer printing process is as follows: the user secures the prepared source and target substrates onto the sample chucks, then attaches the PDMS stamp to the glass plate, flips the plate, and secures it to the vacuum chuck at the bottom of the

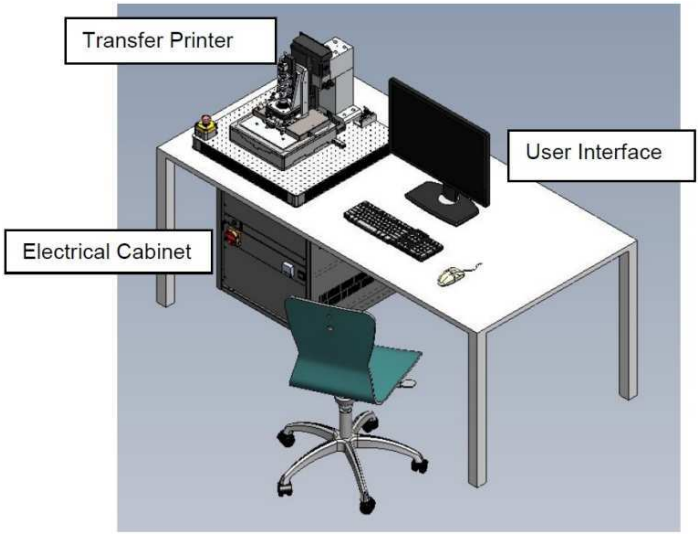



*Figure 1.29: The μTP-100 system [132].*

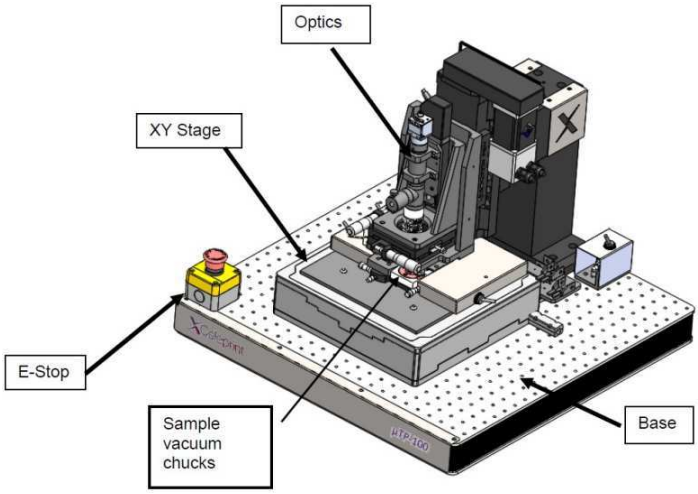



*Figure 1.30: Schematics of the lab-scale transfer printing machine [132].*

head. The user has independent control over the camera movement, focus, and head movement in the Z-direction, as well as the sample stage movement in X and Y directions. The user can manually guide the stamp to the desired positions on the source sample (up to 3-inch wafer), target sample (up to 3-inch wafer), and cleaning pad and execute picking, printing, and cleaning operations by pressing the stamp against the surface of the source, target, and cleaning pad respectively.

It is worth mentioning that an automated transfer printing mode is also available.

## 1.5 Thesis Outline and Attribution of Work

The objective of this PhD research is to demonstrate the integration of widely tunable and narrow-linewidth III–V-on-silicon lasers on IMEC 400nm+ SiPh platform using micro-transfer printing. These lasers, with their narrow linewidth and broad tunability, are promising candidates for a wide range of applications. For instance, biomedical and sensing applications demand ultra-wide tuning, while datacom applications require both tunability and narrow linewidth. Successfully demonstrating such lasers lays the foundation for extending the approach to more advanced platforms such as imec's iSiPP50G, leveraging the inherent scalability and low-cost potential of $\mu$TP for high-volume photonic integration.

With this goal in mind, the thesis is divided into three major sections, covered across five chapters as follows:

- **Demonstration of Ultra-wide Tunable Narrow-linewidth Lasers on IMEC 400nm+ Platform using $\mu$TP**: This is addressed first in Chapter 2 with an overview of the design of tunable and narrow-linewidth heterogeneous lasers, leading to a specific schematic for the laser of this work. The chapter then details the fabrication process, which relies on $\mu$TP integration of pre-fabricated III-V SOAs on IMEC 400nm+ platform. This is followed by the electrical and optical characterization and linewidth measurement of the laser. And the chapter concludes with a series of application-driven demonstrations, where the same laser architecture, or modified variants of it, is adapted to address specific use cases such as biomedical sensing, spectroscopy, gas detection, coherence-critical system, and programmable photonic signal processing. This highlights the versatility and scalability of the demonstrated laser as a foundational building block for diverse photonic systems.

- **Demonstration of $\mu$TP-integrated Optical Amplifiers as Power Boosters for the Lasers**: To extend the applicability of the integrated laser, higher optical output power across the tuning range may be required. Chapter 3 addresses this by proposing, fabricating, and characterizing a specially tapered-designed high-saturation-power SOA, tailored for compatibility with the $\mu$TP process and implemented as a power booster. The chapter concludes with a comparison to state-of-the-art solutions, and discusses potential future improvements as well as alternative approaches.

- **Taking Initial Steps Toward Wafer-Scale $\mu$TP Integration**: Chapter 4 addresses the growing need to scale $\mu$TP technology toward wafer-level integration. It begins by outlining the motivations behind this transition and

introduces the foundational tools and methodologies required to establish a $\mu$TP pilot line, as pursued in the TRANSVERSE initiative. The chapter further discusses the development of an $\mu$TP-based active components PDK, such as lasers and SOAs, that can be integrated atop imec's existing SiPh platforms. It concludes with an outlook on future directions, highlighting the envisioned roadmap for the TRANSVERSE pilot line and its potential to industrialize $\mu$TP-enabled heterogeneous photonics.

The final Chapter 5 provides key takeaways and conclusion along with a perspective on future research directions.

The research was supported by two European Union's Horizon 2020 (H2020) research and innovation program projects, **Wideband Optical Network (WON)** under the **Marie Skłodowska-Curie** grant agreement **814276** [133], and **Photonic Medical Devices (MedPhab)** under grant agreement **871345** [134–136], and was carried out in the **Photonics Research Group (PRG) at Ghent University - imec**.

## 1.6 Publications and Awards

This doctoral dissertation has led to multiple publications in peer-reviewed international journals and conferences. A brief outline of the research contributions is presented below:

### 1.6.1 Publications in international peer reviewed journal papers

1. G. Roelkens, J. Zhang, L. Bogaert, **E. Soltanian**, M. Billet, A. Uzun, B. Pan, Y. Liu, E. Delli, D. Wang, V. Bonito Oliva, L.Thi Ngoc Tran, X. Guo, H. Li, S. Qin, K. Akritidis, Y. Chen, Y. Xue, M. Niels, D. Maes, M. Kiewiet, T. Reep, T. Vanackere, T. Vandekerckhove, I. Luntadila Lufungula, J. De Witte, L. Reis, S. Poelman, Y. Tan, H. Deng, W. Bogaerts, G. Morthier, D. Van Thourhout, B. Kuyken, "Present and future of micro-transfer printing for heterogeneous photonic integrated circuits," Applied Physics Letters - Photonics (invited), 9(1), (2024). doi:10.1063/5.0181099

2. J. Zhang, L. Bogaert, C.J. Krückel, **E. Soltanian**, H. Deng, B. Haq, J.Rimbock, J. Van Kerrebrouck, G. Lepage, P. Verheyen, J. Van Campenhout, P. Ossieur, D. Van Thourhout, G. Morthier, W. Bogaerts, G. Roelkens, "Micro-transfer printing InP C-band SOAs on advanced silicon photonics platform for lossless MZI switch fabrics and high-speed integrated transmitters," Optics Express, 31(26), p.42807-42821 (2023). doi:10.1364/OE.505112

3. **E. Soltanian**, G. Muliuk, S. Uvin, D. Wang, G. Lepage, P. Verheyen, J. Van Campenhout, S. Ertl, J. Rimbock, N. Vaissiere, D. Neel, J. Ramirez,

J. Decobert, B. Kuyken, J. Zhang, G. Roelkens, "Micro-Transfer-Printed Narrow-Linewidth III-V-on-Si Double Laser Structure with Combined 110 nm Tuning Range," Optics Express, 30(22), p.39329-39339 (2022). doi:10.1364/OE.470497

4. G. Roelkens, J. Zhang, L. Bogaert, M. Billet, D. Wang, B. Pan, C.J. Krückel, **E. Soltanian**, D. Maes, T. Vanackere, T. Vandekerckhove, S. Cuyvers, J. De Witte, I. Luntadila Lufungula, X. Guo, H. Li, S. Qin, G. Muliuk, S. Uvin, B. Haq, C. Op de Beeck, J. Goyvaerts, G. Lepage, P. Verheyen, J. Van Campenhout, G. Morthier, B. Kuyken, D. Van Thourhout, R. Baets, "Micro-transfer printing for heterogeneous Si photonic integrated circuits," IEEE Journal on Selected Topics in Quantum Electronics (invited), 29(3), p.8200414 (2022). doi:10.1109/JSTQE.2022.3222686

5. B. Pan, J. Bourderionnet, V. Billault, G. Dande, M. Dahlem, J.H. Song, S. Dwivedi, D. Carbajal Altamirano, C. Cummins, S.S. Saseendran, P. Helin, J. Ramirez, D. Néel, **E. Soltanian**, J. Zhang, G. Roelkens, "III-V-on-$Si_3N_4$ widely tunable narrow-linewidth laser based on micro-transfer printing," Photonics Research, 12(11), pp.2508–2520 (2024). doi:10.1364/PRJ.530925

6. G. Dandé, J. Pennanech, C. Charliac, V. Kemlin, V. Crozatier, I. Ghorbel, V. Billault, B. Pan, **E. Soltanian**, J. Zhang, G. Roelkens, M. Dahlem, J. Song, S. Dwivedi, D. Carbajal Altamirano, C. Cummins, S.S. Saseendran, P. Helin, J. Ramirez, D. Néel, H. Guillet De Chatellus, J. Bourderionnet, "Narrow linewidth III-V-on-SiN laser with extended frequency chirp capability based on micro-transfer printing for high resolution distributed acoustic sensing," Optics Express, 33(8), pp.17192–17202 (2025). doi:10.1364/OE.529238

7. X. Guo, **E. Soltanian**, J. Zhang, S. Qin, N. Vaissière, D. Néel, J. Ramirez, J. Decobert, S. Uvin, G. Roelkens, "Micro-transfer-printed short-wave infrared InP-on-silicon tunable laser," Optics Letters, 50(5), pp.1589–1592 (2025). doi:10.1364/OL.549540

8. Y. Liu, J. Zhang, L. Bogaert, **E. Soltanian**, E. Delli, K. Morozov, S. Mikhrin, J. Rimböck, G. Lepage, P. Verheyen, J. Van Campenhout, P. Ossieur, G. Morthier, G. Roelkens, "Micro-transfer printing of O-band InAs/GaAs quantum-dot SOAs on silicon photonic integrated circuits," Photonics Research, 13(5), pp.1341–1352 (2025). doi:10.1364/PRJ.545946

9. Y. Liu, Y. Chen, L. Bogaert, **E. Soltanian**, E. Delli, G. Lepage, P. Verheyen, J. Van Campenhout, G. Morthier, G. Roelkens, J. Zhang, "Widely tunable narrow-linewidth lasers with booster amplification on silicon photonics," Optics Express, 33(10), pp.22078–22086 (2025). doi:10.1364/OE.561111

10. Y. Xue, B. Pan, Y. Liu, **E. Soltanian**, J. Zhang, G. Morthier, G. Roelkens, "Enhanced feedback sensitivity suppression in phase-detuned tunable lasers with high-Q Vernier-effect based ring resonators," Optics Express, 33(16), pp.33342–33350 (2025). doi:10.1364/OE.561509

11. H. Deng, J. Zhang, **E. Soltanian**, X. Chen, C. Pang, N. Vaissiere, D. Neel, J. Ramirez, J. Decobert, N. Singh, G. Torfs, G. Roelkens, W. Bogaerts, "Single-Chip Silicon Photonic Engine for Analog Optical and Microwave Signals Processing," Nature Communications, 16(1), p.5087 (2025). doi:10.1038/s41467-025-60100-0

### 1.6.2 Publications in international conference proceedings

1. W. Bogaerts, H. Deng, X. Chen, L. Van Iseghem, I. Zand, Y. Zhang, Y. Liu, A. Al Haffar, P. Edinger, G. Jo, A.Y. Takabayashi, C. Antony, A. Mallik Kumar, J. Zhang, **E. Soltanian**, P. Verheyen, J. Beeckman, G. Roelkens, N. Quack, F. Niklaus, K.B. Gylfason, U. Khan, "Building general-purpose programmable photonic chips: opportunities and challenges," SPIE Photonics West - OPTO (invited), 12890, United States, p.12890-55 (2024). doi:10.1117/12.3009922

2. J. Zhang, L. Bogaert, M. Billet, D. Wang, B. Pan, S. Qin, **E. Soltanian**, S. Cuyvers, D. Maes, T. Vanackere, T. Vandekerckhove, S. Poelman, M. Kiewiet, I. Luntadila Lufungula, X. Guo, H. Li, J. De Witte, G. Lepage, P. Verheyen, J. Van Campenhout, B. Kuyken, G. Morthier, D. Van Thourhout, R. Baets, G. Roelkens, "Photonic integrated circuits realized using micro-transfer printing," PIERS (invited), pp.1-1 (2023). http://hdl.handle.net/1854/LU-01HRVKSBD28J2YBH3MJ1RFGFJ8

3. Y. Zhang, H. Deng, **E. Soltanian**, J. Zhang, G. Roelkens, W. Bogaerts, "A Nonlinear Activation Function for Optical Neural Networks Using a Mach-Zehnder Interferometer with a III-V-on-Si Amplifier," 2023 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC), Germany, pp.1-1 (2023). doi:10.1109/CLEO/Europe-EQEC57999.2023.10231574

4. **E. Soltanian**, M. Billet, A. Hermans, B. Kuyken, J. Zhang, G. Roelkens, "Micro-Transfer-Printed III-V-on-Si Semiconductor Optical Amplifier with 15 dBm Output Saturation Power," 2023 IEEE Silicon Photonics Conference (SiPhotonics, Formerly GFP Conference), United States, pp. 1-2 (2023). doi:10.1109/SiPhotonics55903.2023.10141916

5. H. Deng, **E. Soltanian**, J. Zhang, G. Roelkens, W. Bogaerts, "Wavelength Converter using Micro Transfer-Printed Optical Amplifiers on a Full SiPh

Platform," 2023 IEEE Silicon Photonics Conference (SiPhotonics, Formerly GFP Conference), United States, pp. 1-2 (2023). doi:10.1109/SiPhotonics55903.2023.10141958

6. B. Pan, Jerome Bourderionnet, Vincent Billault, Arnaud Brignon, S. Dwivedi, Marcus Dahlem, Cian Cummins, Sandeep S. Saseendran, Nga Pham, Philippe Helin, Nicolas Vaissiere, Delphine Neel, Joan Ramirez, Jean Decobert, Johanna Rimbock, Ruggero Loi, Alin Fecioru, **E. Soltanian**, J. Zhang, B. Kuyken, G. Roelkens, "III-V-on-silicon nitride narrow-linewidth tunable laser based on micro-transfer printing," Optical Fiber Communication Conference (OFC) 2023, Technical Digest Series (Optica Publishing Group, 2023), paper Th3B.5 (2023). doi:10.1364/OFC.2023.Th3B.5

7. **E. Soltanian**, M. Billet, A. Hermans, B. Kuyken, J. Zhang, G. Roelkens, "Micro-Transfer-Printed III-V-on-Si Semiconductor Optical Amplifiers with High Saturation Power," IEEE Benelux Photonics Chapter - Annual Symposim 2022, 26, Netherlands, p.201-204 (2022). https://www.aanmelder.nl/ieee-ps-benelux-2022/wiki/734993/new-proceedings

8. **E. Soltanian**, G. Muliuk, S. Uvin, D. Wang, G. Lepage, P. Verheyen, J. Van Campenhout, S. Ertl, J. Rimbock, N. Vaissiere, D. Neel, J. Ramirez, J. Decobert, B. Kuyken, J. Zhang, G. Roelkens, "Narrow-Linewidth Micro-Transfer-Printed III-V-on-Si Laser with 110 nm Tuning Range," 2022 IEEE Photonics Society Summer Topicals Meeting Series (SUM), Cabo San Lucas, Mexico, 2022, pp. 1-2 (2022). doi:10.1109/SUM53465.2022.9858218

9. **E. Soltanian**, G. Muliuk, S. Uvin, D. Wang, G. Lepage, P. Verheyen, J. Van Campenhout, S. Ertl, J. Rimbock, N. Vaissiere, D. Neel, J. Ramirez, J. Zhang, G. Roelkens, "Micro-Transfer-Printed III-V-on-Si Laser with 120 nm tuning range," 2022 European Conference on Integrated Optics (ECIO2022), Italy, p.282-284 (2022). http://hdl.handle.net/1854/LU-8765148

10. J. Zhang, **E. Soltanian**, B. Haq, S. Ertl, J. Rimboeck, B. Matuskova, E. Pelucchi, A. Gocalinska, J. Van Campenhout, G. Lepage, P. Verheyen, W. Bogaerts, G. Roelkens, "Integrated optical transmitter with micro-transfer-printed widely tunable III-V-on-Si laser," Optical Fiber Communication Conference (OFC) 2022, Technical Digest Series (Optica Publishing Group, 2022), paper Tu2D.2 (2022). doi:10.1364/OFC.2022.Tu2D.2

11. S. Qin, **E. Soltanian**, J. Ramirez, D. Neel, N. Vaissiere, J. Decobert, J. Zhang, G. Roelkens, "Microtransfer printing of InP SOAs on advanced silicon photonics platform for C-band preamplified receivers," SPIE Photonics West, 13371 (2025). doi:10.1117/12.3041159

12. X. Guo, **E. Soltanian**, J. Zhang, N. Vaissière, D. Néel, J. Ramirez, J. Decobert, S. Uvin, G. Roelkens, "SWIR InP-on-silicon tunable laser based on micro-transfer printing," SPIE Photonics West, 13370 (2025). doi:10.1117/12.3039975

13. W. Bogaerts, H. Deng, Y. Zhang, X. Chen, L. Van Iseghem, K.P. Nagarjun, I. Zand, A. Barzanji, A. Ribeiro, F. Vanden Kerchove, U. Khan, **E. Soltanian**, P. Edinger, A. Djuphammer, G. Jo, A.K. Mallik, J.S. Lee, C. Antony, D. Kelly, J.H.P. Morrissey, P. O'Brien, D. Colle, M. Pickavet, F. Niklaus, K. Gylfason, G. Torfs, J. Beeckman, G. Roelkens, "Programmable photonic circuits for signal processing," SPIE Photonics West, 13369 (2025). doi:10.1117/12.3039727

14. H. Deng, J. Zhang, **E. Soltanian**, X. Chen, C. Pang, N. Vaissiere, D. Neel, J. Ramirez, J. Decobert, N. Singh, G. Torfs, G. Roelkens, W. Bogaerts, "Fully integrated single-chip silicon photonic processor for analog optical and microwave signals," SPIE Photonics West, 13372 (2025). doi:10.1117/12.3044760

15. Y. Liu, Y. Chen, L. Bogaert, **E. Soltanian**, E. Delli, G. Lepage, P. Verheyen, J. Van Campenhout, G. Roelkens, J. Zhang, "Widely Tunable InP-on-silicon Lasers based on the Micro-Transfer Printing of Double-Ridge Coupons," Optical Fiber Communication Conference (OFC) 2025, Optica Publishing Group, p. W1G.5 (2025). doi:10.1364/OFC.2025.W1G.5

16. Y. Chen, S. Qin, **E. Soltanian**, L. Bogaert, J. Zhang, G. Roelkens, "400Heterogenous Silicon Photonics Switch Fabric Integrated with SOAs and PDs enabled by Micro-Transfer Printing," IEEE Photonics Benelux Annual Symposium 2024, Twente, Netherlands (November 2024).

### 1.6.3 Awards

**Bronze Award**
Huawei Silicon Photonics PhD Student Contest 2022
Huawei Technologies Research and Development Belgium NV
5 December 2022, Ghent, Belgium
For the demonstration of: Narrow-Linewidth Micro-Transfer-Printed III-V-on-Si Laser with 110 nm Tuning Range.

# References

[1] R. S. Kerdock and D. H. Wolaver. *Atlanta fiber system experiment: results of the atlanta experiment*. The Bell System Technical Journal, 57(6):1857–1879, 1978.

[2] B. J. Puttnam, R. S. Luís, W. Klaus, J. Sakaguchi, J.-M. Delgado Mendinueta, Y. Awaji, N. Wada, Yoshiaki Tamura, Tetsuya Hayashi, Masaaki Hirano, and J. Marciante. *2.15 Pb/s transmission using a 22 core homogeneous single-mode multi-core fiber and wideband optical comb*. In 2015 European Conference on Optical Communication (ECOC), pages 1–3, 2015.

[3] Web Foundation. *History of the Web*, 2009.

[4] Cisco. *Global Consumer Highlights*, 2018.

[5] Cisco. *Annual Internet Report*, 2020.

[6] Daily Mail. *Could enemies sabotage undersea cables linking the world?*, 2018.

[7] TeleGeography. *Submarine Cable Map*, 2024.

[8] Submarine Cable Map. *How the Internet Spans the Globe*, 2024.

[9] A. Abbasi, B. Moeneclaey, J. Verbist, X. Yin, J. Bauwelinck, G. Roelkens, and G. Morthier. *56 Gb/s direct modulation of an InP-on-Si DFB laser diode*. In 2017 IEEE Optical Interconnects Conference (OI), pages 31–32, 2017.

[10] M. Shahin, K. Ma, A. Abbasi, G. Roelkens, and G. Morthier. *45 Gb/s Direct Modulation of Two-Section InP-on-Si DFB Laser Diodes*. IEEE Photonics Technology Letters, 30(8):685–687, 2018.

[11] Ning Hua Zhu, Zhan Shi, Zhi Ke Zhang, Yi Ming Zhang, Can Wen Zou, Ze Ping Zhao, Yu Liu, Wei Li, and Ming Li. *Directly Modulated Semiconductor Lasers*. IEEE Journal of Selected Topics in Quantum Electronics, 24(1):1–19, 2018.

[12] Muliuk, Grigorij. *Micro-transfer-printing of III-V semiconductor and silicon-germanium photodetectors on silicon photonic integrated circuits*. PhD thesis, Ghent University, 2020.

[13] Antonin Gallet. *Hybrid III-V on silicon lasers for optical communications*. Theses, Université Paris Saclay (COmUE), Apr 2019.

[14] Fiberstore. *Single Mode Cabling Cost vs Multimode Cabling Cost*, 2022.

[15] Camplex. *Single Mode and Multimode Fiber Cable*.

[16] Zhang, Jing. *III-V-on-Si transceivers based on micro-transfer-printing*. PhD thesis, Ghent University, 2021.

[17] Jeffrey R. Minch, Seoung-Hwan Park, T. Keating, and Shun Lien Chuang. *Theory and Experiment of In Ga As P and In Ga Al As Long-Wavelength Strained Quantum-Well Lasers*. 1999.

[18] R. Fehse, I. Marko, and A.R. Adams. *Long wavelength lasers on GaAs substrates*. IEE Proceedings - Circuits, Devices and Systems, 150:521–528(7), December 2003.

[19] Rahimi Vaskasi, Javad. *InP-on-Si DFB laser diodes with high wall-plug efficiency, large modulation bandwidth and low noise*. PhD thesis, Ghent University, 2022.

[20] J. Durel, B. Ben Bakir, C. Jany, S. Cremer, K. Hassan, B. Szelag, T. Bria, V. Larrey, L. Sanchez, P. Brianceau, J.-A Dallery, R. Guiavarch, T. Card, R. Thibon, J.-E. Broquin, and F. Bœuf. *Back-side integration of Hybrid III–V on Silicon DBR lasers*. In 2017 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), pages 1–2, 2017.

[21] Duanni Huang, Minh A. Tran, Joel Guo, Jon Peters, Tin Komljenovic, Aditya Malik, Paul A. Morton, and John E. Bowers. *Sub-kHz Linewidth Extended-DBR Lasers Heterogeneously Integrated on Silicon*. In 2019 Optical Fiber Communications Conference and Exhibition (OFC), pages 1–3, 2019.

[22] Hang Guan, Ari Novack, Tal Galfsky, Yangjin Ma, Saeed Fathololoumi, Alexandre Horth, Tam N. Huynh, Jose Roman, Ruizhi Shi, Michael Caverley, Yang Liu, Thomas Baehr-Jones, Keren Bergman, and Michael Hochberg. *Widely-tunable, narrow-linewidth III-V/silicon hybrid external-cavity laser for coherent communication*. Opt. Express, 26(7):7920–7933, Apr 2018.

[23] Aditya Malik, Joel Guo, Minh A. Tran, Geza Kurczveil, Di Liang, and John E. Bowers. *Widely tunable, heterogeneously integrated quantum-dot O-band lasers on silicon*. Photon. Res., 8(10):1551–1557, Oct 2020.

[24] J. A. Tatum, G. D. Landry, D. Gazula, J. K. Wade, and P. Westbergh. *VCSEL-Based Optical Transceivers for Future Data Center Applications*. In 2018 Optical Fiber Communications Conference and Exposition (OFC), pages 1–3, 2018.

[25] Giannis Kanakis, Nikos Iliadis, Wouter Soenen, Bart Moeneclaey, Nikolaos Argyris, Dimitrios Kalavrouziotis, Silvia Spiga, Paraskevas Bakopoulos, and Hercules Avramopoulos. *High-Speed VCSEL-Based Transceiver for 200 GbE Short-Reach Intra-Datacenter Optical Interconnects*. Applied Sciences, 9(12), 2019.

[26] FOWiki. *Understand Fiber Attenuation*, 2015.

[27] Jaernin Shin, Chung-Seok Seo, A. Chellappa, M. Brooke, A. Chattejce, and N.M. Jokerst. *Comparison of electrical and optical interconnect*. In 53rd Electronic Components and Technology Conference, 2003. Proceedings., pages 1067–1072, 2003.

[28] Guoqing Chen, Hui Chen, M. Haurylau, N.A. Nelson, D.H. Albonesi, P.M. Fauchet, and E.G. Friedman. *On-Chip Copper-Based vs. Optical Interconnects: Delay Uncertainty, Latency, Power, and Bandwidth Density Comparative Predictions*. In 2006 International Interconnect Technology Conference, pages 39–41, 2006.

[29] Hoyeol Cho, Pawan Kapur, and Krishna C. Saraswat. *Power Comparison Between High-Speed Electrical and Optical Interconnects for Interchip Communication*. J. Lightwave Technol., 22(9):2021, Sep 2004.

[30] STL. *6 Key Benefits of Optical Interconnect Technology*, 2023.

[31] Amin Abbasi, Jochem Verbist, Joris Van Kerrebrouck, Francois Lelarge, Guang-Hua Duan, Xin Yin, Johan Bauwelinck, Gunther Roelkens, and Geert Morthier. *28 Gb/s direct modulation heterogeneously integrated C-band InP/SOI DFB laser*. Opt. Express, 23(20):26479–26485, Oct 2015.

[32] Taiwan Semiconductor Manufacturing Company Limited. *3nm Technology*. `https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm`, 2024. Accessed: 2025-10-04.

[33] Wikipedia contributors. *3 nm process — Wikipedia, The Free Encyclopedia*. `https://en.wikipedia.org/wiki/3_nm_process`, 2024. [Online; accessed 2025-10-04].

[34] Joseph Byrne. *N3E Will Be TSMC's Main 3nm Node*. `https://www.techinsights.com/blog/n3e-will-be-tsmcs-main-3nm-node`, 2024. Accessed: 2025-10-04.

[35] IMEC. *20 Year Roadmap: Tearing Down the Walls*, 2022.

[36] Z. Alferov. *Double heterostructure lasers: early days and future perspectives*. IEEE Journal of Selected Topics in Quantum Electronics, 6(6):832–840, 2000.

[37] I. Hayashi, M. B. Panish, P. W. Foy, and S. Sumski. *JUNCTION LASERS WHICH OPERATE CONTINUOUSLY AT ROOM TEMPERATURE*. Applied Physics Letters, 17(3):109–111, 08 1970.

[38] Stewart E. Miller. *Integrated optics: An introduction*. The Bell System Technical Journal, 48(7):2059–2069, 1969.

[39] Xiaomin Zhang, Mark Harrison, Audrey Harker, and Andrea M. Armani. *Serpentine low loss trapezoidal silica waveguides on silicon*. Opt. Express, 20(20):22298–22307, Sep 2012.

[40] Lech Wosinski. *Technology for Photonic Components in Silica/Silicon Material Structure*. Phd thesis, Royal Institute of Technology (KTH), Stockholm, Sweden, 2013. KTH Royal Institute of Technology.

[41] Ari Novack, Matt Streshinsky, Ran Ding, Yang Liu, Andy Eu-Jin Lim, Guo-Qiang Lo, Tom Baehr-Jones, and Michael Hochberg. *Progress in silicon platforms for integrated optics*. Nanophotonics, 3(4-5):205–214, 2014.

[42] Philippe P. Absil, Peter Verheyen, Peter De Heyn, Marianna Pantouvaki, Guy Lepage, Jeroen De Coster, and Joris Van Campenhout. *Silicon photonics integrated circuits: a manufacturing platform for high density, low power optical I/O's*. Opt. Express, 23(7):9369–9378, Apr 2015.

[43] Zengkai Shao, Yujie Chen, Hui Chen, Yanfeng Zhang, Fangxing Zhang, Jian Jian, Zeming Fan, Lin Liu, Chunchuan Yang, Lidan Zhou, and Siyuan Yu. *Ultra-low temperature silicon nitride photonic integration platform*. Opt. Express, 24(3):1865–1872, Feb 2016.

[44] Jared F. Bauters, Martijn J. R. Heck, Demis John, Daoxin Dai, Ming-Chun Tien, Jonathon S. Barton, Arne Leinse, René G. Heideman, Daniel J. Blumenthal, and John E. Bowers. *Ultra-low-loss high-aspect-ratio Si3N4 waveguides*. Opt. Express, 19(4):3163–3174, Feb 2011.

[45] Roel Baets, Ananth Z. Subramanian, Stéphane Clemmen, Bart Kuyken, Peter Bienstman, Nicolas Le Thomas, Günther Roelkens, Dries Van Thourhout, Philippe Helin, and Simone Severi. *Silicon photonics: Silicon nitride versus silicon-on-insulator*. In 2016 Optical Fiber Communications Conference and Exhibition (OFC), pages 1–3, 2016.

[46] Quentin Wilmart, Houssein El Dirani, Nicola Tyler, Daivid Fowler, Stéphane Malhouitre, Stéphanie Garcia, Marco Casale, Sébastien Kerdiles, Karim Hassan, Christelle Monat, Xavier Letartre, Ayman Kamel, Minhao Pu, Kresten Yvind, Leif Katsuo Oxenløwe, Wilfried Rabaud, Corrado Sciancalepore, Bertrand Szelag, and Ségolène Olivier. *A Versatile Silicon-Silicon Nitride Photonics Platform for Enhanced Functionalities and Applications*. Applied Sciences, 9(2), 2019.

[47] Thomas F. Kuech. *III-V compound semiconductors: Growth and structures*. Progress in Crystal Growth and Characterization of Materials, 62(2):352–370, 2016. Special Issue: Recent Progress on Fundamentals and Applications of Crystal Growth; Proceedings of the 16th International Summer School on Crystal Growth (ISSCG-16).

[48] Meint Smit, Xaveer Leijtens, Huub Ambrosius, Erwin Bente, Jos van der Tol, Barry Smalbrugge, Tjibbe de Vries, Erik-Jan Geluk, Jeroen Bolk, Rene van Veldhoven, Luc Augustin, Peter Thijs, Domenico D'Agostino, Hadi Rabbani, Katarzyna Lawniczuk, Stanislaw Stopinski, Saeed Tahvili, Antonio Corradi, Emil Kleijn, Dzmitry Dzibrou, Manuela Felicetti, Elton Bitincka, Valentina Moskalenko, Jing Zhao, Rui Santos, Giovanni Gilardi, Weiming Yao, Kevin Williams, Patty Stabile, Piet Kuindersma, Josselin Pello, Srivathsa Bhat, Yuqing Jiao, Dominik Heiss, Gunther Roelkens, Mike Wale, Paul Firth, Francisco Soares, Norbert Grote, Martin Schell, Helene Debregeas, Mohand Achouche, Jean-Louis Gentner, Arjen Bakker, Twan Korthorst, Dominic Gallagher, Andrew Dabbs, Andrea Melloni, Francesco Morichetti, Daniele Melati, Adrian Wonfor, Richard Penty, Ronald Broeke, Bob Musk, and Dave Robbins. *An introduction to InP-based generic integration technology*. Semiconductor Science and Technology, 29(8):083001, jun 2014.

[49] Yifan Qi and Yang Li. *Integrated lithium niobate photonics*. Nanophotonics, 9(6):1287–1320, 2020.

[50] Marco Bazzan and Cinzia Sada. *Optical waveguides in lithium niobate: Recent developments and applications*. Applied Physics Reviews, 2(4):040603, 10 2015.

[51] Aleksandrs Marinins. *Polymer Components for Photonic Integrated Circuits*. PhD thesis, Royal Institute of Technology, 2017.

[52] N. Grote, N. Keil, C. Zawadzki, W. Brinker, D. de Felipe, and Z. Zhang. *Polymer photonic integration platform: Technology and components*. In 2012 17th Opto-Electronics and Communications Conference, pages 285–286, 2012.

[53] Ziyang Zhang, David Felipe, Vasilis Katopodis, Panos Groumas, Christos Kouloumentas, Hercules Avramopoulos, Jean-Yves Dupuy, Agnieszka Konczykowska, Alberto Dede, Antonio Beretta, Antonello Vannucci, Giulio Cangini, Raluca Dinu, Detlef Schmidt, Martin Moehrle, Patrick Runge, Jung-Han Choi, Heinz-Gunter Bach, Norbert Grote, Norbert Keil, and Martin Schell. *Hybrid Photonic Integration on a Polymer Platform*. Photonics, 2(3):1005–1026, 2015.

[54] Kirk-Othmer. *Encyclopedia of Chemical Technology*. John Wiley & Sons, 1985.

[55] P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. Van Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. Van Thourhout, and R. Baets. *Low-loss SOI photonic wires and ring resonators fabricated with deep UV lithography*. IEEE Photonics Technology Letters, 16(5):1328–1330, 2004.

[56] Yurii A. Vlasov and Sharee J. McNab. *Losses in single-mode silicon-on-insulator strip waveguides and bends*. Opt. Express, 12(8):1622–1631, Apr 2004.

[57] Marko Galarza, J MORENO, M LOPEZ-AMO, Ilse Christiaens, Dries Van Thourhout, and Roel Baets. *Simple low-loss waveguide bends using ARROW effect.* 2005.

[58] Wim Bogaerts, Shankar Kumar Selvaraja, Pieter Dumon, Joost Brouckaert, Katrien De Vos, Dries Van Thourhout, and Roel Baets. *Silicon-on-Insulator Spectral Filters Fabricated With CMOS Technology*. IEEE Journal of Selected Topics in Quantum Electronics, 16(1):33–44, 2010.

[59] Xu Wang, Wei Shi, Han Yun, Samantha Grist, Nicolas A. F. Jaeger, and Lukas Chrostowski. *Narrow-band waveguide Bragg gratings on SOI wafers with CMOS-compatible fabrication process*. Opt. Express, 20(14):15547–15558, Jul 2012.

[60] Jan Niehusmann, Andreas Vörckel, Peter Haring Bolivar, Thorsten Wahlbrink, Wolfgang Henschel, and Heinrich Kurz. *Ultrahigh-quality-factor silicon-on-insulator microring resonator*. Opt. Lett., 29(24):2861–2863, Dec 2004.

[61] Tatsuhiko Fukazawa, Fumiaki Ohno, and Toshihiko Baba. *Very Compact Arrayed-Waveguide-Grating Demultiplexer Using Si Photonic Wire Waveguides*. Japanese Journal of Applied Physics, 43(5B):L673, apr 2004.

[62] P.-J. Rigole, S. Nilsson, L. Backbom, T. Klinga, J. Wallin, B. Stalnacke, E. Berglind, and B. Stoltz. *Access to 20 evenly distributed wavelengths over 100 nm using only a single current tuning in a four-electrode monolithic semiconductor laser*. IEEE Photonics Technology Letters, 7(11):1249–1251, 1995.

[63] Ansheng Liu, Ling Liao, Doron Rubin, Hat Nguyen, Berkehan Ciftcioglu, Yoel Chetrit, Nahum Izhaky, and Mario Paniccia. *High-speed optical modulation based on carrier depletion in a silicon waveguide*. Opt. Express, 15(2):660–668, Jan 2007.

[64] Long Chen and Michal Lipson. *Ultra-low capacitance and high speed germanium photodetectors on silicon*. Opt. Express, 17(10):7901–7906, May 2009.

[65] Yole Group. *Silicon photonics: to SOI and beyond!*, 2022.

[66] Intel. *Silicon Photonics Overview Flyer*, 2022.

[67] Intel. *Silicon Photonics Pluggable Optical Transceivers*.

[68] Yole Group. *Silicon Photonics and Photonic Integrated Circuits 2019*, 2019.

[69] Yole Group. *Intel, Cisco, NVIDIA, GlobalFoundries and TSMC... The silicon photonics waltz*, 2023.

[70] Di Liang and John E. Bowers. *Recent progress in lasers on silicon*. Nature Photonics, 4(8):511–517, 8 2010.

[71] Europractice. *MPW Fabrication*.

[72] Imec. *Silicon Photonics Platform Services*, 2023.

[73] IMEC. *Silicon Photonic IC Prototyping*, 2024.

[74] IMEC. *Prototyping and low-volume manufacturing of silicon photonic ICs, iSiPP50G platform*, 2024.

[75] Europractice. *Photonics: Silicon, Silicon-Nitride and Glass Photonics*, 2024.

[76] Europractice IC. *Imec Silicon Photonics and Silicon Nitride Photonics*, 2024.

[77] Europractice: Who we are. *Who We Are*.

[78] Haq, Bahawal. *III-V-on-Si SOAs and DFB/DBR lasers realised using micro-transfer printing*. PhD thesis, Ghent University, 2021.

[79] S. Keyvaninia, S. Verstuyft, L. Van Landschoot, F. Lelarge, G.-H. Duan, S. Messaoudene, J. M. Fedeli, T. De Vries, B. Smalbrugge, E. J. Geluk, J. Bolk, M. Smit, G. Morthier, D. Van Thourhout, and G. Roelkens. *Heterogeneously integrated III-V/silicon distributed feedback lasers*. Opt. Lett., 38(24):5434–5437, Dec 2013.

[80] N. Lindenmann, G. Balthasar, D. Hillerkuss, R. Schmogrow, M. Jordan, J. Leuthold, W. Freude, and C. Koos. *Photonic wire bonding: a novel concept for chip-scale interconnects*. Opt. Express, 20(16):17667–17677, Jul 2012.

[81] P.-I. Dietrich, M. Blaicher, I. Reuter, M. Billah, T. Hoose, A. Hofmann, C. Caer, R. Dangel, B. Offrein, U. Troppenz, M. Moehrle, W. Freude, and C. Koos. *In situ 3D nanoprinting of free-form coupling elements for hybrid photonic integration*. Nature Photonics, 12(4):241–247, 2018.

[82] Nicole Lindenmann, Stephan Dottermusch, Maria Laura Goedecke, Tobias Hoose, Muhammad Rodlin Billah, Temitope Paul Onanuga, Andreas Hofmann, Wolfgang Freude, and Christian Koos. *Connecting Silicon Photonic Circuits to Multicore Fibers by Photonic Wire Bonding*. Journal of Lightwave Technology, 33(4):755–760, 2015.

[83] Markus Deubel, Georg von Freymann, Martin Wegener, Suresh Pereira, Kurt Busch, and Costas M. Soukoulis. *Direct laser writing of three-dimensional photonic-crystal templates for telecommunications*. Nature Materials, 3(7):444–447, 2004.

[84] Muhammad Rodlin Billah, Matthias Blaicher, Tobias Hoose, Philipp-Immanuel Dietrich, Pablo Marin-Palomo, Nicole Lindenmann, Aleksandar Nesic, Andreas Hofmann, Ute Troppenz, Martin Moehrle, Sebastian Randel, Wolfgang Freude, and Christian Koos. *Hybrid integration of silicon photonics circuits and InP lasers by photonic wire bonding*. Optica, 5(7):876–883, Jul 2018.

[85] Riccardo Marchetti, Cosimo Lacava, Lee Carroll, Kamil Gradkowski, and Paolo Minzioni. *Coupling strategies for silicon photonics integrated chips (Invited)*. Photon. Res., 7(2):201–239, Feb 2019.

[86] Jörn P. Epping, Ruud M. Oldenbeuving, Dimitri Geskus, Ilka Visscher, Robert Grootjans, Chris G.H. Roeloffzen, and René G. Heideman. *High power, tunable, narrow linewidth dual gain hybrid laser*. In Laser Congress 2019 (ASSL, LAC, LS&C), page ATu1A.4. Optica Publishing Group, 2019.

[87] Ewoud Vissers, Stijn Poelman, Camiel Op de Beeck, Kasper Van Gasse, and Bart Kuyken. *Hybrid integrated mode-locked laser diodes with a silicon nitride extended cavity*. Opt. Express, 29(10):15013–15022, May 2021.

[88] Zhuqing Zhang and C.P. Wong. *Recent advances in flip-chip underfill: materials, process, and reliability*. IEEE Transactions on Advanced Packaging, 27(3):515–524, 2004.

[89] Andreas C Fischer, Fredrik Forsberg, Martin Lapisa, Simon J Bleiker, Göran Stemme, Niclas Roxhed, and Frank Niklaus. *Integrating MEMS and ICs*. Microsyst. Nanoeng., 1(1), May 2015.

[90] Takeshi Matsumoto, Teruo Kurahashi, Ryotaro Konoike, Keijiro Suzuki, Ken Tanizawa, Ayahito Uetake, Kazumasa Takabayashi, Kazuhiro Ikeda, Hitoshi Kawashima, Suguru Akiyama, and Shigeaki Sekiguchi. *Hybrid-Integration of SOA on Silicon Photonics Platform Based on Flip-Chip Bonding*. Journal of Lightwave Technology, 37(2):307–313, 2019.

[91] T. Matsumoto, T. Kurahashi, K. Tanizawa, K. Suzuki, A. Uetake, K. Takabayashi, K. Ikeda, H. Kawashima, and S. Akiyama. *In-line optical amplification for Si waveguides on 1×8 splitter and selector by flip-chip bonded InP-SOAs*. In Optical Fiber Communication Conference, page Th1C.1. Optica Publishing Group, 2016.

[92] Michael Theurer, Martin Moehrle, Ariane Sigmund, Karl-Otto Velthaus, Ruud M. Oldenbeuving, Lennart Wevers, Ferry M. Postma, Richard Mateman, Frederik Schreuder, Dimitri Geskus, Kerstin Wörhoff, Ronald Dekker, Rene G. Heideman, and Martin Schell. *Flip-Chip Integration of InP to SiN Photonic Integrated Circuits*. Journal of Lightwave Technology, 38(9):2630–2636, 2020.

[93] Nouman Zia, Heidi Tuorila, Jukka Viheriälä, Samu-Pekka Ojanen, Eero Koivusalo, Joonas Hilska, and Mircea Guina. *Hybrid silicon photonics DBR laser based on flip-chip integration of GaSb amplifiers and μm-scale SOI waveguides*. Opt. Express, 30(14):24995–25005, Jul 2022.

[94] Bowen Song, Ludovico Megalini, Sarvagya Dwivedi, Sasa Ristic, and Jonathan Klamkin. *High-Thermal Performance 3D Hybrid Silicon Lasers*. IEEE Photonics Technology Letters, 29(14):1143–1146, 2017.

[95] Bowen Song, Cristian Stagarescu, Sasa Ristic, Alex Behfar, and Jonathan Klamkin. *3D integrated hybrid silicon laser*. Opt. Express, 24(10):10435–10444, May 2016.

[96] Shiyun Lin, Xuezhe Zheng, Jin Yao, Stevan S. Djordjevic, John E. Cunningham, Jin-Hyoung Lee, Ivan Shubin, Ying Luo, Jock Bovington, Daniel Y. Lee, Hiren D. Thacker, Kannan Raj, and Ashok V. Krishnamoorthy. *Efficient, tunable flip-chip-integrated III-V/Si hybrid external-cavity laser array*. Opt. Express, 24(19):21454–21462, Sep 2016.

[97] Jeroen Goyvaerts. *Near-infrared GaAs-on-SiN photonic integration platform based on micro-transfer-printing*. PhD thesis, Ghent University, 2021.

[98] "John E. Bowers Di Liang". *Recent Progress in Heterogeneous III-V-on-Silicon Photonic Integration*, 2021.

[99] U. Gösele, Y. Bluhm, G. Kästner, P. Kopperschmidt, G. Kräuter, R. Scholz, A. Schumacher, St. Senz, Q.-Y. Tong, L.-J. Huang, Y.-L. Chao, and T. H. Lee. *Fundamental issues in wafer bonding*. Journal of Vacuum Science & Technology A, 17(4):1145–1152, 07 1999.

[100] F. Niklaus, H. Andersson, P. Enoksson, and G. Stemme. *Low temperature full wafer adhesive bonding of structured wafers*. Sensors and Actuators A: Physical, 92(1):235–241, 2001. Selected Papers for Eurosensors XIV.

[101] S. Keyvaninia, M. Muneeb, S. Stanković, P. J. Van Veldhoven, D. Van Thourhout, and G. Roelkens. *Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate*. Opt. Mater. Express, 3(1):35–46, Jan 2013.

[102] I. Christiaens, G. Roelkens, Kurt De Mesel, D. Van Thourhout, and R. Baets. *Thin-film devices fabricated with benzocyclobutene adhesive wafer bonding*. Journal of Lightwave Technology, 23(2):517–523, 2005.

[103] G. Roelkens, J. Brouckaert, D. Thourhout, Van, R.G.F. Baets, R. Nötzel, and M.K. Smit. *Adhesive bonding of InP/InGaAsP dies to processed silicon-on-insulator wafers using DVS-bis-benzocyclobutene*. Journal of the Electrochemical Society, 153(12):G1015–G1019, 2006.

[104] D. Pasquariello and K. Hjort. *Plasma-assisted InP-to-Si low temperature wafer bonding*. IEEE Journal of Selected Topics in Quantum Electronics, 8(1):118–131, 2002.

[105] Dongling Li, Zhengguo Shang, Yin She, and Zhiyu Wen. *Investigation of Au/Si Eutectic Wafer Bonding for MEMS Accelerometers*. Micromachines, 8(5), 2017.

[106] Xianshu Luo, Yulian Cao, Junfeng Song, Xiaonan Hu, Yuanbing Cheng, Chengming Li, Chongyang Liu, Tsung-Yang Liow, Mingbin Yu, Hong

Wang, Qi Jie Wang, and Patrick Guo-Qiang Lo. *High-Throughput Multiple Dies-to-Wafer Bonding Technology and III/V-on-Si Hybrid Lasers for Heterogeneous Integration of Optoelectronic Integrated Circuits*. Frontiers in Materials, 2, 2015.

[107] Gunther Roelkens. *Heterogeneous III-V/Silicon Photonics: Bonding Technology and Integrated Devices*. PhD thesis, Universiteit Gent, 2007.

[108] Alexander W. Fang, Hyundai Park, Oded Cohen, Richard Jones, Mario J. Paniccia, and John E. Bowers. *Electrically pumped hybrid AlGaInAs-silicon evanescent laser*. Opt. Express, 14(20):9203–9210, Oct 2006.

[109] G. Roelkens, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit. *Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a Silicon-on-Insulator waveguide circuit*. Opt. Express, 14(18):8154–8159, Sep 2006.

[110] Intel. *Intel® Silicon Photonics*, 2024.

[111] Hyundai Park, Chong Zhang, Minh A. Tran, and Tin Komljenovic. *Heterogeneous silicon nitride photonics*. Optica, 7(4):336–337, Apr 2020.

[112] Yuting Shi, Zhechao Wang, Joris Van Campenhout, Marianna Pantouvaki, Weiming Guo, Bernardette Kunert, and Dries Van Thourhout. *Optical pumped InGaAs/GaAs nano-ridge laser epitaxially grown on a standard 300-mm Si wafer*. Optica, 4(12):1468–1473, Dec 2017.

[113] Yu Han, Wai Kit Ng, Chao Ma, Qiang Li, Si Zhu, Christopher C. S. Chan, Kar Wei Ng, Stephen Lennon, Robert A. Taylor, Kam Sing Wong, and Kei May Lau. *Room-temperature InP/InGaAs nano-ridge lasers grown on Si and emitting at telecom bands*. Optica, 5(8):918–923, Aug 2018.

[114] Daehwan Jung, Zeyu Zhang, Justin Norman, Robert Herrick, M. J. Kennedy, Pari Patel, Katherine Turnlund, Catherine Jan, Yating Wan, Arthur C. Gossard, and John E. Bowers. *Highly Reliable Low-Threshold InAs Quantum Dot Lasers on On-Axis (001) Si with 87% Injection Efficiency*. ACS Photonics, 5(3):1094–1100, 2018.

[115] Jinkwan Kwoen, Bongyong Jang, Joohang Lee, Takeo Kageyama, Katsuyuki Watanabe, and Yasuhiko Arakawa. *All MBE grown InAs/GaAs quantum dot lasers on on-axis Si (001)*. Opt. Express, 26(9):11568–11576, Apr 2018.

[116] Siming Chen, Wei Li, Jiang Wu, Qi Jiang, Mingchu Tang, Samuel Shutts, Stella N. Elliott, Angela Sobiesierski, Alwyn J. Seeds, Ian Ross, Peter M.

Smowton, and Huiyun Liu. *Electrically pumped continuous-wave III–V quantum dot lasers on silicon*. Nature Photonics, 10(5):307–311, 2016.

[117] Shi, Yuting. *GaAs nano-ridge lasers epitaxially grown on silicon*. PhD thesis, Ghent University, 2020.

[118] Takuro Fujii, Tatsurou Hiraki, Takuma Aihara, Hidetaka Nishi, Koji Takeda, Tomonari Sato, Takaaki Kakitsuka, Tai Tsuchizawa, and Shinji Matsuo. *Development of an Epitaxial Growth Technique Using III-V on a Si Platform for Heterogeneous Integration of Membrane Photonic Devices on Si*. Applied Sciences, 11(4), 2021.

[119] Mitsuru Sugo, Hidefumi Mori, Masami Tachikawa, Yoshio Itoh, and Mitsuo Yamamoto. *Room-temperature operation of an InGaAsP double-heterostructure laser emitting at 1.55 μm on a Si substrate*. Applied Physics Letters, 57(6):593–595, 08 1990.

[120] Alan Y. Liu, Chong Zhang, Justin Norman, Andrew Snyder, Dmitri Lubyshev, Joel M. Fastenau, Amy W. K. Liu, Arthur C. Gossard, and John E. Bowers. *High performance continuous wave 1.3$\mu m$ quantum dot lasers on silicon*. Applied Physics Letters, 104(4):041104, 01 2014.

[121] Zhechao Wang, Bin Tian, Marianna Pantouvaki, Weiming Guo, Philippe Absil, Joris Van Campenhout, Clement Merckling, and Dries Van Thourhout. *Room-temperature InP distributed feedback laser array directly grown on silicon*. Nature Photonics, 9(12):837–842, 2015.

[122] Dhoore, Sören. *Heterogeneously Integrated III-V-on-Silicon Wavelength-Tunable DFB and DBR Lasers*. PhD thesis, Ghent University, 2018.

[123] E. Menard, K. J. Lee, D.-Y. Khang, R. G. Nuzzo, and J. A. Rogers. *A printable form of silicon for high performance thin film transistors on plastic substrates*. Applied Physics Letters, 84(26):5398–5400, 06 2004.

[124] Matthew A. Meitl, Zheng-Tao Zhu, Vipan Kumar, Keon Jae Lee, Xue Feng, Yonggang Y. Huang, Ilesanmi Adesida, Ralph G. Nuzzo, and John A. Rogers. *Transfer printing by kinetic control of adhesion to an elastomeric stamp*. Nature Materials, 5(1):33–38, 2006.

[125] C. A. Bower, E. Menard, S. Bonafede, J. W. Hamer, and R. S. Cok. *Active-matrix OLED display backplanes using transfer-printed microscale integrated circuits*. In 2010 Proceedings 60th Electronic Components and Technology Conference (ECTC), pages 1339–1343, 2010.

[126] David Gomez, Kanchan Ghosal, Matthew A. Meitl, Salvatore Bonafede, Carl Prevatte, Tanya Moore, Brook Raymond, David Kneeburg, Alin Fecioru, António Jose Trindade, and Christopher A. Bower. *Process Capability and Elastomer Stamp Lifetime in Micro Transfer Printing*. In 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), pages 680–687, 2016.

[127] John Justice, Chris Bower, Matthew Meitl, Marcus B Mooney, Mark A Gubbins, and Brian Corbett. *Wafer-scale integration of group III–V lasers on silicon using transfer printing of epitaxial layers*. Nature Photonics, 6(9):610–614, 2012.

[128] XDisplay Company. *XDisplay TM: Leading Developer and Licensor of Advanced Assembly and Display Solutions*, 2024.

[129] De Groote, Andreas. *Heterogeneous integration of multibandgap III-V semiconductor light sources on silicon photonics*. PhD thesis, Ghent University, 2017.

[130] Andreas De Groote, Paolo Cardile, Ananth Z. Subramanian, Alin M. Fecioru, Christopher Bower, Danae Delbeke, Roel Baets, and Günther Roelkens. *Transfer-printing-based integration of single-mode waveguide-coupled III-V-on-silicon broadband light emitters*. Opt. Express, 24(13):13754–13762, Jun 2016.

[131] Haq, Bahawal and Roelkens, Günther. *Alignment-tolerant taper design for transfer printed III-V-on-Si devices*. In Integratred Optics, 21st European conference, Papers, page 3, 2019.

[132] X-Celeprint. *uTP-100 micro transfer printer, model MTP1001. User manual*, 2015.

[133] Aston Photonics. *European Training Network WON "Wideband Optical Networks"*, 2019.

[134] MedPhab. *MedPhab: Photonics Medical Devices*, 2020.

[135] MedPhab. *MedPhab: Fast track from idea to product in photonics-based medical devices*, 2024.

[136] imec. *III-V-on-Si via Micro-Transfer-Printing - MedPhab Community Marketplace*, 2020.

# 2

# Ultra-wide Tunable Narrow-linewidth III-V on Si Laser

This chapter is structured into five sections as follows:

- Aiming for ultra-wide tunable narrow-linewidth lasers (2.1): This section centers on the goal of demonstrating an ultra-wide tunable narrow linewidth III-V-on-Si laser using $\mu$TP integration of pre-fabricated SOAs and explains the rationale for targeting such a specific requirement standard.
- Design (2.2): This section outlines the fundamentals of a laser and progresses to a specific layout design that aligns with the set requirement of the integrated laser in section 2.1. To provide a clearer picture, the design steps are accompanied by a concise theoretical review of the basic principles of the laser as well as the concept of linewidth reduction.
- Fabrication (2.3): This section details the fabrication processes of the integrated widely-tunable and narrow linewidth laser using $\mu$TP.
- Characterization (2.4): This section presents the performance of the integrated laser, comprising the basic operation, tunability, and linewidth characteristics.
- Broader Application Demonstrators (2.5): This section briefly presents additional application demonstrators that extend the use of the laser design introduced earlier, showcasing its versatility in biomedical sensing, spectroscopy, gas detection, coherence-critical systems, and programmable photonics.

- Conclusion (2.6): This final section reviews the significance of the work and the provided demonstrations.

## 2.1 Aiming for ultra-wide tunable narrow-linewidth lasers

Here in this section, we delve into the motivation behind the need for ultra-wide tunable narrow-linewidth integrated lasers, a topic we touched upon in the first chapter (1).

Silicon Photonics (SiPh) is a relatively nascent field, brimming with potential applications due to its compatibility with CMOS and compactness. As the field evolves, new applications for SiPh continue to emerge. Each application has unique requirements (such as wavelength stability, tunability, output power, linewidth, and integration compatibility) on the optical source, leading to a lack of a specific general standard. Even within the same application, requirements can vary due to differences among manufacturers and the platform itself (Si, SiN, etc).

Currently, the primary drivers for SiPh is Datacom followed by sensing and medical applications, as discussed in the first chapter (1). Fortunately, in the field of Datacom, laser requirements based on desired data rates are standardized by the Optical Internetworking Forum (OIF).

The OIF is a non-profit consortium that was founded in 1998 [1]. It promotes the development and deployment of interoperable computer networking products and services through implementation agreements (IAs) for optical networking products and component technologies, accelerating the market adoption of optical networking technologies. The OIF has more than 150 member companies spanning component suppliers to network operators [2]. OIF members are committed to identifying the industry's needs and requirements. They rapidly develop solutions that have a direct impact on and facilitate global connectivity in the open network world.

For a quarter of a century, OIF has been at the forefront of driving transformation in optical networking. As the sole global industry forum, it has been instrumental in promoting electrical, optical, and control interoperability, thereby enabling a more efficient and reliable network [3, 4].

The OIF's interoperability solutions, which are based on established methodologies such as documenting industry requirements, proposing member-driven technical solutions, conducting validation testing, and free publishing, are indispensable to the global network.

To cater to the growing data rates and bandwidth needs in the realm of Datacom, the OIF has seen the evolution of optical communication standards, including 100G [5], 400G-ZR [6], and setting up IAs of 800G [7] and 1600G [8]. The shift

from 10G to 100G marked a significant milestone, enabling a tenfold increase in data transmission speeds. The subsequent adoption of 400G standards offered another leap in capacity, with 800G and 1600G standards set to further redefine the capabilities of fiber-optic networks.

### 2.1.1 OIF 400G-ZR Standard

The 400G-ZR standard, developed by the OIF for the coherent communication, is a significant advancement in optical networking by enabling more flexible network deployment strategies, including optimization of spectral efficiency and tunable optical wavelength resources [9]. It enables the transfer of 400 Gigabit Ethernet over a single optical wavelength, leveraging technologies like dense wavelength division multiplexing (DWDM) and higher-order modulation such as Quadrature Amplitude Modulation (e.g. 16-QAM) [6, 10]. This standard provides an interoperable interface for 400G data transmission, marking a pioneering standard in this domain [11, 12].

The benefits of 400G-ZR are derived from its adoption of cutting-edge coherent optical technology, which provides robust support for high-capacity point-to-point data transport over Data Center Interconnect (DCI) links spanning distances between 80 and 120 km. Moreover, the intentionally limited performance of 400G-ZR modules ensures cost efficiency and compact physical dimensions, facilitating integration into smaller modules like the Quad Small Form-Factor Pluggable Double-Density (QSFP-DD) and Octal-Small Form-Factor Pluggable (OSFP) [11, 12].

As data center architectures become increasingly distributed to meet the growing demands for processing and storage, Global Content Network (GCN) companies need to connect these data centers in distributed clusters. These clusters require massive interconnect bandwidth and need to be in close proximity. The 400G-ZR standard meets these requirements, providing a full-bandwidth optical interconnect solution that delivers both high capacity and high density [11].

In the coming years, a new part of the network will undergo transformation with 400G-ZR solutions meeting the specific space, power, and operational requirements of single-span DCI network connections. This evolution marks a significant growth in data center construction, a trend set to continue, driven by the operation and evolution of networks to support cloud services on a massive scale [11, 12].

For instance, Coherent Inc., acquired by II-VI Incorporated and rebranded as Coherent, showcased its award-winning 100G and 400G digital coherent optics (DCO) transceivers at OFC 2023. These transceivers are expected to fundamentally change how optical transport networks are deployed, simplifying network architectures by eliminating unnecessary layers of equipment [13]. Moreover, II-

VI Incorporated, rebranded as Coherent, shipped its 400G-ZR+ QSFP-DD-DCO transceivers, the world's first with 0 dBm output power, to Windstream Wholesale (which has recently rebranded as Uniti Wholesale) for field qualification [14]. These transceivers are the world's first digital coherent optics with the highest optical output power of 0 dBm that can plug directly into QSFP-DD transceiver slots on IP routers. This technology allows routers to be directly connected to access, metro, and regional DWDM transport networks without additional intermediary interfaces, significantly reducing both capital and operational expenditures [14].

The limits related to the integrated laser extracted from the optical specifications on transmitter side, specified by 400G-ZR, are summarized in the Table 2.1.

| | |
|---|---|
| Wavelength Range (nm) | 1530–1625 (C+L-band) |
| Intrinsic Linewidth[1] (kHz) | 500 |
| Frequency Accuracy (GHz) | $\pm 1.8$ |
| RIN (dB/Hz) | –145 (Avg.) & –140 (Peak) |
| Output Power Window[2] (dBm) | –10 to 0 |

† 400G-ZR defines a mask that specifies the maximum allowable laser frequency noise power spectral density (PSD) for coherent communication systems. The intrinsic linewidth of a laser can be estimated from the flat region of the frequency noise PSD at high offset frequencies, typically the last two decades, where the noise is dominated by white frequency noise. In this region, the linewidth is related to the frequency noise by the following expression: $\Delta\nu = \pi \cdot S_\nu$, where $S_\nu$ is the flat frequency noise level in units of $Hz^2/Hz$. This relationship and the extraction method are further discussed in Section 2.4.

‡ This is the transmitter's allowable output power window. There is no direct specification on the laser's launch power in 400G-ZR.

*Table 2.1: Integrated laser's requirements extracted from the optical specifications of a 400G-ZR transmitter [6].*

The key requirements for integrated lasers in the 400G-ZR (remained the same for 800G) are challenging to meet but are strict enough to serve as a standard in other applications as well (potentially with additional limits for each specific application). Therefore, in our demonstration, we aim to meet the most important general requirements of wavelength range and intrinsic linewidth. To ensure the lasers are also useful for sensing and medical applications, we aim to extend the wavelength range beyond what is required in Datacom (400G-ZR and above). A broader tunability range generally results in a wider sensing spectrum, which could be beneficial for sensing as well as medical applications.

## 2.2 Design

In this section, we concentrate on the design of a laser that is widely tunable and possesses a narrow linewidth, in order to fulfill the previously mentioned specifi-

cations. We begin by introducing the basic principles of a laser and discussing the essential components needed for a III-V-on-Si laser. We then shift our focus to the design and requirements of a narrow linewidth laser, starting with the underlying theory and progressing towards the construction of the layout. Subsequently, we delve into the requirements for utlra-wide tunability. The section concludes with the finalization of our laser design.

### 2.2.1 Building Blocks of a III-V-on-Si laser

A laser, which stands for "Light Amplification by Stimulated Emission of Radiation," is a device that emits coherent light through a process of optical amplification. The key components of a basic laser, as shown in Fig. 2.1, include:

- Active Medium: This is the source of optical gain within a laser. The active medium can be a gas, liquid, or solid that amplifies the light signal by the process of stimulated emission.
- Optical Resonator: This is typically formed by two mirrors that reflect light back and forth through the active medium, allowing the light to build up to a high intensity. This configuration is known as a standing-wave cavity, or Fabry–Pérot resonator, where the mirrors create a stationary interference pattern. Alternatively, some lasers use a traveling-wave cavity, such as a ring resonator, which can be mirrorless and allows light to circulate in one direction. In the Fabry–Pérot type, one of the mirrors in the optical resonator is partially reflective, allowing some light to escape. This is where the amplified light exits the laser cavity with the same phase in the same direction, coherently.
- Pump Source: This provides the energy required to excite the atoms or molecules in the active medium to higher energy states. The pump source can be electrical (e.g., current injection in semiconductor lasers) or optical (e.g., another laser) depending on the laser type. It is not shown in the figure.

Figures 2.2 and 2.3 illustrate how the laser schematic can be modified to align with both hybrid and heterogeneous integration methods. These methods, comprehensively explored in Chapter 1 (1), play a crucial role in the evolution of integrated lasers.

In the context of this chapter, our primary focus is the utilization of prefabricated III-V SOA as a gain medium. This gain medium is heterogeneously integrated into the IMEC 400nm+ platform, described in the section 1.3.2, using the $\mu$TP technique. Consequently, our attention is particularly drawn to Fig. 2.3.

In the subsequent sections, we will delve into the components required to construct the desired laser. Each component's role and interaction within the system

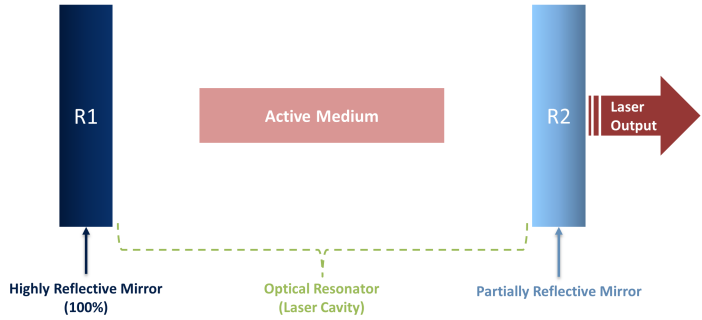



*Figure 2.1: Basic Schematic of a Laser.*

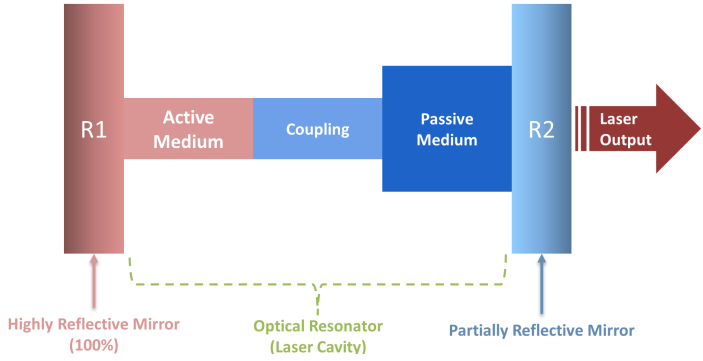



*Figure 2.2: Basic Schematic of a hybrid laser.*

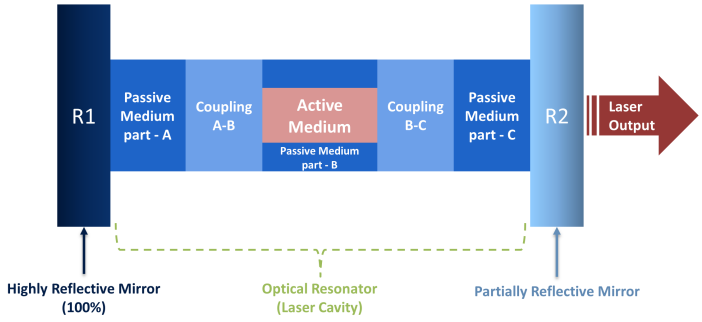



*Figure 2.3: Basic Schematic of a heterogeneous laser.*

will be explained, providing a comprehensive understanding of the laser's operation and performance.

#### 2.2.1.1 Si-Waveguide

The first basic component of a SiPh platform is the Si waveguide (WG). Full etch and 180 nm partial etch steps are available in the IMEC 400nm+ platform, enabling the formation of two types of WGs: wire-waveguide (WWG) and rib-waveguide (RWG) as shown in the Fig. 2.4. Waveguides in the SiPh platform act not only as a photonics wire to connect integrated photonics components together, but also as a generic module to build other components of the photonics platform. For instance, Bend-WGs (BWGs), Spot-Size converters (SSCs), Transition Tapers (TTs), Directional Couplers (DCs), Micro-Ring Resonators (MRRs), and others are built based on the WG cross-sections.

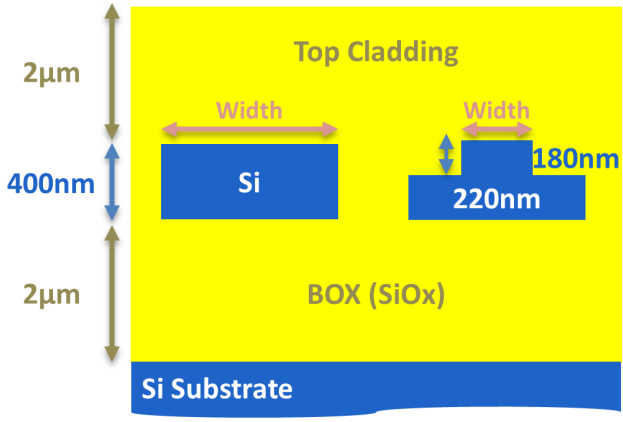



*Figure 2.4: Schematic cross-section of IMEC 400nm+ pltaform's WWG (left) and RWG (right). The scale is not kept for a better representation.*

To ensure maintaining single-mode operation, the width of the WWG and RWG are set to 450 nm and 650 nm, respectively. This is illustrated in Fig. 2.5, and Fig. 2.6, presenting the simulation results done at the wavelength of 1550 nm, where the highest effective index difference between the zeroth order mode (zeroth Transverse Electric or TE0) from the first (Zeroth Transverse Magnetic or TM0) and second order (TE1) modes has been sought. The widest options (450 nm for WWG, and 650 nm for RWG) are chosen to maximize the confinement of the TE0 mode within Si core, while minimizing the mode's interactions with the sidewalls and thereby reducing the sidewall scattering loss, as demonstrated for the WWG in Fig. 2.7. Table 2.2 summarizes the RWG specifications extracted from the simulations and the measurements.

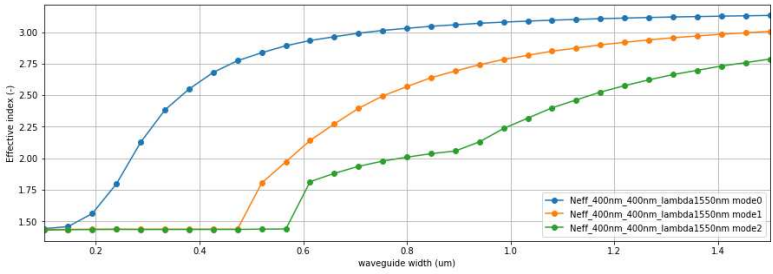



*Figure 2.5: Effective Index vs. the Core width of WWG at 1550 nm.*

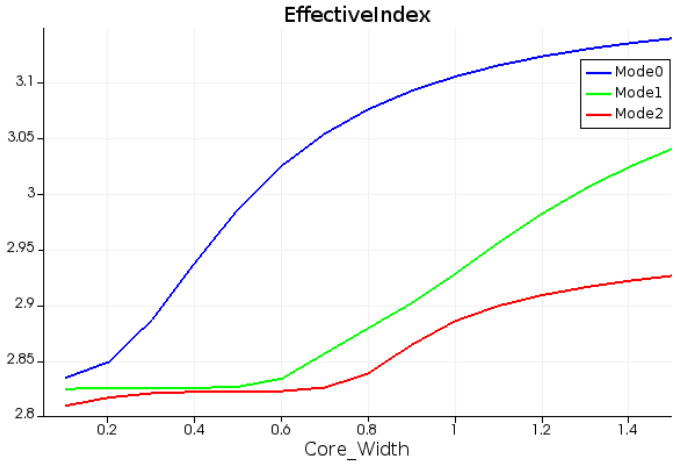



*Figure 2.6: Effective Index vs. the Core width of RWG at 1550 nm.*

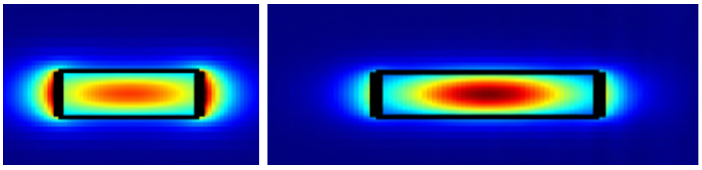


*Figure 2.7: Fundamental mode profile at 1550 nm with WWG width of 350 nm (left), and 450 nm (right) to maximize the confinement in the Si core or minimizing the sidewall loss.*

#### 2.2.1.2 Grating Coupler

A grating coupler (GC) is a component that utilizes a periodic structure to diffract light out-of-plane. Grating couplers can be implemented at any location on a chip, not just the edges (in contrast to edge couplers). This advantage makes them a key interface for out-coupling laser light from the SiPh circuit to the outside world,

| | |
|---|---|
| Core Width ($\mu$m) | 0.65 |
| Effective Index | 3.06 |
| Group Index | 3.82 |
| Loss (dB/cm) | 1$\pm$0.15 |

*Table 2.2: IMEC 400nm+ RWG specifications extracted from the simulations and measurements.*

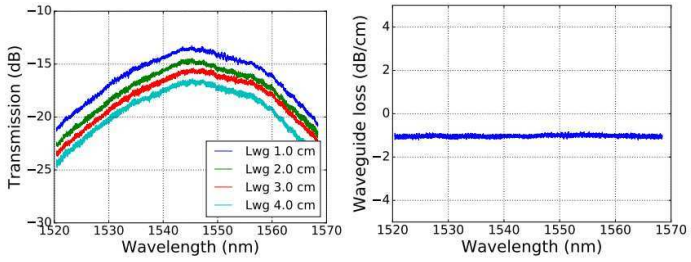



*Figure 2.8: (a): Measured transmission spectra for a set of waveguides with different length, (b): Calculated propagation loss of the fundamental TE mode in 650 nm wide rib waveguide [15].*

such as a fiber optic cable, providing a crucial link between integrated photonics and fiber optics. The key figure of merits (FoMs) in the design of a grating coupler include the coupling efficiency, back-reflection and operational bandwidth at the target wavelength. They are highly sensitive to the grating's pitch, length and etch depth as well as to the fiber's position and tilting angle. These parameters are usually optimized together to maximize the performance of the device.

The IMEC 400nm+ PDK includes a GC with a coupling peak at 1550 nm under 10 degrees of fiber angle (to minimize the back-reflection into the WG). Fig. 2.9 shows the screenshot of the GDS layout of the grating coupler and the measured insertion loss spectrum.

#### 2.2.1.3 Multi-mode-interfrometer (MMI)

A multi-mode interferometer (MMI), also known as a multimode interference coupler, is a microscale structure in which multiple modes are excited in a wide waveguide, interfere during propagation, and form self-images of the input field at the output ports, enabling predictable splitting or combining of optical power.

MMIs are designed not only to output a certain fraction of the input power, but are also designed so that the outputs have a certain phase difference. This makes MMIs crucial for splitting and combining light in the cavity.

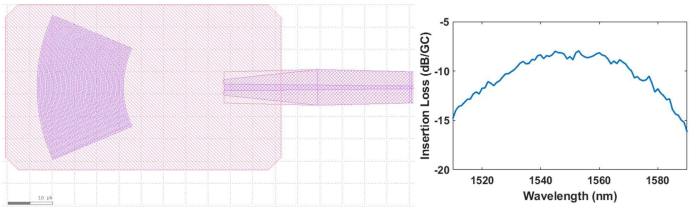



*Figure 2.9: The screenshot of the GDS layout of the IMEC 400nm+ PDK grating coupler (left), and it's insertion loss spectrum (right).*

An ideal 1x2 MMI would be a 50/50 power splitter, such that light enters along one path and exits along two paths, with half the power in each exit path. A 2x2 MMI can perform a similar function but uses a symmetric structure that enables more complex signal routing.

The simulation results of the 1x2 and 2x2 MMIs are shown in Fig. 2.10 and Fig. 2.11, respectively.

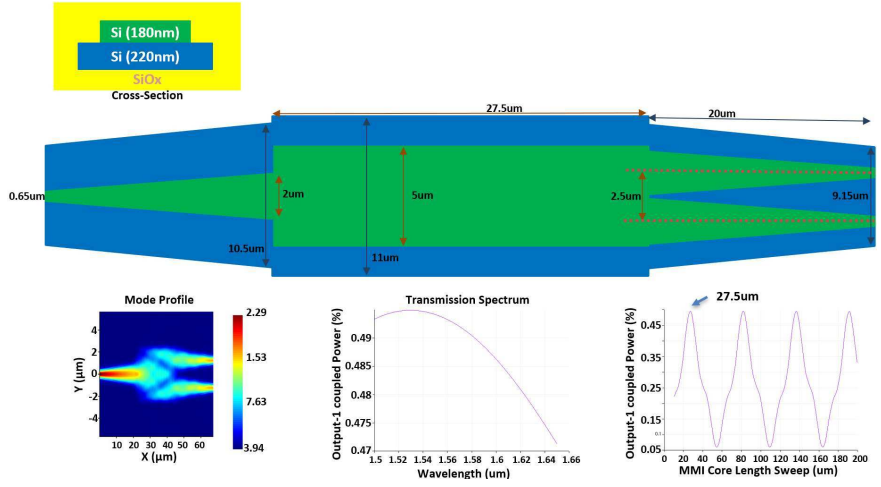



*Figure 2.10: The schematic layout design of the 50/50 1x2 MMI based on IMEC 400nm+ RWG, The mode profile, transmission spectrum, and coupling percentage vs. the core length of the MMI.*

In addition to splitting and combining light, MMIs can also be used as partial reflectors (R2 in Fig. 2.2) in the form of a Sagnac loop mirror based on a Mach-Zehnder interferometer (MZI), as shown in the Fig. 2.12. Directional couplers in a closed loop as a Sagnac loop mirror and DBR grating filters can also be used [15], although using MMI in a Sagnac loop mirror brings the advantage of functionality over a broader wavelength range.

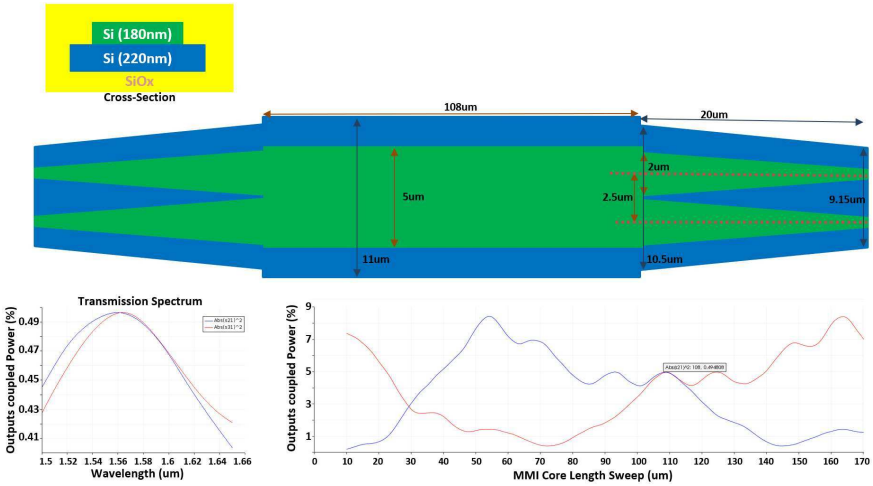



*Figure 2.11: The schematic layout design of the 50/50 2x2 MMI based on IMEC 400nm+ RWG, transmission spectrum and coupling percentage vs. the core length of the MMI.*

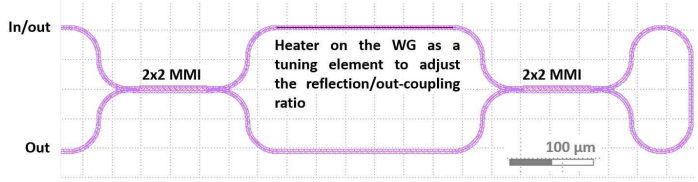



*Figure 2.12: Schematic layout of a tunable Sagnac loop mirror formed by connecting two 50/50 MMIs. In the default state (no phase shift), the structure reflects all input light back to the input waveguide due to destructive interference at the output. By applying a phase shift via a heater on one of the MZI arms, the reflection/out-coupling ratio can be tuned. The tuning range spans from 0% to 100% out-coupling.*

#### 2.2.1.4 Pre-fabricated micro-transfer-printing compatible SOA

To date, a wide variety of heterogeneously integrated lasers have been demonstrated on various silicon photonic platforms using different techniques. These lasers can be categorized into two main types based on the mode distribution in the III-V/silicon hybrid waveguide [15]. The first type, known as the evanescent laser, uses a relatively thick silicon device layer with a typically very thin bonding layer [15–18]. Consequently, the transverse optical mode is primarily confined within the silicon layer, with a small portion of the optical field evanescently extending into the overlying III-V layers. Due to the low optical confinement factor in the III-V active layers, a longer optical amplifier is often necessary to provide sufficient gain to offset the cavity loss [15]. However, a low confinement factor in

the active region does not necessarily lead to low modal gain. Other factors, such as absorption losses in the III-V layers (e.g., p-cladding and p-contact), must also be considered. For instance, some designs, such as DFB laser in [19], achieve high efficiency and short cavity lengths despite low confinement, thanks to optimized loss management and gain distribution.

In contrast, the second type predominantly confines the optical mode within the III-V region. This distribution is achieved using a silicon waveguide with a smaller cross-sectional geometry or no Si layer beneath the III-V layers [15, 20–23]. This design inherently offers higher optical gain and potentially a shorter device length. Additionally, the thickness of the bonding interface can exceed 100 nm, although a longer adiabatic taper structure is required to ensure efficient mode conversion [15]. For instance, a 185 $\mu$m long adiabatic inverted taper structure is used in [20].

Beyond the optical coupling between the III-V layer and the silicon waveguide, meticulous attention must be given to the design of the hybrid waveguide cross-section. For example, aluminum-containing III-V materials (e.g., AlGaInAs) are susceptible to oxidation at room temperature. This issue can be effectively addressed through surface passivation using $(NH_4)_2S$ in combination with dielectric encapsulation [15, 24, 25]. Alternatively, mitigating this problem can be achieved by confining carriers and photons away from the sidewalls of the QW waveguide. A mesa structure featuring a wide quantum well but a relatively narrower InP mesa can serve this purpose [15]. Figure 2.13 depicts a schematic cross-section of a classic heterogeneously integrated III-V-on-silicon laser developed by the Photonics Research Group at Ghent University, utilizing the evanescent coupling scheme (Fig. 2.14).

Later on, the same group conducted an intensive study on evanescent coupling, as detailed in [23], to develop micro-transfer printing ($\mu$TP) compatible SOAs with a focus on adiabatic alignment-tolerant taper design. Meanwhile, [15] examined the impact of BCB thickness and taper's length and tip-width on a $\mu$TP-compatible SOA design (figures 2.4 and 2.8 in [15]), presenting several first-time demonstrations of $\mu$TP integrated lasers and detectors. This PhD thesis builds upon the foundations laid by these references, leveraging the robust $\mu$TP-compatible SOA designs they have developed.

The PhD thesis referenced in [23] presents two types of evanescent-based hybrid III-V-on-Si SOA designs, as depicted in Fig 2.15. These designs are referred to as partial coupling and full coupling.

For this thesis, we have chosen to proceed with the partial coupling design due to its several advantages over the full coupling design:

- Partial coupling eliminates the constraint of longitudinal alignment, making it a more reliable design, as illustrated in Fig. 2.15. It also offers more flexibility for circuit designers.

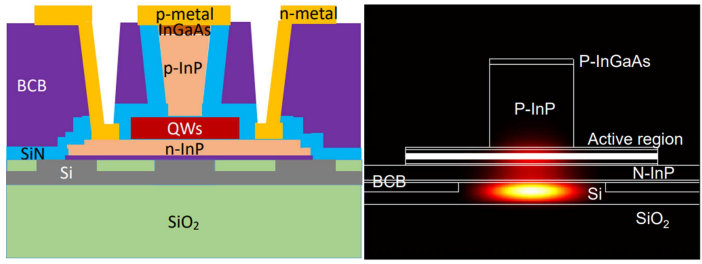



*Figure 2.13: Schematic layout of a cross-section of the III-V-on-Si laser (left), and the intensity profile of the fundamental optical mode in the hybrid III-V/Si waveguide (right) [15].*

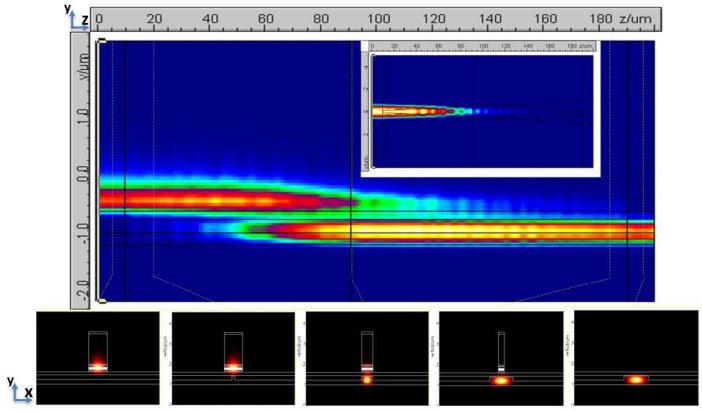



*Figure 2.14: Simulated optical mode conversion over the adiabatic taper structure [15].*

- The photonic circuit remains functional and measurable even without the integrated III–V components thanks to the presence of the continuous Si waveguide in the active region.
- The partial coupling design removes the need for a Si taper to facilitate coupling with the III-V taper. Instead, a simple wide Si RWG can be used. This simplification makes it easier to provide $\mu$TP-compatible SOA on other SiPh platforms (like iSiPP50G), and even on other material platforms like SiN platforms (as demonstrated in [26]; see also Chapter 2, Section 2.5.3 for a related discussion). The required modifications may involve the III-V taper and, in some cases, only the width of the underlying passive waveguide. This design also offers flexibility in selecting different III–V device lengths.
- The aforementioned point also contributes to a more generic design, supporting the idea of making the $\mu$TP-compatible SOA a PDK component across different platforms.

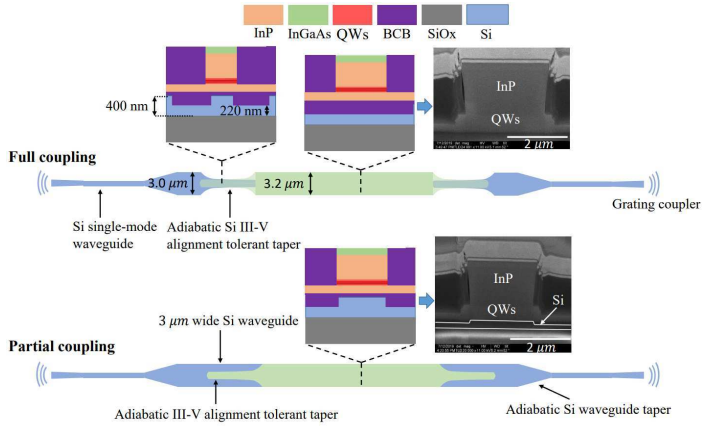



*Figure 2.15: Schematics and FIB cross-sections illustrating the design of the full-coupling and partial-coupling III-V-on-Si SOAs [23].*

- Partial coupling scheme has been shown to offer improved coupling efficiency and robustness to lateral integration misalignment, as illustrated in Fig. 2.16 [23]. This has been demonstrated on both the Si-400 nm and iSiPP50G platforms. In the case of iSiPP50G, a 160 nm thick poly-Si layer (with a refractive index close to c-Si) is incorporated on top of the 220 nm thick c-Si (see Fig. 2.17). This compensates for the lower thickness of c-Si in iSiPP50G compared to the Si-400 nm platform, resulting in a total thickness close to 400 nm for efficient optical coupling.

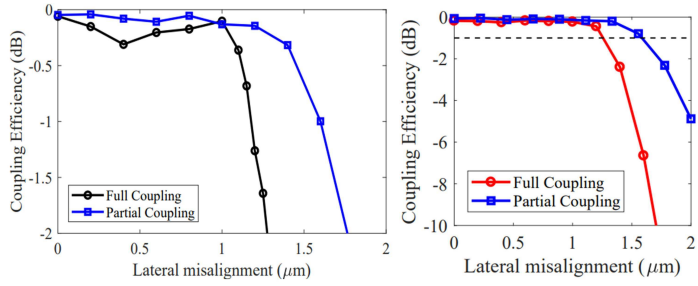



*Figure 2.16: The simulated coupling efficiency of the adiabatic taper structures for the partial and full-coupling designs versus the lateral misalignment: Si-400 nm (left), iSiPP50G (right) [23].*

- The partial coupling scheme allows for the incorporation of a DFB laser by including gratings within the underlying passive Si waveguide. This has been demonstrated in both [23] (Fig. 2.18) and [15]. Both partial and full

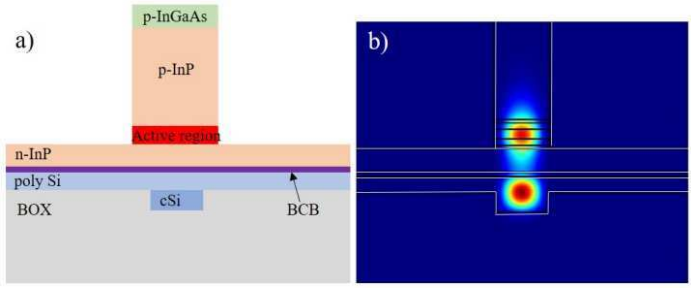



*Figure 2.17: Schematic illustration and simulated mode profile of the ISIPP50G waveguide cross-section with integrated SOA [23].*

coupling designs have the potential to define DBR lasers (see Fig. 2.19).

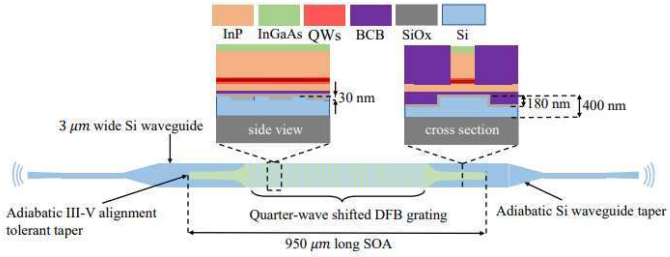



*Figure 2.18: Schematic illustrating the design of the DFB laser, the cross-section view of the adiabatic taper and the side view of the DFB grating [23].*

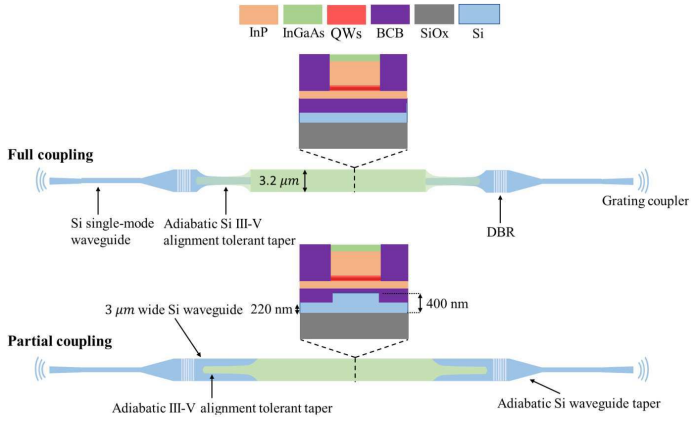



*Figure 2.19: Design schematic of full-coupling and partial-coupling DBR lasers. The cross-section in the gain section is also illustrated [23].*

Taking into account these advantages, along with the higher tolerance versus the lateral misalignment up to about 1.5 $\mu$m as re-presented from [23] in Fig. 2.20, Fig. 2.21, and Fig. 2.22, we plan to use a 3 $\mu$m-wide Si RWG as the underlying passive waveguide in the partial coupling scheme.

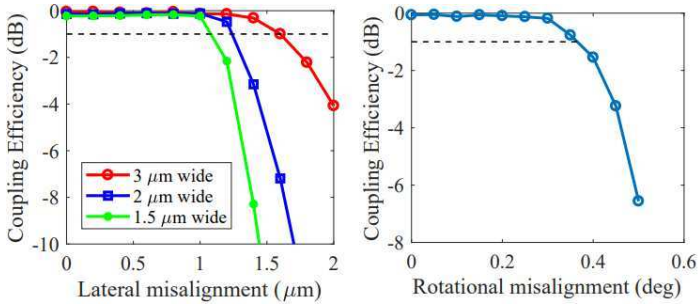



*Figure 2.20: (left) Calculated power coupling between full-coupling III-V adiabatic taper design and Si waveguide of width 3.0 μm, 2.0 μm and 1.5 μm, (right) Calculated coupling efficiency against the rotational misalignment between III-V adiabatic taper and Si waveguide [23].*

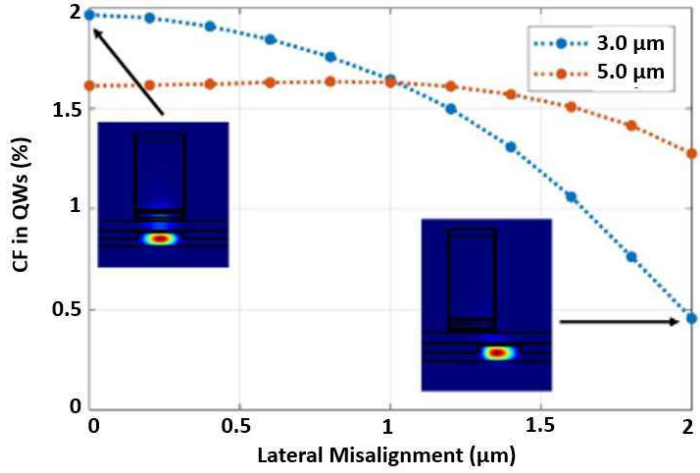



*Figure 2.21: The change in confinement factor in QWs with the misalignment variation for 3.0 μm and 5.0 μm Si waveguide width, insets illustrate the mode profile at zero and 2.0 μm misalignment [23].*

Figure 2.23 provides a schematic and layout design representation of the III-V-on-Si SOA that we intend to utilize in this work.

Figure 2.24(a) presents the simulated optical coupling between the III–V and silicon waveguides based on the design proposed in this work. Figure 2.24(b)

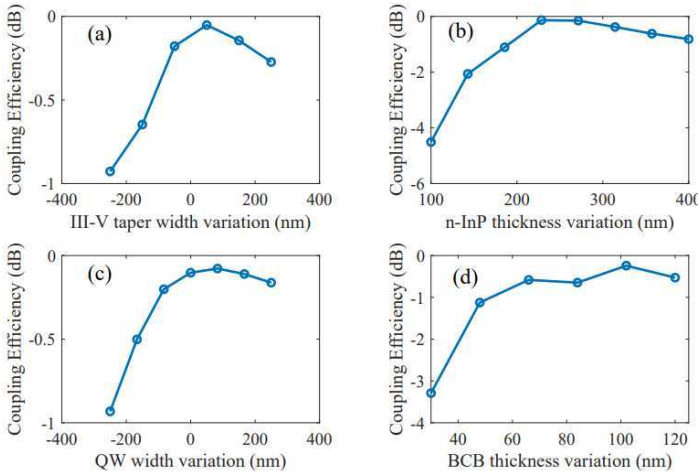



*Figure 2.22: (a) Calculated coupling efficiency for variation in a) adiabatic III-V taper width, (b) n-InP thickness, (c) QW width and (d) BCB thickness [23].*

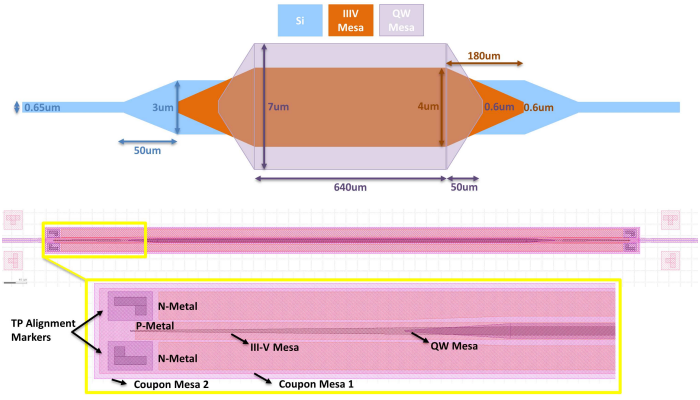



*Figure 2.23: Schematic (Top) and layout design (Bottom) of this work's SOA.*

illustrates the relationship between mode confinement and transmission efficiency as a function of the lateral misalignment between the transfer-printed SOA and the underlying silicon waveguide [27].

To fully populate a 2-inch InP epitaxial wafer, the following variations were considered in the design of the SOAs:

- Coupon's Mesa Width: Each quarter of the wafer is dedicated to SOAs with mesa widths of 2 $\mu$m, 3 $\mu$m, 4 $\mu$m, and 6 $\mu$m (its reason is further discussed in the section 2.2.2.2), while coupon's total width is kept as 47.5 $\mu$m to maintain the compactness and uniform outline for more uniform fabrication

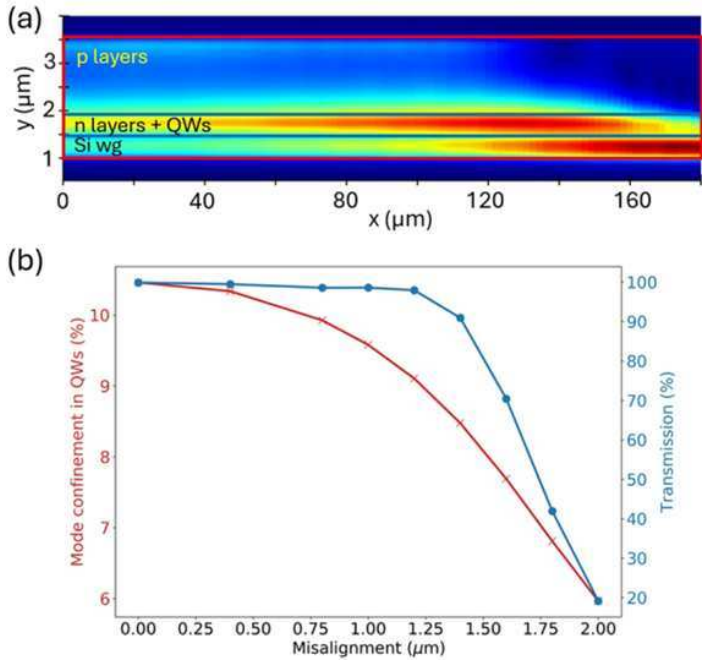



*Figure 2.24: Simulated optical coupling from the III–V to silicon. (a) Optical intensity distribution showing mode coupling between the silicon waveguide and III–V layers. (b) Impact of µTP misalignment on mode confinement and transmission efficiency [27].*

and easier integration.

- Coupon's Total Length: Each variation includes three lengths (≈800 $\mu$m, ≈1 mm, and ≈1.2 mm) to compare gain versus length, though this is not the context of this PhD thesis. The 1 mm long coupon is intended to be used in this PhD thesis work.

- Arrays: Three arrays for each length is considered, with a vertical pitch of 70 $\mu$m between coupons to maintain compactness.

As a result, approximately 15000 coupons are populated on the 2-inch InP wafer. Figure 2.25 shows the layout design of the populated 2-inch InP epitaxial wafer with SOA device coupons.

#### 2.2.1.5 Highly Reflective Filter

In the section 2.2.1.3, we utilized a broadband filter as a Sagnac loop mirror to partially reflect light into the laser cavity without filtering out any part of the spectrum

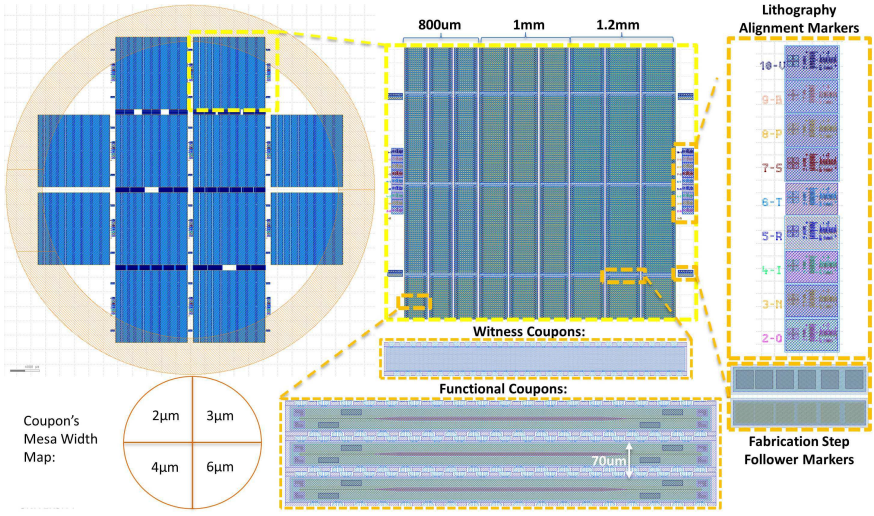



*Figure 2.25: Schematic (Top) and layout design (Bottom) of this work's SOA.*

(R2 in Fig. 2.3). However, to achieve single-mode operation for the laser and function as a highly reflective mirror (R1 in Fig. 2.3) at the same time, a narrow-band highly reflective filter must also be incorporated into the cavity. In other words, the highly reflective mirror must be a frequency-selective mirror as well.

For this purpose, we can use DBR gratings, which create DBR lasers (as presented in [23]), or ring resonators (as presented in [15]). In this PhD thesis, we opt for ring resonators as the narrow-band highly reflective filter for the laser cavity due to their advantage of small foot-print and narrow resonances. Wavelength tuning can be realized by incorporating a micro-heater on the ring's waveguide. Utlizing p-n (or p-i-n) junction inside the ring waveguide is another approach to make it tunable (available on IMEC iSiPP50G Platform). However, in this PhD thesis, we focus solely on the heater-based method (thermo-optic effect) for two reasons: first, this is the only available option on the IMEC 400nm+ Platform platform, and second, it allows for wider tuning range and is available on most SiPh platforms. We aim to demonstrate that our approach to create an integrated laser is extendable and applicable to the vast majority of SiPh platforms.

This narrow-band highly reflective filter must be carefully designed to ensure single-mode operation. It also significantly influences the wavelength tunability and linewidth of the laser. Therefore, we will thoroughly explore the design of an ultra-wide tunable and narrow-linewidth filter based on ring resonators in the following sections.

### 2.2.2 Design of Tunable Narrow-Linewidth Laser

The objective of this PhD thesis is to develop an integrated laser suitable for a range of applications, including Datacom, Telecom, sensing, and spectroscopy. As such, both wavelength tunability and narrow linewidth are critical. A narrow linewidth ensures spectral stability, while tunability enables systematic access to different wavelengths for versatile functionality [28, 29]. In this thesis, tunability refers to the overall wavelength tuning range, defined as the superimposed spectrum of all accessible lasing modes. This is not to be confused with mode-hop-free tuning, which refers to continuous tuning without abrupt jumps between cavity modes. Although mode-hop-free tuning is important for generating all relevant frequencies and avoiding missed spectral features [28, 30], its required range is application-dependent. Our final extended cavity design, along with the synchronized tuning of the ring resonators and the phase section, could potentially enable a mode-hop-free tuning range to exceed far beyond the laser cavity FSR [28, 29]. However, the focus of this thesis is on the broader wavelength tuning range, and no experimental investigation of mode-hop-free tuning is presented.

Conventionally in bulk lasers and fiber lasers, narrow-linewidth single-mode oscillation with a large mode-hop-free tuning range is achieved by tuning the lasing wavelength through moving one of the cavity mirrors (to tune the cavity modes/phase) and adjusting the filter center wavelength accordingly [31, 32]. However, this method is not feasible for fully integrated lasers, as the their parts can not be mechanically adjusted. Instead, these lasers use a phase section (PS) [33, 34] to change the phase of the recirculating light and, consequently, its wavelength [29]. Phase shifting in integrated photonics, is mostly realized through thermo-optic, strain-optic, or electro-optic effects, which typically are limited by the small values of material coefficients. As mentioned in 2.2.1.5, the only available option in the IMEC 400nm+ platform is based on thermo-optic effect using micro-heaters on top of the waveguides.

#### 2.2.2.1 Ring Resonator Based Filters

In this section, we discuss the ring resonator, a well-known fundamental component in photonic integrated circuits (PICs). Ring resonators are crucial in PICs due to their ability to confine light in a small volume and store it for thousand or even millions of round trips [35]. This unique property makes them ideal for various applications, including optical filters, modulators, frequency converters, and frequency comb generators [36]. Their compact size supports high device density and seamless integration with other optical components, enabling the development of complex and multifunctional photonic systems [35]. For a comprehensive review of ring resonators, please refer to reference [37].

This work focuses on the add-drop configuration of a ring resonator, which

serves as a filter for the laser cavity. This setup comprises a ring waveguide and two bus waveguides, as illustrated in 2.26.

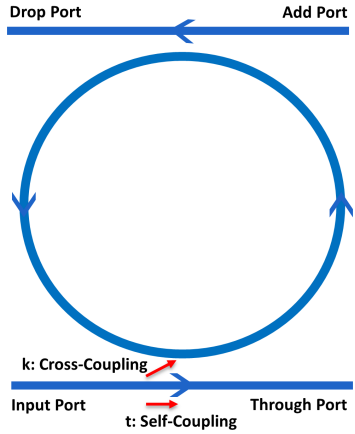



*Figure 2.26: Schematic of an add-drop ring resonator with two bus waveguides and a ring waveguide.*

In an add-drop ring resonator, light enters the input port of the lower bus waveguide. A portion of this light couples into the ring waveguide via a directional coupler. Only the light that satisfies the resonance condition of the ring, where the total roundtrip phase is an integer multiple of $2\pi$ is coupled to the other bus waveguide and directed to the drop port. The remaining light passes through to the through port. Fig. 2.27 shows a basic simulation of light transmission to the drop and through ports for a ring with a 25 $\mu$m radius and a group index of 3.82 (See 2.2). For reference, here are some key parameters of ring resonators along with their corresponding formulas. For a detailed review, refer to [37] and section 2.2.1 in [28].

- Free Spectral Range (FSR): The wavelength spacing between consecutive resonances.

$$\text{FSR} = \frac{\lambda^2}{n_g \cdot L_r} \tag{2.1}$$

  where $\lambda$ is the wavelength, $n_g$ is the group index, and $L_r$ is the circumference of the ring.

- Quality Factor (Q-factor): A measure of the resonator's efficiency in terms of energy loss. The Q-factor is defined as the sharpness of the resonance relative to its central frequency [37], indicating the stored energy divided by the power lost per optical cycle [28]. The losses due to the coupling to the bus waveguides are included in the so-called loaded Q-factor, while the

intrinsic or unloaded Q-factor refers to the state when the ring is not coupled to the bus waveguides.

$$Q = \frac{\lambda}{\Delta\lambda} \tag{2.2}$$

where $\Delta\lambda$ is the full width at half maximum (FWHM) of the resonance.

- Finesse (F): The ratio of the FSR to the linewidth of the resonance [37], representing the number of roundtrips before the light energy is reduced to $1/e$ of the initial energy [28].

$$F = \frac{\text{FSR}}{\Delta\lambda} \tag{2.3}$$

- Effective Length at Resonance: The optical path length of the resonator at resonance.

$$L_{r,\text{eff}} = \left(\frac{1}{2} + \frac{1-\kappa^2}{\kappa^2}\right) L_r \tag{2.4}$$

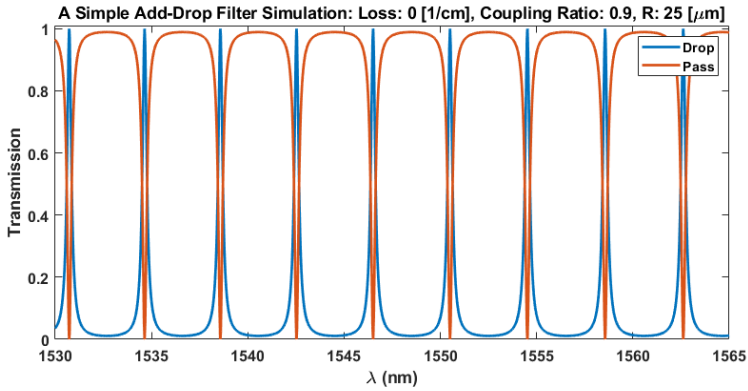



*Figure 2.27: Transmission to the through port and drop port of an add-drop ring resonator, as a function of wavelength.*

Considering a ring resonator-based filter as a reflective mirror in the laser cavity, with a 25 $\mu$m radius, the drop port transmission spectrum in Fig. 2.27 indicates an FSR of about 4 nm. Typically, a semiconductor optical amplifier (SOA) provides gain over a large bandwidth of about 50 nm (up to 100 nm). The FSR of the ring thus limits the laser's tunability to the same range. Reducing the ring length (and hence its radius) to increase the FSR is theoretically possible. However, to achieve an FSR of about 30 nm, 40 nm, and 100 nm, the ring radius would need to be reduced to approximately 3.34 $\mu$m, 2.5 $\mu$m, and 1 $\mu$m, respectively. This is practically unfeasible due to fabrication constraints and bend losses. The Si-400 nm platform design rules, and as a result the same for the IMEC 400nm+ platform,

discourage bend radii below 20 $\mu$m due to high loss. Therefore, a minimum radius of 25 $\mu$m is maintained.

A well-known approach to increase the filter FSR, without reducing the size of the ring resonator, is to use two ring resonators with slightly different ring radii in series, in a Vernier configuration. The effective FSR of such a Vernier filter, can be calculated using the following formula.

$$\mathrm{FSR}_{\mathrm{Vernier}} = \frac{\mathrm{FSR}_1 \cdot \mathrm{FSR}_2}{|\mathrm{FSR}_1 - \mathrm{FSR}_2|} \tag{2.5}$$

By setting $R_1 = 25$ $\mu$m and $R_2 = 27$ $\mu$m, an combined FSR of about 48 nm can be achieved (as shown in Fig. 2.28), providing a laser tuning range of about 48 nm. This is sufficient to cover the C-band (35 nm bandwidth) or partially the L-band (60 nm bandwidth). In the following section, we will explore methods to achieve a narrow-linewidth laser and further enhance its tunability range.

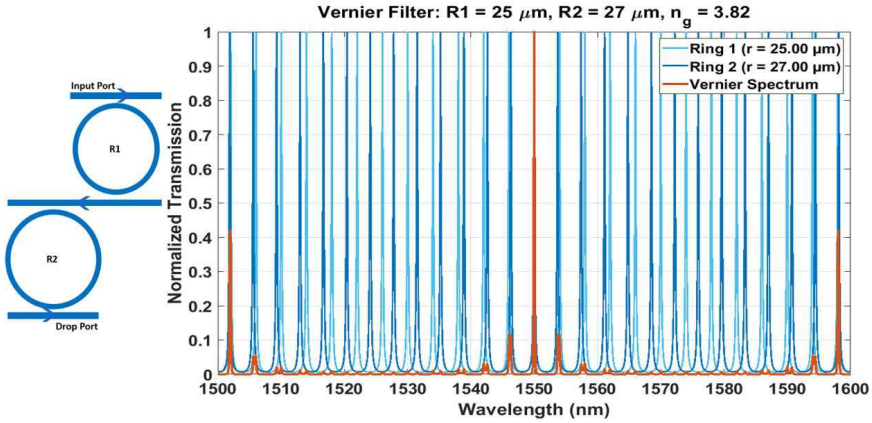



*Figure 2.28: Vernier filter schematic (left), Transmission to the drop port of the vernier filter, as a function of wavelength.*

#### 2.2.2.2 Theory of Laser Linewidth

In this section, we first introduce the basics of frequency noise, noise sources, and spectral line shape. We then review in summary methods to reduce quantum noise in extended cavity semiconductor lasers.

**Basics of Frequency Noise and Spectral Linewidth:** The linewidth of a laser is a complex output property, not fully described by a single number. Instead, the residual frequency instability of lasers is best characterized by the power spectral density (PSD) of frequency noise, which quantifies frequency deviations from the

average versus the timescale (Fourier frequency) at which they occur. This metric helps discriminate the main physical processes contributing to frequency noise at various timescales [28].

The laser optical field power spectral density, or laser "spectral line shape," can be derived from the laser frequency noise by integrating over the full range of Fourier frequencies [38–40], as shown in Eq. (2.6). Here, $\nu_0$ is the laser's center optical frequency, $S_E(\nu)$ is the optical PSD at optical frequency $\nu$, $E_0$ is the constant amplitude of the optical field, and $S_\nu(f)$ is the frequency noise PSD at Fourier frequency $f$:

$$S_E(\nu) = E_0^2 \int_0^\infty \cos[2\pi(\nu - \nu_0)\tau] \exp\left[-4 \int_0^\infty S_\nu(f) \frac{\sin^2(\pi f \tau)}{f^2}\, df\right] d\tau \tag{2.6}$$

Although Eq. 2.6 is not analytically solvable in general, it is shown that low-frequency noise primarily determines the typical spectral shape of a laser, while high-frequency noise contributes to the wings or tails [38, 41]. Therefore, the laser spectral profile can be approximated as a combination of a Gaussian shape near the center and a Lorentzian shape near the tails, forming a Voight profile [38, 40], shown in Fig. 2.29.

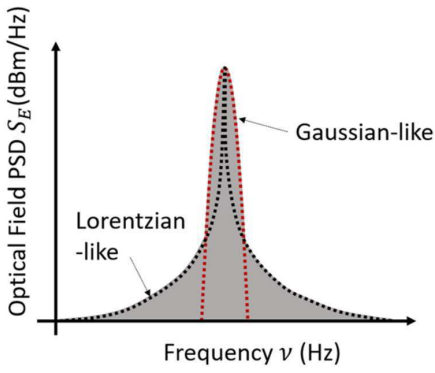



*Figure 2.29: The spectral line shape of the laser optical field exhibits a Gaussian-like profile near the peak and transitions to a Lorentzian-like profile at the tails. Axes are presented in logarithmic scale. Representation from [38].*

**Noise Sources in Semiconductor Lasers:** As shown in Fig. 2.30, the frequency noise spectrum of a free-running semiconductor diode laser typically features distinct frequency ranges with different characteristics [38]:

- Lower Frequency Range: The strongest noise occurs at long observation times (low Fourier frequencies), termed technical noise, dominated by vari-

ous $1/f^{\alpha}$ noises (with $\alpha > 0$). These include instabilities in the diode pump current, temperature variations, and acoustic perturbations [28]. External technical noises also meddle in this range. The resulting laser line shape due to $1/f^{\alpha}$ noise can be approximated as a Gaussian by integrating the noise above the so-called $\beta$-separation line [28, 41]. The integrated linewidth, defined as the full-width-half-maximum (FWHM) of the optical field PSD profile, is crucial in spectrometry, metrology, or sensing [38]. Reducing this noise requires stable laser resonators and active stabilization against a natural reference, such as a molecular transition [28].

- Higher Frequency Range: At short timescales, where $1/f$ noises and other technical noises die out, laser frequency fluctuations align with the quantum noise. This noise has a constant value at high frequencies, known as white noise, caused by spontaneous emission and carrier fluctuations [38]. The corresponding line shape can be approximated as a Lorentzian (shown in Fig. 2.29), with the linewidth given by $\pi S_0^{\nu}$, representing the minimum achievable linewidth when subjected solely to white quantum-noise processes. This Lorentzian linewidth is also referred to as fundamental linewidth, intrinsic linewidth, or instantaneous linewidth, widely known as the Schawlow-Townes linewidth, as its theoretical formula was first given by Schawlow and Townes in their well-known paper [42]. Reducing quantum noise requires controlling the ratio of spontaneous to stimulated emission, which cannot be achieved by active noise control methods due to bandwidth limitations of photodetection, electronics, and delay in servo loops [28, 38]. In high-speed applications, such as data communications, high-frequency noise characteristics are critical as they affect phase-error variance in coherent communication links [43, 44].

**Linewidth Reduction Strategies:** In semiconductor lasers, the Lorentzian linewidth is fundamentally determined by spontaneous emission noise and how efficiently it perturbs the phase of the optical field. As discussed in the previous subsection, this linewidth can be reduced by increasing the photon lifetime or decreasing the interaction of the optical field with the noisy active region. In the context of external cavity laser (ECL) designs, Tran et al. [38] identify four key strategies that directly contribute to significant linewidth narrowing:

- Reduction of Optical Loss in the Passive Region: Lowering the propagation loss in the passive waveguide section increases the photon lifetime and reduces the cavity losses. A higher photon lifetime leads to reduced phase noise, and therefore a narrower laser linewidth. Platforms such as SiN or optimized SOI can achieve low-loss guiding, and integrating them in the cavity design is a key enabler for linewidth reduction.

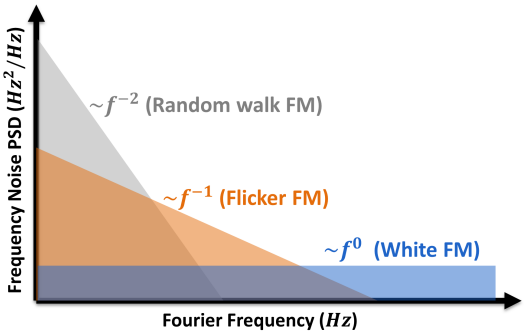



*Figure 2.30: A schematic illustration of the power spectral density (PSD) of frequency noise as a function of Fourier frequency, highlighting the various noise contributions typically present in hybrid-integrated diode lasers, each indicated with different colors [28, 38].*

- Increase in Mode Volume Ratio (Passive to Active): By designing the cavity such that a larger fraction of the optical mode resides in the low-loss passive section compared to the noisy gain region, one reduces the spontaneous emission noise affecting the lasing mode. This passive-to-active mode volume ratio directly impacts the Schawlow-Townes linewidth. In our work, the external cavity formed by low-loss microring filters and passive waveguides enables this spatial decoupling, effectively reducing linewidth, enabled by $\mu$TP integration method.

- Increase in Cavity Length: A longer cavity increases the photon round-trip time, which directly improves the effective quality factor (Q) and lowers the linewidth. This is especially true in extended cavities where the passive waveguides significantly increase the cavity length without introducing excessive loss. In our design, the extended cavity spans several hundred microns thanks to integrated microrings, Sagnac mirrors, phase shifters, and longer effective length due to the MRRs.

- Reduction of Out-Coupling Coefficient ($\kappa^2$): Lowering the coupling coefficient between the laser cavity and the output (i.e., reducing mirror outcoupling losses) increases the external quality factor, which narrows the linewidth. However, this must be balanced against differential quantum efficiency as too low a $\kappa^2$ will reduce output power. In our design, a tunable Sagnac loop mirror moderates $\kappa^2$ to balance linewidth reduction and power extraction.

In this thesis, the laser structure leverages all four principles by incorporating pre-fabricated SOA on an SOI external cavity with MRRs in a Vernier configuration: (1) low-loss Si waveguides as passive sections, (2) external cavity design

that extends the mode beyond the active SOA region, (3) increased cavity length through microrings and waveguides, and (4) optimized coupling strength via tunable Sagnac loop mirror. These design choices collectively enable Lorentzian linewidths below 500 kHz, meeting the OIF 400G-ZR requirement, while retaining sufficient optical power for practical applications.

#### 2.2.2.3 Design of Laser's Filter and Passives

To realize an external-cavity laser (ECL) that combines ultra-wide tunability with narrow linewidth, three essential components were integrated: a Vernier-based MRR filter for wavelength selection, a tunable Sagnac loop mirror for cavity feedback, and pre-fabricated III–V SOAs as the optical gain medium as schematically shown in Fig. 2.31. This section describes how these elements were co-designed and integrated on the IMEC 400nm+ platform using $\mu$TP, along with the rationale for the key design parameters that enable optimized linewidth and wavelength tunability.

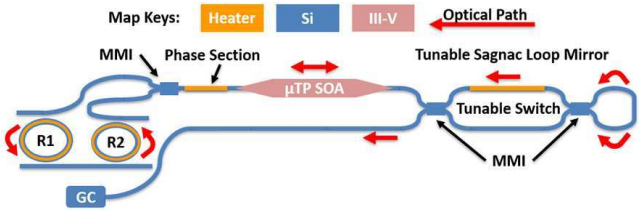



*Figure 2.31: A schematic layout of the external cavity design of the widely tunable narrow-linewidth III-V-on-Si laser.*

Two sets of Vernier filters were implemented, targeted respectively for the C- and L-band, comprising ring pairs with radii of 25 $\mu$m & 27 $\mu$m and 27 $\mu$m & 29.3 $\mu$m. These combinations yield Vernier FSRs of approximately 49.6 nm (with individual ring FSRs of 3.87 nm and 3.59 nm) for the C-band and 45nm (FSRs of 3.83 nm and 3.53 nm) for the L-band. These Vernier FSRs comfortably cover the expected GBW of the SOAs in both spectral bands, ensuring full wavelength coverage for tuning.

A major design objective, in addition to wide tunability, was the suppression of Lorentzian linewidth to meet stringent requirements from standards such as OIF 400G-ZR, which specify a laser linewidth below 500 kHz. Given that typical Fabry–Pérot-type semiconductor lasers exhibit intrinsic linewidths on the order of few MHz [38, 45], this implies a required linewidth reduction factor (LRF) of approximately 10–100.

This reduction is enabled by the extended external cavity formed with high-Q and low-loss MRRs, which enhances the photon lifetime and provides narrow band optical feedback. The relationship between the Q-factor of the passive cavity

and the achievable laser linewidth is derived from a modified Schawlow–Townes model, where the Lorentzian linewidth is inversely proportional to the loaded Q-factor [38]:

$$\Delta\nu \propto \frac{1}{Q} \tag{2.7}$$

If we consider the Q-factor of the entire laser cavity as a combination of the solitary cavity (SOA and mirrors) and extended cavity (Vernier filter), then in the case where the Vernier filter employs sufficiently high-quality factor rings, its Q-factor becomes dominant. In other words, the total Q-factor of the cavity can be approximated as $Q_{total} \approx Q_{Vernier}$. Under this condition, the linewidth reduction factor (LRF) can be defined as:

$$\text{LRF} = \frac{\Delta\nu_{\text{solitary cavity}}}{\Delta\nu_{\text{Vernier}}} \approx \frac{Q_{\text{Vernier}}}{Q_{\text{solitary cavity}}} \tag{2.8}$$

, where $Q_{\text{solitary cavity}}$ represents the effective Q-factor of the solitary SOA cavity, typically estimated around 500-1000.

Based on measured ring resonator data from fabricated test structures, we compiled the Q-factors and insertion losses (IL) for various coupling gaps, and ring radii, summarized below in Table 2.3, and Table 2.4

| **Radius ($\mu$m)** | **Gap ($\mu$m)** | **IL (dB)** | **Q-factor** |
|---|---|---|---|
| 25 | 0.2 | 0.40 | 6182 |
| 25 | 0.3 | 1.00 | 11908 |
| 25 | 0.4 | 1.28 | 22229 |
| 27 | 0.2 | 1.29 | 7761 |
| 27 | 0.3 | 1.67 | 13424 |
| 27 | 0.4 | 2.92 | 25931 |

*Table 2.3: C-band microring resonator parameters.*

| **Radius ($\mu$m)** | **Gap ($\mu$m)** | **IL (dB)** | **Q-factor** |
|---|---|---|---|
| 27 | 0.2 | 0.25 | 8048 |
| 27 | 0.3 | 0.50 | 14633 |
| 27 | 0.4 | 1.00 | 31953 |
| 29.3 | 0.2 | 0.614 | 8888 |
| 29.3 | 0.3 | 1.77 | 16646 |
| 29.3 | 0.4 | 1.93 | 34041 |

*Table 2.4: L-band microring resonator parameters.*

Since the Vernier resonance arises from the multiplicative overlap of the resonance profiles of the two constituent rings, it results in a sharper transmission peak

compared to the individual rings, when their resonances are well-aligned. This leads to a narrower linewidth and consequently a higher Q-factor. Therefore, as an estimation method, the higher Q-factor for each gap setting is taken as the effective Vernier Q-factor, which is then used to calculate the corresponding linewidth reduction factors (LRFs), as presented in Table 2.5.

| Wavelength Band | Gap ($\mu$m) | Estimated Vernier Q-Factor | Estimated LRF (Q/1000) |
|---|---|---|---|
| C-band | 0.2 | 7761 | 7.76× |
| | 0.3 | 13424 | 13.42× |
| | 0.4 | 25931 | 25.93× |
| L-band | 0.2 | 8888 | 8.88× |
| | 0.3 | 16646 | 16.64× |
| | 0.4 | 34041 | 34.04× |

*Table 2.5: Relationship between the gap of the constituent rings and the estimated Vernier Q-factor and Vernier Linewidth Reduction Factor (LRF) for C-band and L-band.*

While a larger coupling gap (e.g., 0.4 $\mu$m) typically results in higher Q-factors and thus more effective linewidth suppression, it also introduces greater insertion loss, meaning more optical power is dissipated as light circulates within the ring. In contrast, smaller gaps enhance coupling efficiency, resulting in lower optical loss. This reduced loss can potentially improve wavelength tunability, as more resonance modes may reach a condition where the laser gain exceeds the cavity loss. However, stronger coupling can compromise the filter's ability to isolate a single cavity mode, as noted in [38]. Additionally, high-Q rings are more susceptible to nonlinear optical losses, such as two-photon absorption. To balance linewidth narrowing, insertion loss, and mode selectivity, our design employs microrings with loaded Q-factors in the range of 10000 to 25000.

After evaluating the performance trade-offs, a 300 nm ring gap was selected as the optimal configuration. This setting offers a balanced Q-factor in the range of approximately 13000 to 16000, with an associated insertion loss between 0.5 and 1.77 dB. Based on the previously discussed relationship, this corresponds to an estimated LRF of 13–16×, potentially reducing the intrinsic linewidth to well below 500 kHz. This is significant, considering that typical solitary lasers exhibit Lorentzian linewidths on the order of a few megahertz [38, 45].

### 2.2.3 Design of Ultra-Wide Tunable Narrow-Linewidth Laser

Achieving both ultra-wide tunability and narrow linewidth in a laser involves inherent design trade-offs. Vernier-based filtering structures are commonly employed to extend the wavelength tuning range by exploiting the spectral mismatch between two microring resonators. To further increase the wavelength tuning range, an unbalanced MZI (with doubled FSR of the Vernier) can be added in series with the Vernier structure. This effectively eliminates every other one of the

Vernier resonances, as illustrated in Fig. 2.32, allowing a doubling of the filter's FSR. However, such configurations assume the gain medium offers a sufficiently wide gain bandwidth (GBW) to support the entire tuning range, a condition that is not always met in practical devices.

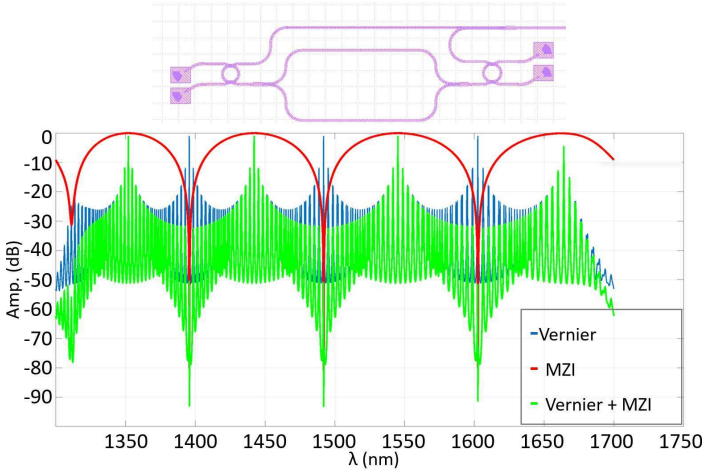



*Figure 2.32: An MZI added in series to a Vernier filter to double the total FSR. In this configuration, the arm's length difference of MZI needs to be chosen so the MZI's FSR be twice the Vernier's FSR.*

In our case, we will use the pre-fabricated SOAs provided by III-V Lab, aiming a GBW of approximately 50 nm, which constrains the achievable tuning range when using a single SOA. Although it is theoretically possible to design a custom SOA with extended GBW, this poses considerable challenges from the epitaxial processing perspectives. To overcome this limitation, we propose a practical and scalable solution that leverages the flexibility of $\mu$TP integration method. $\mu$TP enables heterogeneous integration of multiple SOAs, even those based on different source wafers and epitaxial compositions, onto the same substrate. This unique capability allows us to realize a dual-laser architecture, conceptually illustrated in Fig. 2.33, in which two distinct laser cavities, each with a dedicated SOA, are integrated to cover complementary spectral regions.

More specifically, the two laser cavities each incorporate SOAs with photoluminescence (PL) peaks centered at $\sim$1500 nm and $\sim$1550 nm, respectively. Each SOA supports a GBW of approximately 50 nm, enabling a combined spectral coverage of about 100 nm. As a result, one cavity covers the range from 1500–1550 nm, while the other spans 1550–1600 nm, with partial overlap at 1550 nm to ensure seamless and continuous tunability across the full range. The outputs of both cavities are combined using an 1x2 MMI combiner, followed by a grating coupler. While this introduces an additional insertion loss of $>$3 dB, future implementa-

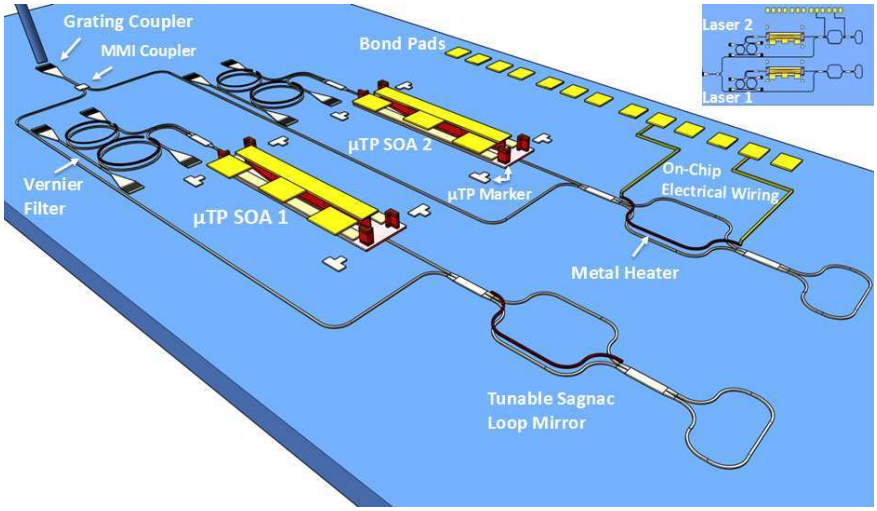



*Figure 2.33: 3D schematic layout of the dual-laser configuration. For simplicity, just one pair of electrical connections to a heater is shown.*

tions may replace the MMI with a switch (as shown in Section 2.5.2, Fig. 2.61), trading footprint for higher optical coupling efficiency.

To achieve narrow linewidth, wide tunability, and output power as high as possible, we implemented a sweep on the ring-to-bus coupling gap, with the values of 200 nm and 300 nm to find out the best practical balance, keeping the 300 nm as the main target. This design choice allows us to explore the trade-off between the quality factor and insertion loss of the microring resonators. These parameter variations were included in the fabrication mask. The finalized dual-laser mask layout is shown in Fig. 2.34. This structure forms the foundation for the fabrication and $\mu$TP integration processes, which are discussed in the next section.

## 2.3 Fabrication

In this section, we will explore the fabrication and integration steps of ultra-wide tunable narrow-linewidth III-V-on-Si lasers, focusing on the integration of pre-fabricated SOAs on IMEC 400nm+ platform using the $\mu$TP method. This section is divided into the following subsections: SOI Fabrication (IMEC 400nm+ platform) to provide the photonics circuit of the laser, SOA Fabrication and preparation for integration as the gain medium of the laser, and Integration and Post-Processing of the SOAs on the SiPh circuit.

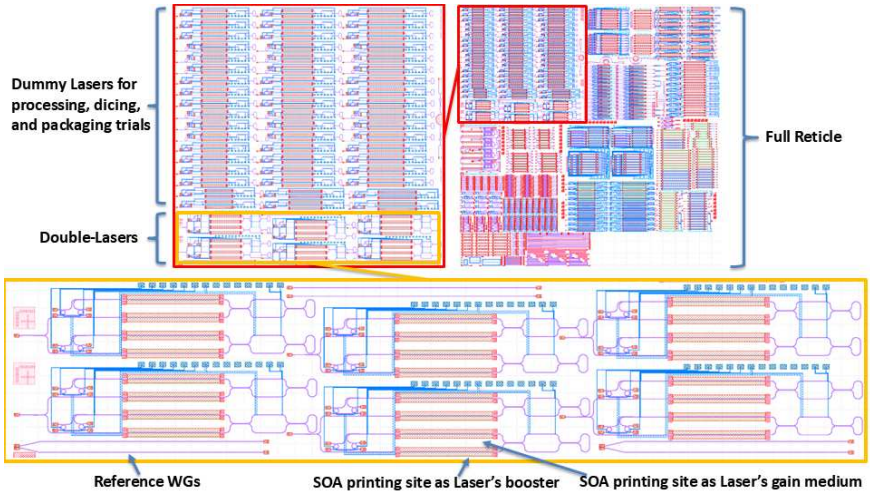



*Figure 2.34: Dual-Laser GDS Mask.*

### 2.3.1 SOI Fabrication

The SOI process is based on IMEC 400nm+ SiPh platform (see Chapter 1, Section 1.3.2). In this section, we first provide a brief overview of the overall process and then focus on the SOI preparation steps required before $\mu$TP integration.

The SOI fabrication process begins with an SOI wafer that has a 400 nm crystalline silicon device layer on a 2 $\mu$m thick buried Oxide (BOX) layer. Waveguide circuits are created using 193 nm Deep Ultra Violet (Deep-UV) lithography and a partial 180 nm etch step via dry etching.

Next, a 2 $\mu$m cladding oxide layer is deposited by chemical vapor deposition (CVD) and planarized using chemical mechanical polishing (CMP) process. An additional $\approx$2.5 $\mu$m Oxide layer on top of the cladding hosts the metal heaters, electrical bond pads, and connecting vias through the Oxide, while acts as an electrical passivation layer as well. The final schematic cross-section of the IMEC 400nm+ is shown in Fig. 2.35, with the image of the fabricated SiPh 200 mm wafer in Fig. 2.36.

To prepare the SOI for $\mu$TP integration, we need to etch back the cladding top Oxide ($\approx$2 $\mu$m) to expose the target waveguide. The cladding top oxide consists of a combination oxides. Therefore, the etch-back process must be performed carefully in two major steps. We first pattern the opening areas slightly larger than the SOA coupons (1080 $\mu$m $\times$ 100 $\mu$m) using photolithography to protect the rest of the circuit with a thick Ti-35E photoresist (PR) layer, as shown in Fig. 2.37. This creates a recess where the SOA will be integrated:

- Dry Etch using Reactive Ion Etching (RIE): By using $SF_6$-$CF_4$-$H_2$ in RIE


*Figure 2.35: Schematics of the IMEC 400nm+ SOI cross-section with the integrated metal layers and back-end stack.*

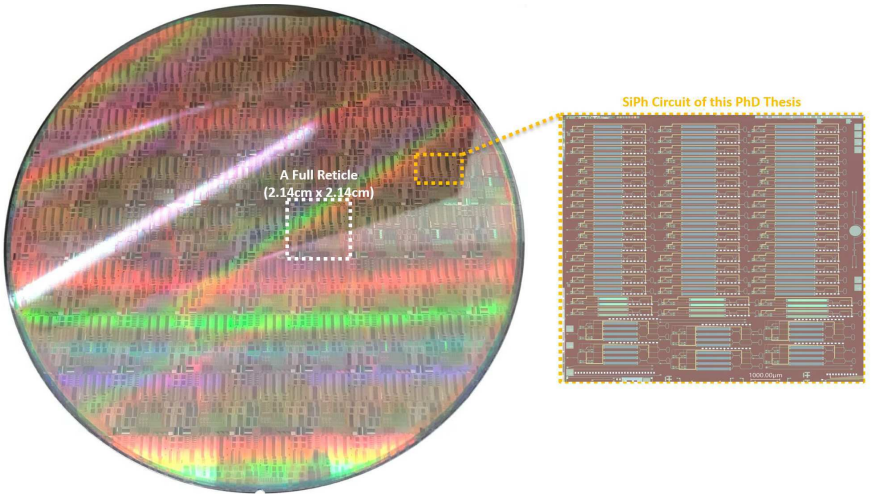



*Figure 2.36: Fabricated design on a 200 mm SiPh wafer based on the IMEC 400nm+ platform through an internal MPW run.*

for about 45 minutes, we stop slightly (≈120 nm) above the Si waveguide, as shown in the SEM image in Fig. 2.38. This is because the recipe also attacks Si (as shown in Fig. 2.39).

- Wet Etch using Buffered-HF (BHF): The etch-back process is completed by immersing the structures in BHF for about 1 minute (etch rate ≈120 nm/min), fully etching the Oxide layer and exposing the Si waveguides in the recess, as schematically shown in Fig. 2.40. In contrast to RIE, BHF offers very high selectivity over Si.

However, incorporating an etch-stop layer on top of the Si waveguide within the stack can be considered as a process modification to enable wafer-scale in-

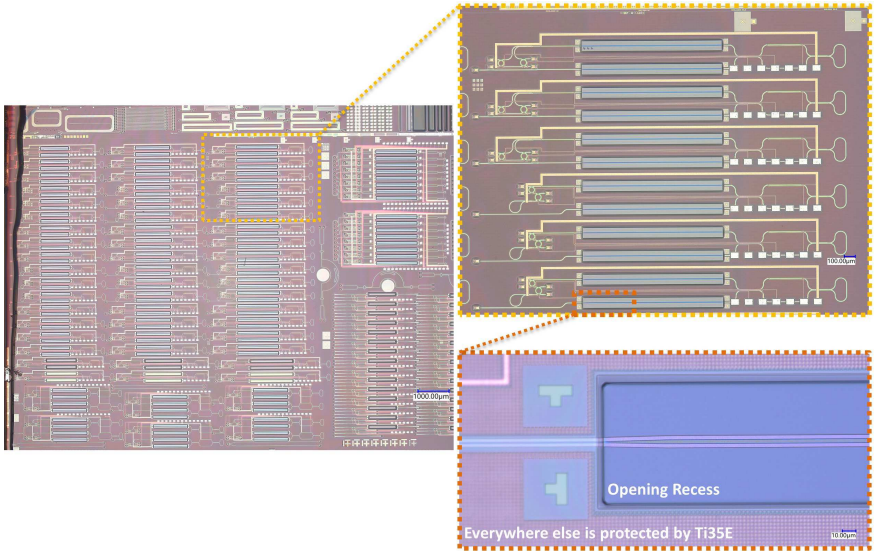



*Figure 2.37: Opening recess patterning by photolithography using Ti35E photoresist.*

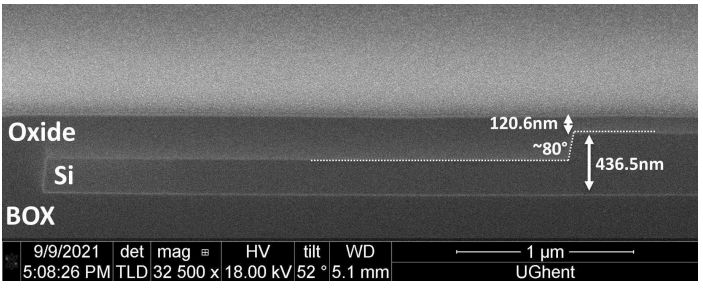



*Figure 2.38: Cross-sectional SEM image of the waveguide inside a recess after back-end etch-back by RIE.*

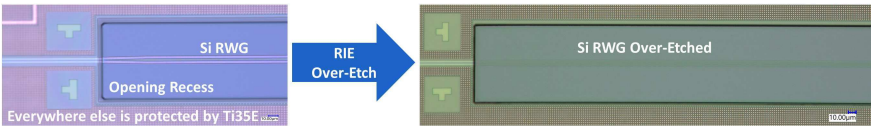



*Figure 2.39: Microscope image of the over-etched Si-waveguide inside a recess after back-end etch-back by RIE.*

tegration. This approach is already implemented in IMEC Passives+, iSiPP50G, and iSiPP200 platforms, where a recess can be defined in-line with the backend processing by using the poly-Si as an etch-stop layer, onto which the SOA can be printed.

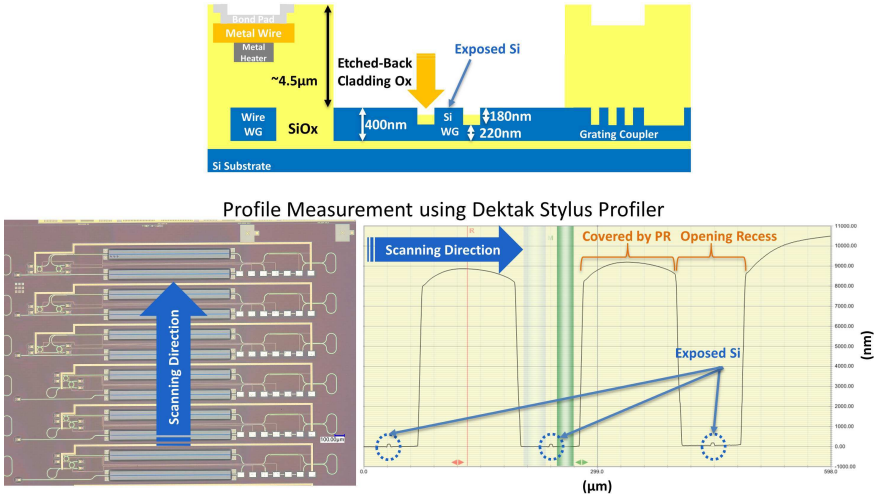



*Figure 2.40: Schematic cross-section overview after completion of back-end recess opening by BHF etching (top). Microscope image of the processed sample and its scanned profile (bottom), showing the Si-waveguide is exposed after BHF etching.*

Next, a thin DVS-BCB adhesive layer with a thickness of 100 nm is spray-coated to enhance the bonding strength between the III-V SOA and the underlying Si waveguide, followed by a short soft bake at 110 °C, shown in Fig. 2.41. During the spray-coating, DVS-BCB builds up at the edges of the recess, allowing the metallization in the final step to run over the sidewall of the recess, which is about 4.5 $\mu$m high.


*Figure 2.41: Schematic cross-section overview after BCB spray-coating over the recess.*

## 2.3.2 SOA Fabrication

The fabrication of the SOAs undertaken by III-V Lab, a private R&D organisation jointly established by Nokia, Thales and the CEA under the French "Economic Interest Grouping" (GIE) status [46, 47], begins with two InP wafers. The epitaxial

| Layer | Layer type | Material | Thickness [nm] | Doping level $[cm^{-3}]$ | Dopant |
|---|---|---|---|---|---|
| 26 | Cap P | InP | 100 | $\approx 1 \times 10^{19}$ | Zn |
| 25 | Contact P | GaInAs (lattice matched) | 200 | $\overset{\approx}{2.5 \times 10^{19}}$ | Zn |
| 24 | Transition P | GaInAsP ($\lambda_g$ = 1170 nm) | 20 | $\approx 6 \times 10^{18}$ | Zn |
| 23 | Cladding P | InP | 1000 | $\overset{\approx}{1-2\times 10^{18}}$ | Zn |
| 22 | Cladding P | InP | 500 | $\approx 5 \times 10^{17}$ | Zn |
| 21 | Etch stop | GaInAsP ($\lambda_g$ = 1170 nm) | 25 | $\approx 5 \times 10^{17}$ | Zn |
| 20 | Transition | $(Al_{0.9}Ga_{0.1})_{0.47}In_{0.53}As$ | 25 | | |
| 19 | SCH | $(Al_{0.7}Ga_{0.3})_{0.47}In_{0.53}As$ | 25 | | |
| 8x6 | Barrier | $(Al_{0.45}Ga_{0.65})_{0.51}In_{0.49}As$ | 10 | | |
| 7x6 | Well | $(Al_{0.25-0.20}Ga_{0.75-0.80})_{0.3}In_{0.7}As$ | 6 | | |
| 6 | Barrier | $(Al_{0.45}Ga_{0.65})_{0.51}In_{0.49}As$ | 10 | | |
| 5 | SCH | $(Al_{0.7}Ga_{0.3})_{0.47}In_{0.53}As$ | 25 | | |
| 4 | Transition | $(Al_{0.9}Ga_{0.1})_{0.47}In_{0.53}As$ | 25 | $1 \times 10^{18}$ | Si |
| 3 | Contact N | InP | 200 | $2 \times 10^{18}$ | Si |
| 2 | Sacrificial | GaInAs (lattice matched) | 50 | nid | |
| 1 | Sacrificial | AlInAs (lattice matched) | 500 | $\approx 1 \times 10^{18}$ | Si |
| 0 | Buffer layer | InP | 150 | nid | |

*Table 2.6: III-V SOA epitaxial layer stacks, with MQW variants achieving photoluminescence peaks at 1500 nm and 1550 nm.*

layer structures, depicted in Fig. 2.43(a) and detailed in Table 2.6, are grown using metal-organic vapor-phase epitaxy (MOVPE). Two epitaxial structures are separately grown with only variants in multi-quantum wells (MQWs), designed to achieve laser emissions around 1525 nm and 1575 nm. Photoluminescence (PL) spectra and wafer map are reported for both the grown epitaxial structures by III-V Lab, as shown in Fig. 2.42.

Initially, a 100 nm InP sacrificial layer is removed through 1 HCl : 3 $H_3PO_4$ etching (Fig. 2.43(b)), followed by the deposition of a 300 nm thick silicon nitride (SiNx) layer via plasma-enhanced chemical vapor deposition (PECVD) at 250°C (Fig. 2.43(c)). This SiNx layer serves as a hard mask for the definition of the p-cladding mesa the adiabatic taper structure. It is patterned using electron beam (e-beam) lithography.

The p-GaInAs, p-GaInAsP, and p-InP layers are etched using inductively coupled plasma (ICP) etching, followed by an anisotropic p-InP etch using 1 HCl : 3

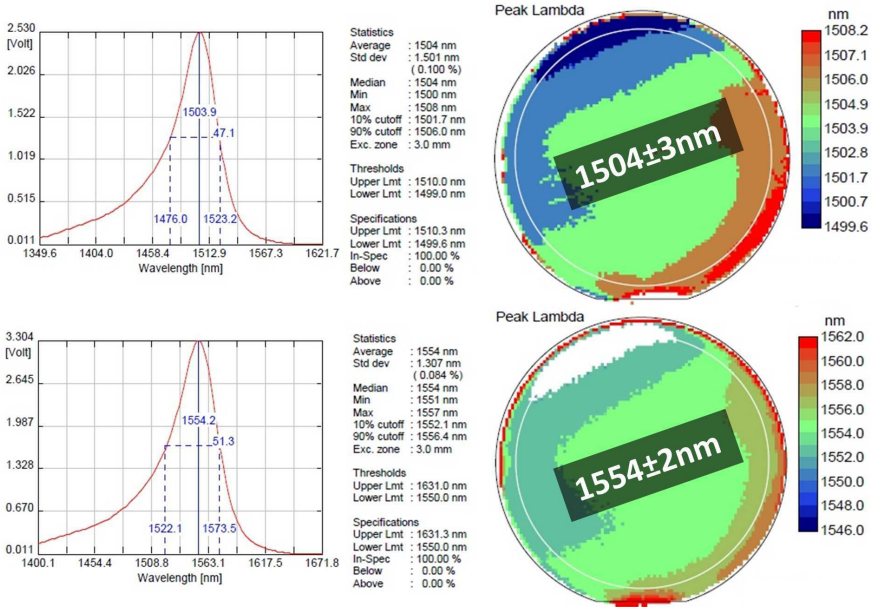



*Figure 2.42: Photoluminescence spectra and wafer map of the III-V SOA epitaxial layer stacks with MQW variants, achieving photoluminescence peaks at 1500 nm and 1550 nm, reported by III-V Lab.*

$H_3PO_4$ for three minutes to form negatively angled side walls on the mesa (Fig. 2.43(d)), resulting in a much narrower width at the bottom of the mesa. Another SiNx hard mask is then deposited to protect the side walls and is used for MQW patterning via ICP (Fig. 2.43(e)).

Ti/Pt/Au contacts are formed on both sides of the QW cross-section (left and right) on the n-InP through a lift-off process (Fig. 2.43(f)). Positioning n-contacts on both sides of the QW cross-section enhances the homogeneity of current injection and reduces the series resistance.

A new SiNx layer is deposited to protect the entire device and serves as a hard mask for defining the device island in the n-InP layer (Fig. 2.43(g)). Subsequently, the InGaAs and AlInAs layers are etched through, extending approximately 100 nm into the InP substrate (Fig. 2.43(h)). Tethers are then defined by SiNx deposition and RIE (Fig. 2.43(i)), which support the III-V coupons during and after the selective chemical etching of the release layer and act as anchors for the suspended device. The narrowest part of the tethers, designed to be located near the coupon (Fig. 2.44), will break during the micro-transfer printing process, while the wider part remains on the InP substrate.

As shown in Fig. 2.43(j), the entire device is encapsulated with a thick layer of DVS-BCB. This layer is then thinned to the top of the waveguides, and the SiNx

covering the top of the waveguide is etched before the p-contact is deposited via lift-off (Fig. 2.43(k)). Next, vias are etched in the DVS-BCB and SiNx to access the n-contacts, and a mesa is formed around the coupons to separate individual structures and provide access to the release layer (Fig. 2.43(l)).

Figure 2.44(a) shows a scanning electron microscope (SEM) image of a fabricated InP coupon before release etching. Prior to the release etching (Fig. 2.43(n)) using a $FeCl_3$ wet-etch, a thick layer of Ti35E photoresist is spin-coated and patterned by a contact photolithography step to encapsulate the devices and reinforce the tethers, as shown in Fig. 2.43(m) and Fig. 2.45 [23] (carried out in UGent cleanroom). Figure 2.44(b), shows a microscope top-view image of the fabricated coupons in the dense array with a vertical pitch of 70 $\mu$m as mentioned before in the Pre-fabricated micro-transfer-printing compatible SOA section (2.2.1.4).

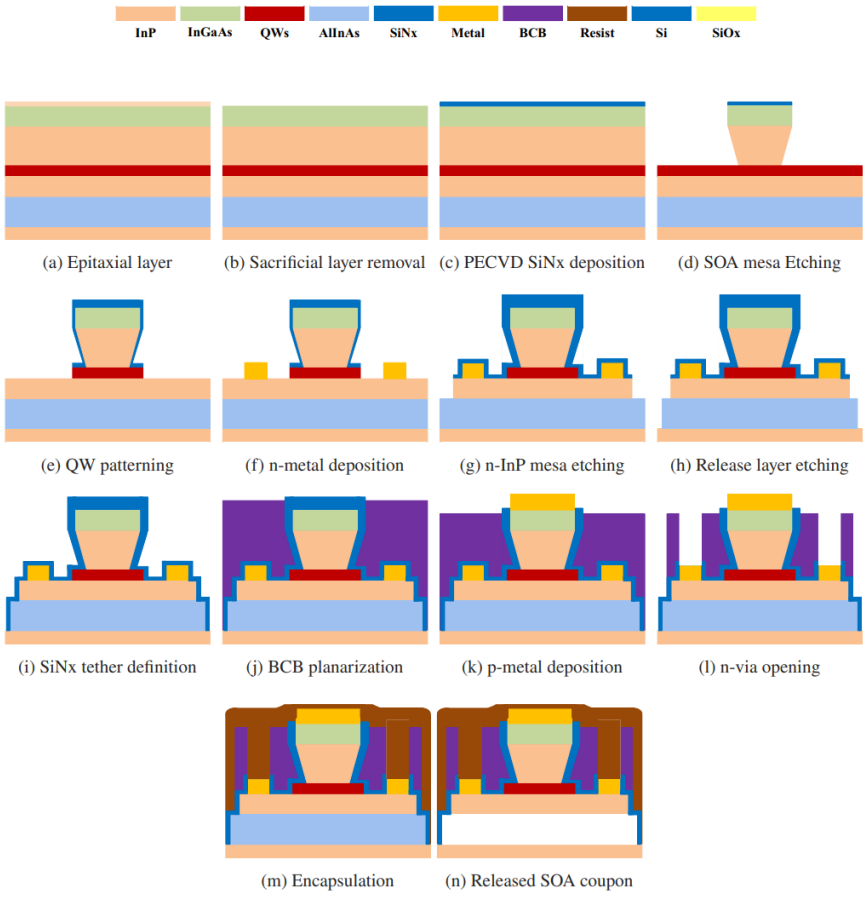



*Figure 2.43: Process flow of SOA device fabrication on the source InP substrate.*

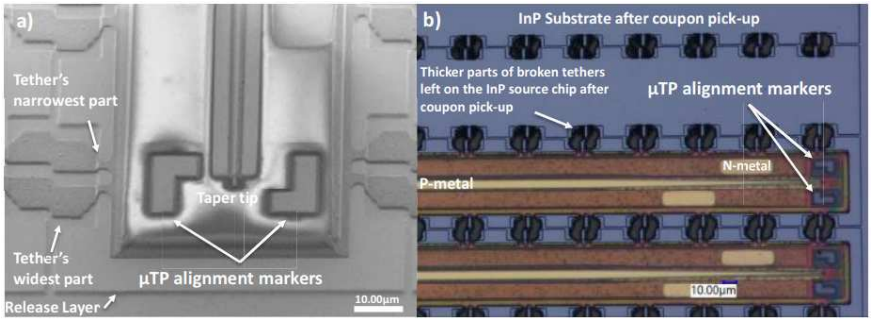



*Figure 2.44: A fabricated InP coupon source: a) Side-view SEM image, b) Top-view microscope image.*

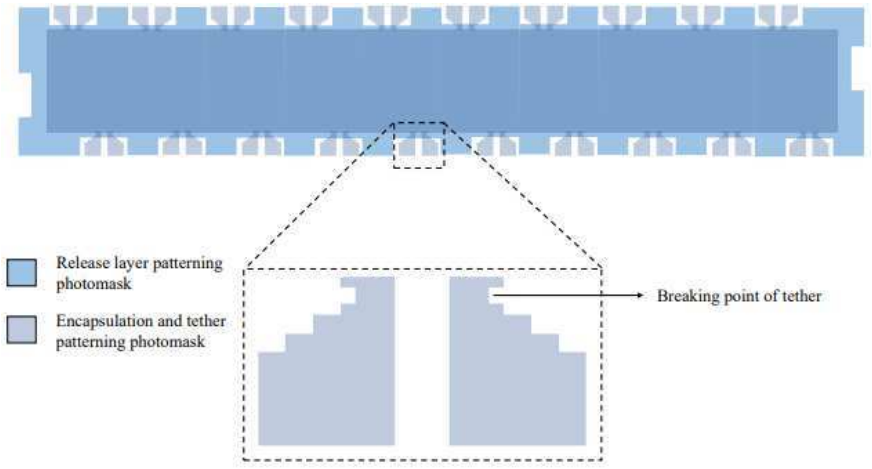


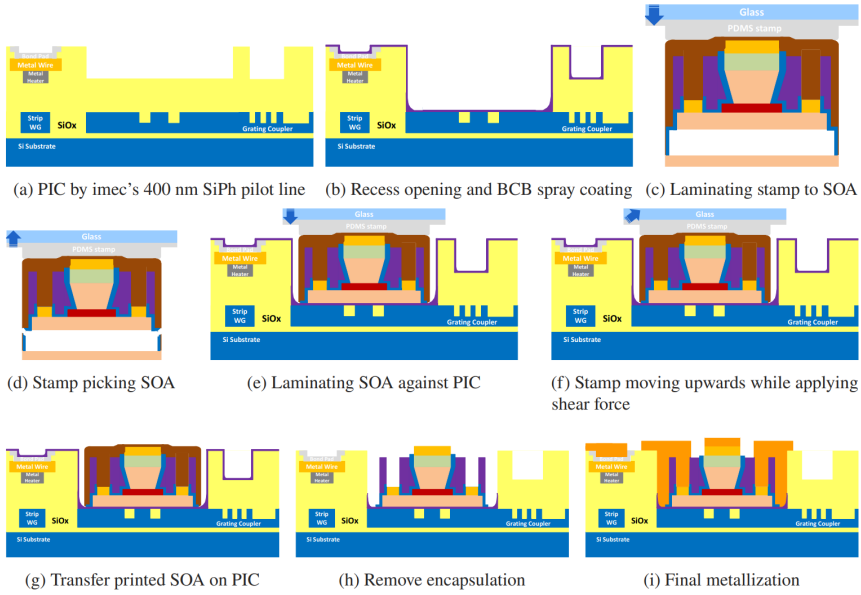

*Figure 2.45: Schematic presentation of the photomask used for patterning the release layer and encapsulating the device, along with a close-up view of the tether design [23].*

### 2.3.3 Integration and Post-Processing

Before micro-transfer printing, the spray-coated sample underwent a brief soft bake at 150°C to re-flow the DVS-BCB, ensuring a smooth printing process. The $\mu$TP of III-V SOAs was performed using an X-Celeprint $\mu$TP-100 lab-scale printer with a PDMS stamp featuring a post of $1150 \times 50$ $\mu$m² and a height of 50 $\mu$m, used for printing $1000 \times 47.5$ $\mu$m² SOA coupons. Although a single-post stamp was utilized in this experiment, array printing using a multi-post stamp is possible, which is beneficial for high-throughput integration, particularly at wafer scale, as outlined in the $\mu$TP method roadmap.

After preparing the target sample, both the SOA coupon source sample and the SOI target sample were loaded into the $\mu$TP tool. Proper angular alignment

is crucial for the long SOA devices. The printing process, illustrated in Fig. 4, begins with laminating the stamp to the released SOA coupon (Fig. 2.46(c)). The stamp then accelerates away from the coupon, breaking the tethers at the narrowest point on top of the release layer (Fig. 2.46(d)). After pickup, the COGNEX VisionPro software [23, 48] auto-aligns the coupon using pattern recognition on the alignment markers on both the SOA coupon and the target circuit (Fig. 2.47). Following auto-alignment, the stamp is laminated to the target SOI substrate (Fig. 2.46(e)). Upon contact, a shear force is applied in both the x and y directions to detach the SOA coupon from the stamp, which then slowly moves up, leaving the SOA coupon on the target site (Fig. 2.46(f)). A schematic cross-section of the transfer-printed SOA coupon on the SiPh circuit is shown in Fig. 2.46(g).




(a) PIC by imec's 400 nm SiPh pilot line (b) Recess opening and BCB spray coating (c) Laminating stamp to SOA

(d) Stamp picking SOA (e) Laminating SOA against PIC (f) Stamp moving upwards while applying shear force

(g) Transfer printed SOA on PIC (h) Remove encapsulation (i) Final metallization

*Figure 2.46: Process flow of PIC preparation for $\mu$TP, micro-transfer printing and post processing.*

The process continues with an oxygen-plasma etch using RIE to remove the PR encapsulation on the printed III-V SOAs and the spray-coated DVS-BCB on electrical bond pads (Fig. 2.46(h)). This is followed by fully curing BCB at 270°C for about 2 hours, with a gradual temperature profile taking about 6 hours in total. Post-printing processing concludes with electrically connecting the printed SOAs to the Al bond pads using 40 nm of Ti and 1 $\mu$m thick Au on top (Fig. 2.46(i)). Figure 2.47 shows a stitched microscope image of the fabricated lasers, featuring two transfer-printed SOAs and a combined output port for the two lasers via a 3-dB combiner (1x2 MMI ). The SOA in the first individual laser (laser 1) has a

gain peak around 1525 nm, while the SOA in the second individual laser (laser 2) has a gain peak around 1575 nm. This highlights the significant advantage of $\mu$TP over other heterogeneous integration methods, allowing for the close integration of multiple devices from different sources onto a common substrate.

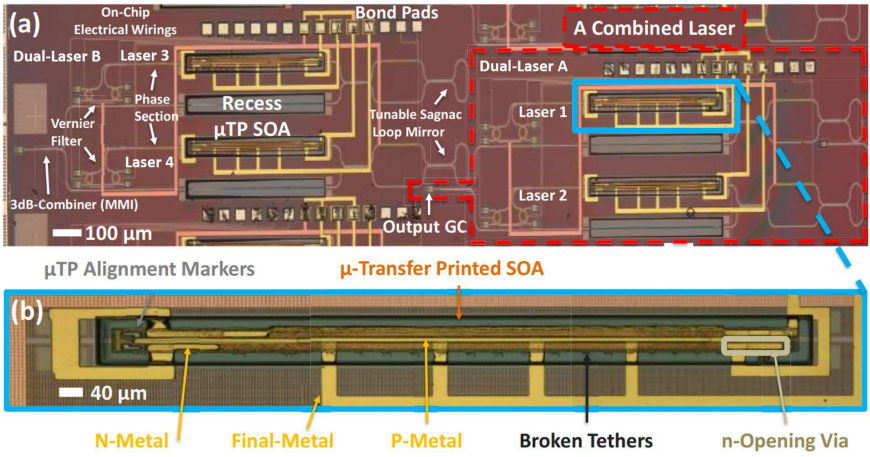



*Figure 2.47: (a) Stitched microscope image of the combined widely tunable lasers. (b) Micro-transfer-printed III-V amplifier in the recess (after final metallization).*

## 2.4 Characterization

This section presents the characterization results of the fabricated dual-laser structures. We first outline the general measurement setup and initial performance metrics, followed by a detailed analysis of the tunability behavior. Finally, we discuss the laser linewidth measurements, starting with a brief overview of conventional measurement methods and then presenting the results obtained from our devices. To characterize the lasers, the photonic chip was mounted on a temperature-controlled stage stabilized at 15 °C, as shown in Fig. 2.48. The laser output was coupled into a single-mode fiber (SMF), which was connected to a 10/90 optical splitter to feed an optical spectrum analyzer (OSA) and an optical power meter simultaneously. Multiple Keithley 2400 SourceMeters were used to bias the SOAs, while a Keysight E36300 Series triple-output power supply drove the thermal tuning elements, such as tunable microring resonators, phase shifters, and tunable reflectors, via DC probes. Reference waveguides with grating couplers, fabricated on the same die and processed identically to the laser cavities (see Fig. 2.34), were used to calibrate grating coupler losses and estimate the on-chip optical power at the output of the 3 dB combiner. The mask included two sets of dual-laser configurations: one with a ring-to-bus gap of 300 nm (labeled Dual-Laser A), and

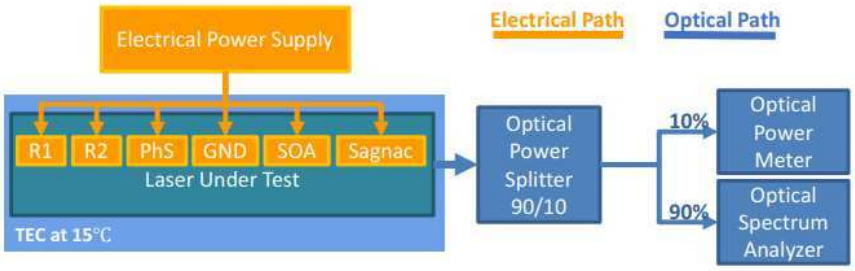



*Figure 2.48: Schematic layout of the laser characterization setup.*

another with a 200 nm gap (Dual-Laser B), designed for performance comparison. In Dual-Laser A, the two cavities are referred to as Laser 1 and Laser 2, while those in Dual-Laser B are denoted as Laser 3 and Laser 4. As all lasers on the chip underwent the same metallization process to form the electrical redistribution layer, the differential resistances of the integrated amplifiers are nearly identical. This is consistent with the fact that while the SOAs in each dual-laser structure are based on different epitaxial sources (with different QW layers), the p-InP cladding and n-InP contact, responsible for charge injection, are similar, resulting in comparable electrical characteristics. Under a drive current of 120 mA, Lasers 1 and 2 exhibited a differential series resistance of approximately 10Ω. A current sweep from 0 to 120 mA on either Laser 1 or Laser 2 (without activating any tuning elements) yielded threshold currents around 85 mA. However, when one of the microrings was thermally tuned, the lasing threshold dropped to 50 mA for Laser 1 and 60 mA for Laser 2, confirming that in external-cavity configurations, the laser threshold strongly depends not only on the SOA but also on feedback from cavity tuning elements.

### 2.4.1 Laser Tunability

The tunability of the lasers was investigated by thermally tuning the microring resonators and phase sections. Coarse wavelength tuning of each laser was achieved by tuning only one microring and the phase section, while fine tuning was realized by simultaneously adjusting both rings and the phase section. For Dual-Laser A (Lasers 1 and 2, ring gap = 300 nm), injecting 120 mA into each SOA resulted in a combined tuning range of 111 nm, as shown in Fig. 2.49. For Dual-Laser B (Lasers 3 and 4, ring gap = 200 nm), the combined tuning range extended to 121 nm, illustrated in Fig. 2.50. To the best of our knowledge, this represents the widest tuning range reported on a single silicon photonic chip.

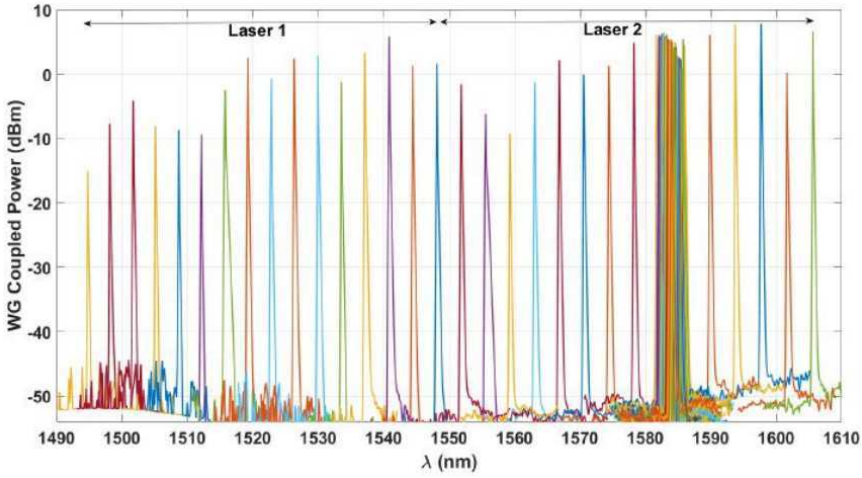



*Figure 2.49: Tuning spectrum of Dual-Laser A (300 nm ring gap). Fine tuning in steps of 100 pm was performed over a 4 nm range, equivalent to the FSR of one ring.*

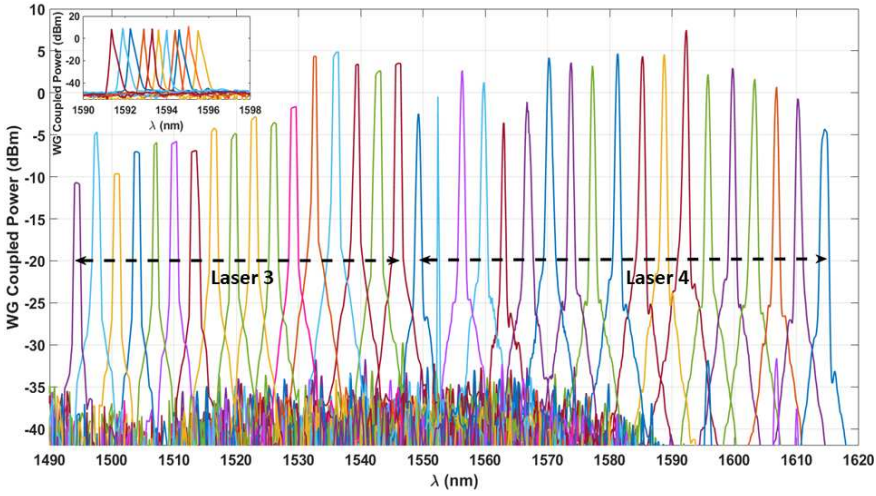



*Figure 2.50: Tuning spectrum of Dual-Laser B (200 nm ring gap). Fine tuning was done in 10 steps over a 4 nm range, matching the ring FSR.*

## 2.4.2 Linewidth characterization

In this section, we provide a summarized overview of narrow-linewidth measurement techniques, with a more detailed discussion available in [49]. Afterwards, we present the linewidth measurement results of the fabricated lasers.

#### 2.4.2.1 Narrow-linewidth measurement methods

The two main methods for measuring laser linewidth are:

- Direct calculation from the laser's power spectral density (PSD).
- Indirect estimation using the relationship between phase noise and linewidth

The PSD method is preferred due to its intuitive nature and ease of implementation and is therefore widely used in linewidth measurement experiments [49]. Optical beat notes are required to obtain the PSD. When two incoherent lasers, both with Lorentzian line shapes, are mixed, the resulting beat signal also exhibits a Lorentzian line shape. The PSD of these beat notes is given by [49, 50]:

$$s(v) = \frac{\Delta v}{2\pi \left[ (v - v_b)^2 + \left( \frac{\Delta v}{2} \right)^2 \right]} \tag{2.9}$$

In this formula (Eq. 2.9), $\Delta v$ represents the sum of the linewidths of the tested laser ($v_t$) and the reference laser ($v_r$), while $v_b$ is the frequency difference between the two lasers (also the center frequency of the beat notes). The beat signal arises from the interference of two lasers with closely matched frequencies, producing a lower-frequency beat. The linewidth of the beat signal is equal to the sum of the linewidths of the two lasers.

Two common scenarios arise when measuring linewidth through beat notes, as shown in Fig. 2.51. In the first scenario, if $v_t \approx v_r$, the linewidth of the beat notes is roughly twice that of the tested laser ($\Delta v \approx 2v_t$, case 1). In the second scenario, if $v_t \gg v_r$, where the reference laser has an exceptionally narrow linewidth compared to the tested laser, the beat signal's linewidth approximates that of the tested laser ($\Delta v \approx v_t$, case 2). These two cases are applied flexibly depending on the specific conditions of the lasers. In this section, we will examine four measurement configurations based on these scenarios.

**Beating with a Reference Laser** Figure 2.52 illustrates the setup where an additional laser generates a reference beam, which is then mixed with the tested laser. The photodetector (PD) captures the beat signal and sends it to an electrical spectrum analyzer (ESA). According to case 1, a reference laser with a similar linewidth as the tested laser is used, allowing measurement of any linewidth, though obtaining and calibrating such a reference laser can be challenging. In case 2, using a reference laser with an extremely narrow linewidth relative to the tested laser is sufficient for most measurements, although it may not be accurate for ultra-narrow linewidths. The lasers involved in the beat should have the similar amplitude, nearly identical optical frequencies, and the optical path should be stable [49, 51], which requires a stable experimental setup.

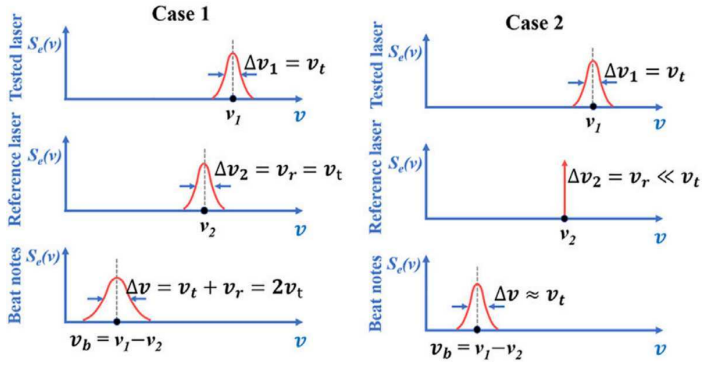



*Figure 2.51: Principle of optical beat notes [49].*

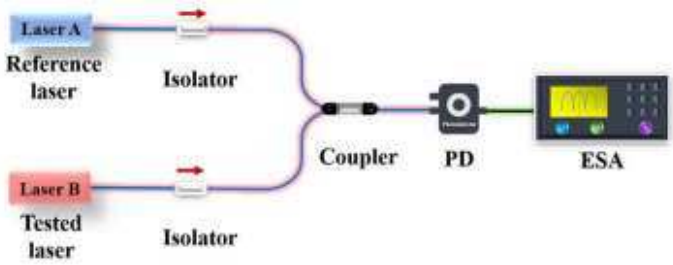



*Figure 2.52: Beat note with a reference laser [49].*

**Beating with a Delayed Version of the Laser Under Test (LUT)**

- Self-Homodyne Configuration: the delayed self-homodyne interferometer setup, shown in Fig. 2.53, follows the principle outlined in case 1. This configuration is based on an unbalanced Mach–Zehnder interferometer (UMZI) [49, 52]. It avoids the range limitations of other setups and offers a simple structure, broad measurement range, and low optical transmission loss [49]. However, since the center frequency $v_b$ of the beat notes is 0 Hz, the low-frequency environmental noise can affect measurement accuracy. Additionally, disturbances from environmental factors, such as temperature and pressure, may significantly impact the test results [49, 53, 54].

- Self-Heterodyne Configuration: Delayed self-heterodyne interferometry (DSHI) improves upon the self-homodyne setup by mitigating the effects of low-frequency noise. As shown in Fig. 2.54, an acousto-optic modulator (AOM) shifts the center frequency of the beat notes to a higher value, reducing system errors and enhancing measurement precision. However, for narrow-linewidth lasers, the delay time must significantly exceed the coherence

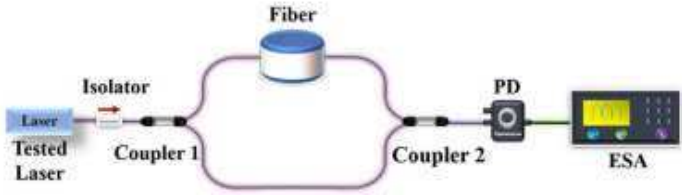



*Figure 2.53: Delayed self-homodyne detection [49].*

time [49]. For instance, testing a 100-Hz linewidth requires a fiber length of approximately 1,590 km [55]. Such long fibers increase experimental complexity, introduce attenuation, and contribute to 1/f noise, broadening the spectral line and introducing measurement errors [49, 56].

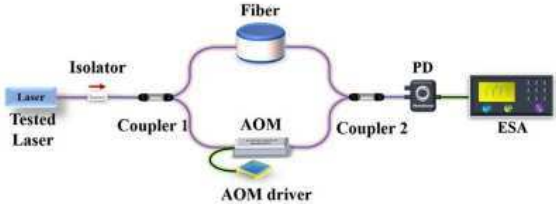



*Figure 2.54: Delayed self-heterodyne detection [49].*

In this PhD thesis, the laser linewidth measurements are conducted using the OE4000 HI-Q® LASER LINEWIDTH/PHASE NOISE ANALYZER from OEwaves [57], shown in Fig. 2.55. This analyzer is based on a self-homodyne configuration and uses a proprietary stabilized interferometer along with a unique optical signal extraction technique. Unlike traditional homodyne detection, it does not require complex modulation. Additionally, it incorporates a high-speed signal processing algorithm that avoids the typical offset frequency limitations and high-frequency instabilities of conventional methods. The OEwaves analyzer supports a wide wavelength range, broad power range, and flexible measurement capabilities [58–60].

#### 2.4.2.2 Linewidth measurement results of the fabricated lasers

Figure 2.56 shows the measured Lorentzian linewidth of Dual-Laser A (with a ring gap of 300 nm) across its tuning range biased at 120 mA, as characterized using the OEwaves OE4000 Optical Phase Noise Test System. While the linewidth

*Figure 2.55: OEwaves HI-Q® LASER LINEWIDTH/PHASE NOISE ANALYZER [57, 59].*

varies from approximately 13 kHz to 170 kHz over the tuning span, the frequency noise consistently remains below the threshold defined by the OIF 400G-ZR standard [61]. Figure 2.57 illustrates the frequency noise power spectral density (PSD) of Laser 1, operating at 1530 nm and biased at 120 mA. The corresponding Lorentzian linewidth derived from the PSD is approximately 20 kHz, confirming excellent coherence performance within the target range. For Dual-Laser B (ring gap = 200 nm), the measured Lorentzian linewidth spans from 50 kHz to 350 kHz across its tuning range, biased at 120 mA. While slightly broader linewidths are expected due to the lower quality factor (Q) of the filtering cavities, attributable to the reduced ring-to-bus gap, the linewidth values remain well below the OIF 400G-ZR compliance threshold, confirming suitability for advanced coherent communication and sensing applications.

### 2.4.3 Comparison with State-of-the-Art

This section compares the performance of the lasers developed in this work with state-of-the-art integrated laser technologies, focusing on tunability and intrinsic linewidth. Latkowski et al. demonstrated a monolithically integrated laser with a tuning range of approximately 74 nm and a linewidth of 360 kHz, delivering an output power of 3 mW [62]. Another monolithic design reported in [63] achieved a high side-mode suppression ratio (SMSR) of 54.5 dB, an output power of 19 dBm, and a linewidth of 80 kHz across 103 channels spanning the C-band (35 nm tunability). McKinzie et al. [64] presented a monolithic InP-based laser with linewidths between 30–50 kHz and an average output power exceeding 180 mW over the extended C-band ($\approx$55 nm tunability). Gao et al. demonstrated a hybrid-integrated III-V laser (based on InGaAsP multiple quantum wells) butt-coupled to a silicon photonic chip, achieving a record-high output power of 21.5 dBm across

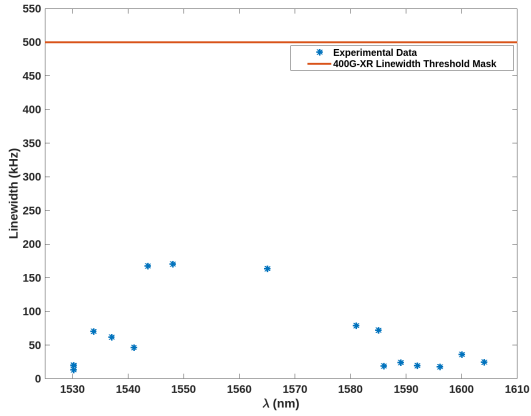



*Figure 2.56: Measured Lorentzian linewidth of the Dual-Laser A (ring gap = 300 nm) across its tuning range, obtained using the OEwaves OE4000 Optical Phase Noise Test System. All measured linewidths remain well below the 400G-ZR standard linewidth threshold mask (500 kHz), demonstrating the laser's suitability for advanced coherent applications.*

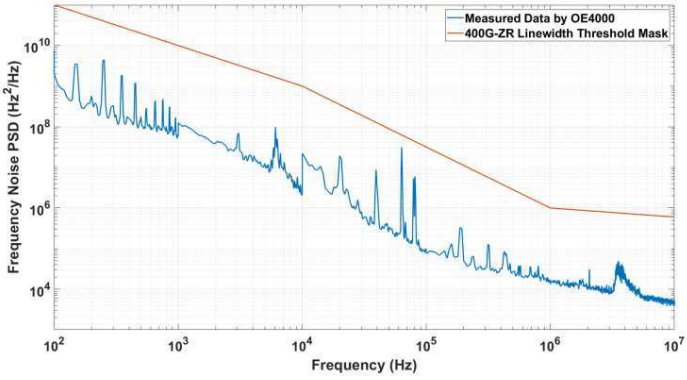



*Figure 2.57: Frequency noise power spectral density of Laser 1 (ring gap = 300 nm), measured using the OEwaves OE4000 Optical Phase Noise Test System. The laser was biased at 120 mA and operated at a wavelength of 1530 nm. The measured noise remains well below the 400G-ZR linewidth threshold mask, indicating suitability for coherent optical communication standards.*

a 65 nm tuning range in the C-band. This device also exhibited narrow linewidths down to 60 kHz and SMSR greater than 50 dB [65]. A heterogeneously integrated III-V-on-Si laser using wafer bonding was reported in [66], offering a 50 nm tuning range, 10 mW fiber-coupled output power, and a linewidth of 259 kHz. In a notable example, Tran et al. [38] demonstrated a heterogeneously integrated III-V-on-Si laser with a deep-etched silicon quad-ring cavity, achieving a 120 nm tuning range

(1485–1605 nm) and an ultra-narrow intrinsic linewidth of approximately 100 Hz. In comparison, the dual-laser designs presented in this work achieve tuning ranges of 111 nm and 121 nm for Dual-Laser A and B, respectively, with Lorentzian linewidths as low as 13 kHz and 50 kHz. These results offer a more relaxed and generic design approach, avoiding the need for complex deep-etched silicon structures like quad-ring cavities. As discussed, monolithic lasers typically offer higher optical output power, while hybrid designs tend to achieve narrower linewidths. Among all categories, heterogeneous integration, such as the approach used in this work, enables both ultra-narrow linewidths and wide tunability by optimizing extended cavities with low-loss silicon ring-based filters. Further linewidth reduction is possible by integrating III-V gain materials onto low-loss SiN platforms, as discussed in Section 2.5.3. However, heterogeneous lasers generally exhibit lower output power compared to monolithic or hybrid counterparts. This highlights the importance of integrating booster amplifiers, as discussed in Chapter 3, to enhance output power. Once addressed, heterogeneous integration offers the most scalable path for high-volume laser integration, particularly for coherent communication applications. Among heterogeneous integration techniques, $\mu$TP stands out for enabling high-throughput, wafer-scale III-V integration with minimal disruption to the silicon photonics process flow, as discussed in Chapter 4. It eliminates the need for singulating and handling individual III-V chips and supports dense integration of non-native components on silicon photonic platforms. A comparison of the fabricated dual-lasers with key state-of-the-art devices is summarized in Table 2.7.

| **Integrated Laser** | **Platform** | **Tuning Range** | **Linewidth** |
|---|---|---|---|
| **This Work (Dual-Laser B)** | III-V-on-Si | **121 nm** | 50 kHz |
| **This Work (Dual-Laser A)** | III-V-on-Si | 111 nm | **13 kHz** |
| **Ref [38]** | III-V-on-Si | **120 nm** | **$\sim$100 Hz** |
| Ref [65] | Hybrid III-V-Si | 65 nm | 60 kHz |
| Ref [62] | Monolithic InP | 74 nm | 360 kHz |
| Ref [63] | Monolithic InP | 35 nm | 80 kHz |
| Ref [64] | Monolithic InP | $\sim$55 nm | 30–50 kHz |
| Ref [66] | III-V-on-Si | 50 nm | 259 kHz |

*Table 2.7: Comparison of key performance metrics for widely tunable narrow-linewidth integrated lasers.*

## 2.5 Broader Application Demonstrators

This section showcases additional application demonstrators that build upon the laser design and integration approach detailed in the preceding sections. While the laser was originally developed to meet the stringent requirements of the 400G-ZR telecom standard, such as ultra-wide tunability and narrow linewidth, its high performance also makes it highly suitable for a broad range of other application domains. These include biomedical sensing, where the same laser was employed with mounted optics for heartbeat monitoring; spectroscopy in the short-wave infrared (SWIR) range enabled through wavelength extension; and gas sensing, demonstrated using a packaged version of the laser featuring an integrated wavelength monitor.

In addition, a linewidth-reduced variant was realized via $\mu$TP integration of III–V devices onto a SiN photonic platform, targeting coherence-critical applications such as LiDAR. Finally, by integrating multiple tunable lasers and optical amplifiers on an iSiPP50G platform, alongside high-speed modulators and detectors, a general-purpose microwave photonic processor chip was demonstrated, showcasing all the essential building blocks for microwave photonic functionality integrated on a single chip for the first time.

These demonstrations collectively underscore the versatility of the laser platform and highlight its potential as a scalable foundation for diverse high-performance photonic systems.

### 2.5.1 Biomedical Sensing Applications

Widely tunable, narrow-linewidth lasers are highly attractive for miniaturized biomedical sensing applications. Their narrow linewidth enables high-resolution measurements, while their broad wavelength coverage allows interaction with a variety of biological materials through absorption peaks across a wide spectral range.

#### 2.5.1.1 Heartbeat Monitoring

In this demonstration, the same laser design described in the previous sections was used for heartbeat monitoring. A micro-lens ($\mu$Lens) was mounted on the laser's output grating coupler, as shown in Fig. 2.58, and the PIC was integrated onto a PCB to create both a fiber-coupled hyperspectral sensor and a wearable wireless prototype (Fig. 2.59).

Figure 2.58 illustrates the $\mu$Lens mounting process, developed by CSEM [68], including a schematic cross-sectional view of the PIC with the integrated laser and $\mu$Lens, a microscope top view of the mounted lens, and an SEM side view of the assembly. Figure 2.59 shows the PCB layout, designed by VTT [69], with two laser dies mounted on a single board. A fiber was aligned to the $\mu$Lens-mounted

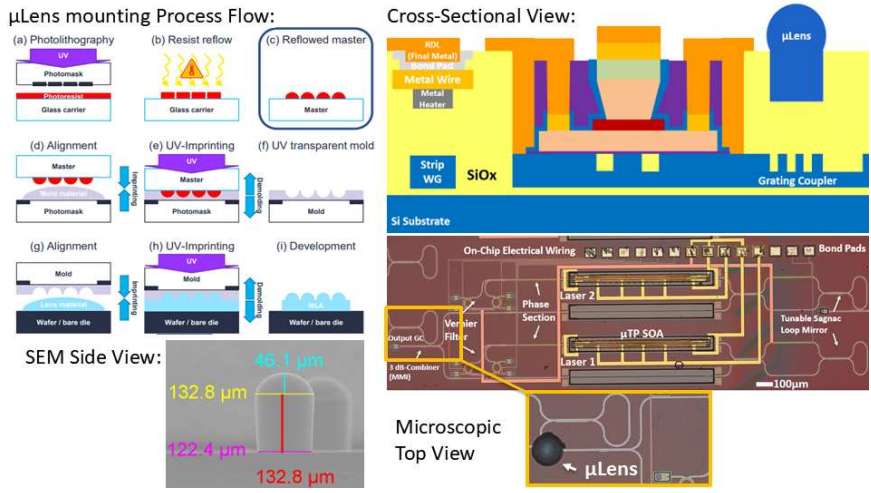



*Figure 2.58: µLens mounting process flow by CSEM (Top Left) [67], along with the schematic cross-section view of the PIC with a micro-transfer-printed laser and a µLens (Top Right). Microscope top view image of the mounted µLens on a PIC (Bottom Right), with a side view SEM image (Bottom Left).*

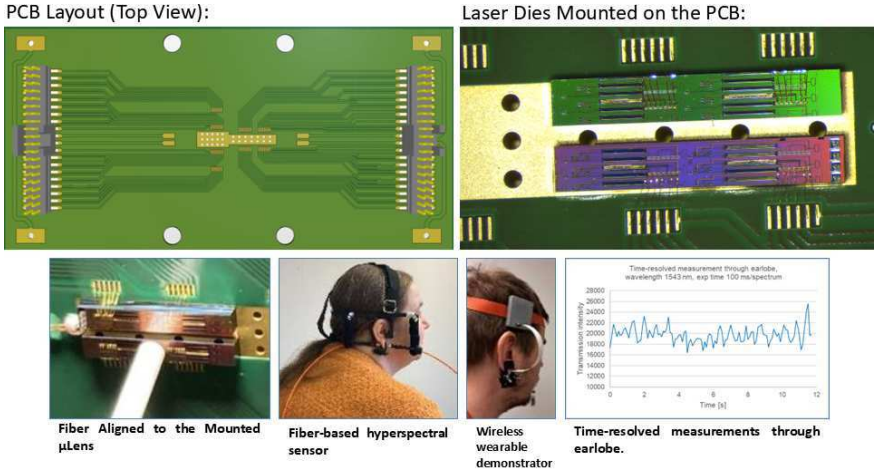



*Figure 2.59: PCB layout by VTT (Top Left). Two Laser dies mounted and wirebonded to the PCB (Top Right). Two prototype configurations as fiber-based and wireless wearable Hyperspectral sensors with the time-resolved measurements of heartbeat through the earlobe.*

laser PIC and wirebonded to the PCB. This setup was used by POLAR to build two types of prototypes: a fiber-based hyperspectral sensor and a wireless wearable device. Both prototypes operate by shining the laser light through the earlobe and

detecting the transmitted signal with a photodetector. The time-resolved intensity signal measured through the earlobe at 1543 nm is also shown in Fig. 2.59. The observed intensity oscillation had a frequency of 1.33 Hz, corresponding to a heart rate of 80 Bit-Per-Minute (BPM), which was attributed to blood pulsation, demonstrating the viability of laser-based heartbeat monitoring.

Although the tunability of the laser was not essential for this specific heartbeat monitoring demonstration, it enabled broader spectral exploration in other tests. Additional experiments conducted by POLAR [70] leveraged the tunable laser to differentiate between resting and active states (e.g., cycling on a stationary bike), supporting its suitability for wearable sensing applications beyond heart rate detection.

#### 2.5.1.2 Spectroscopy

As shown in Fig. 2.60, many biological substances, such as water, fat, protein, and glucose, exhibit absorption peaks within the 1400–1700 nm wavelength range [71]. Integrating tunable lasers that operate in this region directly on-chip significantly facilitates the miniaturization of spectroscopic sensing platforms. To address this, we demonstrated an extended tuning range from 1640 nm to 1710 nm [27], expanding beyond the previously demonstrated 1500–1600 nm range. This was accomplished by micro-transfer printing three different pre-fabricated InP SOA coupons, each engineered with distinct photoluminescence (PL) peaks by III-V Lab, onto an imec iSiPP200 photonic platform. Each micro-transfer-printed laser circuit was custom-designed for optimal performance within its designated wavelength range. Furthermore, the output grating couplers of all three lasers were closely aligned on the chip, and a single micro-lens ($\mu$Lens), developed by CSEM, was designed to cover all outputs simultaneously. This enabled simplified coupling into a single optical fiber for downstream spectral analysis. In total, we achieved over 160 nm wavelength tuning on a single chip, as illustrated in Fig. 2.60. This broad wavelength tuning range is particularly well-suited for short-wave infrared (SWIR) spectroscopy, highlighting the potential of this laser platform for compact, high-performance biosensing applications.

### 2.5.2 Gas Sensing

In collaboration with OnePlanet Research Center [73] and PHIX Photonics Assembly [74], a SiPh chip based on the imec iSiPP200 platform, integrated with $\mu$TP lasers covering the 1500–1600 nm range, is demonstrated in a packaged form for multi-gas sensing. This system enables fine-grained air quality monitoring, providing actionable insights for agriculture and industry to assess and reduce their emissions [75]. The targeted wavelength range is ideal for detecting several environmentally relevant gases, as many exhibit absorption features in this

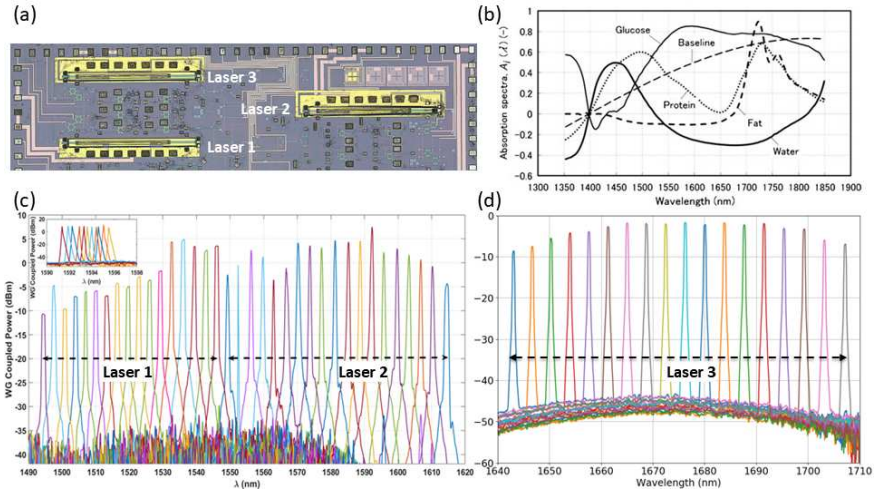



*Figure 2.60: (a) Microscope image of the PIC with three μTP lasers. (b) Absorption peak of biological substances [71]. (c) Previously demonstrated tuning spectrum within the range of 1500-1600 nm [72]. (d) Extended tunability range of more than 60 nm within the range of 1640-1710 nm [27].*

band. Specifically, $CO_2$ shows a prominent absorption peak near 1570 nm [76], and $CH_4$ around 1600 nm [77]. Additionally, gases such as $NH_3$, CO, and $C_2H_2$ display combinational vibrational bands within this range, although their spectral features may be weaker or less pronounced [78].

Figure 2.61 presents the die layout of the SiPh chip, which includes two $\mu$TP-integrated lasers that are routed to a shared output grating coupler via a tunable switch. The chip also features an on-chip wavelength monitoring system consisting of a micro-ring resonator (MRR), connected from the tunable switch's input port to a photodiode (PD) via the MRR's drop port. The wavelength monitoring scheme functions by directing a small portion of the laser output (e.g., 10%) to the MRR. As the MRR heater is driven, its resonance wavelength is tuned. When the MRR's resonant wavelength aligns with the laser output, light is coupled to the drop port and detected by the PD. The resulting electrical signal is read by a microcontroller, which, using a pre-calibrated lookup table of heater current vs. resonance wavelength, determines the actual laser wavelength.

Tuning of the laser can be performed using several control parameters, including pump current to the gain section, tuning of the ring-based Vernier filter, and phase section actuation. Closed-loop feedback is enabled by the wavelength monitoring system, allowing for wavelength locking to a desired value, as illustrated in Fig. 2.62.

The laser PIC was packaged and assembled by PHIX, as shown in Fig. 2.63.

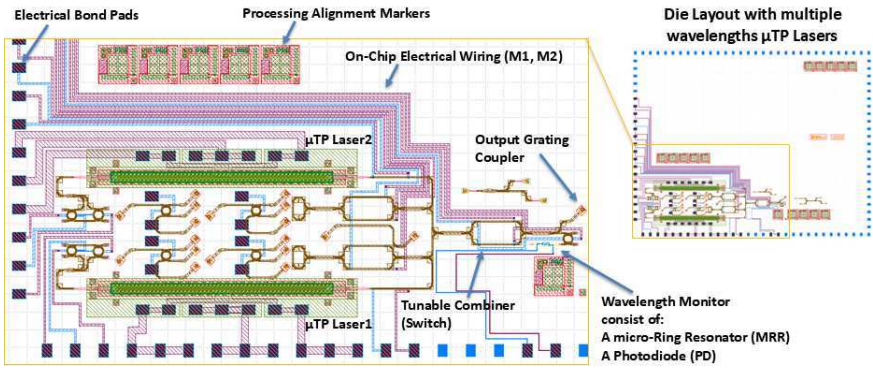



*Figure 2.61: Schematic layout of a SiPh PIC integrating two µTP-based lasers, a tunable optical switch (combiner), and a wavelength monitoring and locking system composed of a micro-ring resonator (MRR) and a photodiode (PD).*

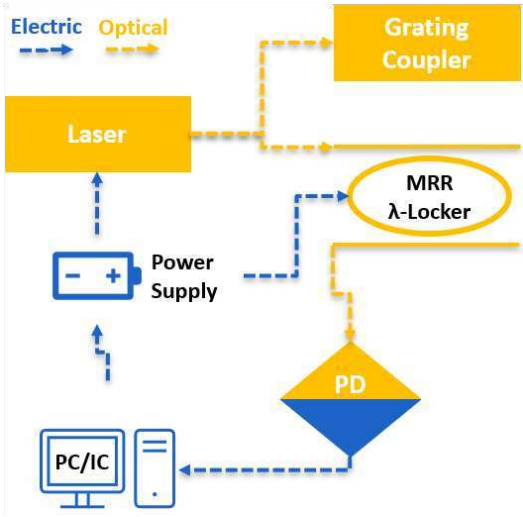



*Figure 2.62: Block diagram illustrating the concept of the on-chip wavelength monitoring and locking system. A portion of the laser output is coupled to an MRR whose resonance is swept via a heater. When the MRR's resonance matches the laser wavelength, the signal is dropped to the PD and converted into an electrical signal for feedback control.*

The packaging process involved mounting the PCB onto a submount, placing and wirebonding the PIC, and actively aligning a fiber array head (FA) to the laser's grating coupler (GC) by maximizing the collected optical power during laser operation. The aligned FA was then fixed in place. The full assembly was mounted onto a thermoelectric cooler (TEC) within a sealed housing, which was hermetically closed under a nitrogen atmosphere. This approach ensures environmental

isolation and long-term reliability.

For cost-sensitive applications where full hermeticity is not required, a non-hermetic packaging option can be considered by encapsulating the laser with a passivating oxide layer. While detailed hermeticity specifications may vary depending on the target use-case, the demonstrated packaging process offers flexibility to meet both high-reliability and low-cost integration needs.

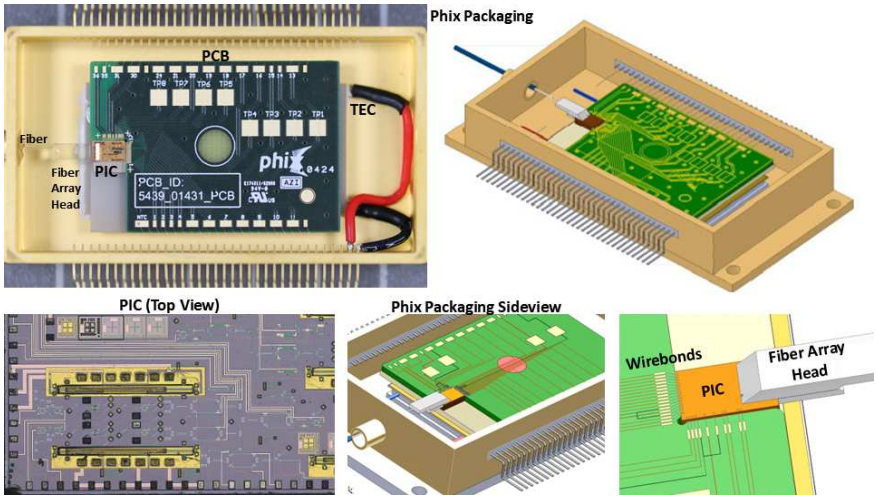



*Figure 2.63: Packaged SiPh laser PIC using PHIX assembly technology. The 3D schematic illustrates the alignment of the fiber array (FA) to the PIC while the chip is wirebonded to the PCB. The microscope image shows the PIC surface, including gold metallization atop the SOA regions to redistribute electrical connections to the bond pads.*

Stability testing by OnePlanet demonstrated that the laser exhibited only $\approx$10 pm of wavelength drift over 4 hours, even without TEC, comparable to a commercial semiconductor laser (Chilas-ATLAS) with a drift of $\approx$4 pm in the same timeframe [79]. The laser output power was measured at $\approx$1.5 mW, which was sufficient for the targeted gas sensing experiments, though lower than the $>$10 mW output of the Chilas-ATLAS (based on hybrid InP-to-SiN integration) [79, 80]. Furthermore, the laser was capable of wavelength sweeps in steps of 13 pm, aligning well with the Chilas-ATLAS, which supports grid steps of 4–10 pm.

### 2.5.3 Linewidth-Reduced Laser for Coherence-Critical Applications

Coherence-critical applications such as optical sensing, narrowband RF signal generation, and frequency-modulated continuous-wave (FMCW) LiDAR demand ultra-low linewidth semiconductor lasers. A promising route to achieve this on-chip involves leveraging the high-Q, low-loss properties of SiN photonics. In this

work, we demonstrated a hybrid integrated laser architecture based on the micro-transfer printing ($\mu$TP) of pre-fabricated InP-based gain sections onto imec low pressure chemical vapor deposition (LPCVD) $Si_3N_4$ platform, realizing a significant reduction in intrinsic linewidth [45, 81].

As shown in Fig. 2.64(a), the laser design relies on a complex mode-evolution taper structure to bridge the significant mode mismatch between the InP and SiN waveguides. This taper sequence includes a transition from a SiN strip to amorphous silicon (a-Si:H), followed by a rib taper and a transition into the InP epitaxial stack. Simulated mode profiles (panels a1–a8) confirm the adiabatic evolution and high coupling efficiency through each stage of the taper.

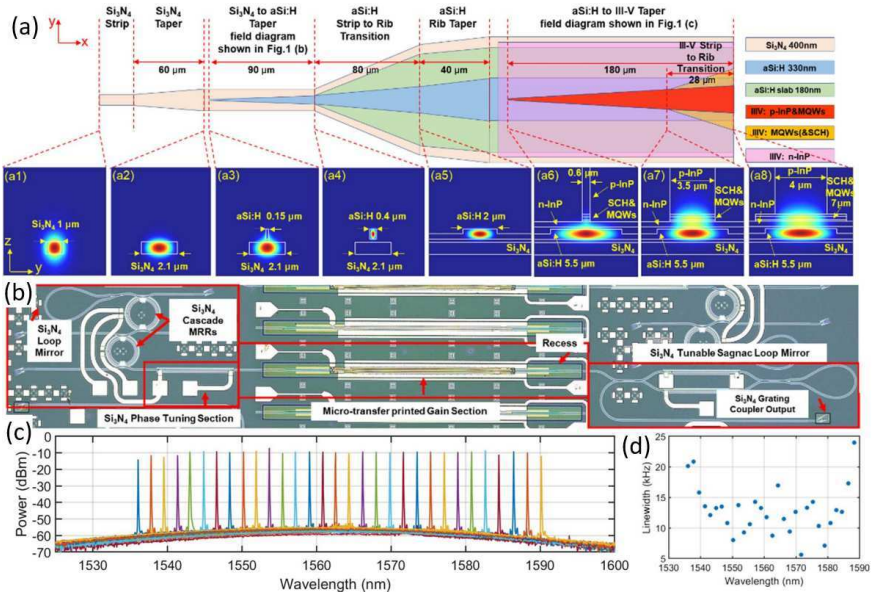



*Figure 2.64: Narrow-Linewidth III–V/SiN laser [81]. (a) Taper design with simulated mode evolution from SiN to InP. (b) Photonic circuit with $\mu$TP-integrated gain, tunable Sagnac loop mirror, MRRs, and phase control. (c) Output spectrum showing 54 nm tuning range. (d) Linewidths <25 kHz across the wavelength tuning range, suitable for coherence-critical applications.*

The photonic circuit layout (Fig. 2.64(b)) incorporates a tunable Sagnac loop mirror, $\mu$TP-integrated gain sections embedded into recesses, cascaded SiN micro-ring resonators (MRRs) for linewidth narrowing, and thermo-optic phase shifters for precise resonance alignment and feedback control. The ultra-low-loss SiN feedback path significantly enhances the photon lifetime, effectively suppressing frequency noise and narrowing the intrinsic linewidth.

As shown in Fig. 2.64(c), the micro-transfer-printed III-V-on-SiN laser exhibits a wide tuning range of 54 nm across the C/L-band, with on-chip output

powers reaching up to 6.3 mW. Linewidth characterization (Fig. 2.64(d)) confirms intrinsic linewidths consistently below 25 kHz, along with a side-mode suppression ratio (SMSR) of approximately 40 dB.

Furthermore, in a follow-up collaborative work [45], this III-V-on-SiN laser platform was successfully employed in a proof-of-concept optical frequency domain reflectometry (OFDR) system. The laser's ability to deliver chirp amplitudes exceeding 20 GHz at a 1 kHz repetition rate, combined with its narrow linewidth and low phase noise, enabled OFDR measurements with sub-centimeter spatial resolution, confirming its suitability for high-precision ranging and sensing applications.

This work underscores the enabling role of $\mu$TP in realizing compact, high-coherence lasers on passive, low-loss platforms. By decoupling the gain material from the photonic circuit, $\mu$TP offers a versatile and scalable pathway for engineering application-specific laser sources across a wide range of spectral bands.

### 2.5.4 Programmable Photonics

One of the most ambitious goals in integrated photonics is the development of a fully reconfigurable microwave photonic processor that acts as a black-box engine, capable of executing a wide range of analog and RF signal-processing tasks without requiring internal reprogramming by the user. Toward this goal, we demonstrated a fully integrated programmable photonic engine, in which all essential building blocks are co-integrated on a single silicon photonic chip. These include widely tunable lasers and SOAs, enabled by the versatility $\mu$TP, alongside high-speed modulators, programmable filters, optical switches, and photodetectors made possible by the high-performance imec iSiPP50G platform [82].

Although $\mu$TP integration of multiple III–V devices onto iSiPP50G has been explored in earlier efforts, this work represents the first complete on-chip demonstration of all the critical active and passive functionalities required for microwave photonic signal processing. This was achieved by $\mu$TP integration of several prefabricated InP-based gain blocks, forming two widely tunable lasers and multiple SOAs, combined with the native capabilities of the iSiPP50G platform, including low-loss filters, dense electrical routing, and high-speed modulation.

As illustrated in Fig. 2.65(a) and Fig. 2.66(a), the photonic engine architecture is composed of modular functional blocks, such as SOA arrays, tunable couplers, phase shifters, and optical switches, interfaced through a fiber array and extensive electrical control. The chip was wirebonded to a PCB for system-level packaging, including integrated RF, DC, and thermal control, as shown in Fig. 2.65(b).

Performance evaluation confirmed wide wavelength tunability (1507–1598 nm), narrow linewidth, and excellent phase noise and power stability. The processor demonstrated programmable filter responses and dynamic signal routing, estab-

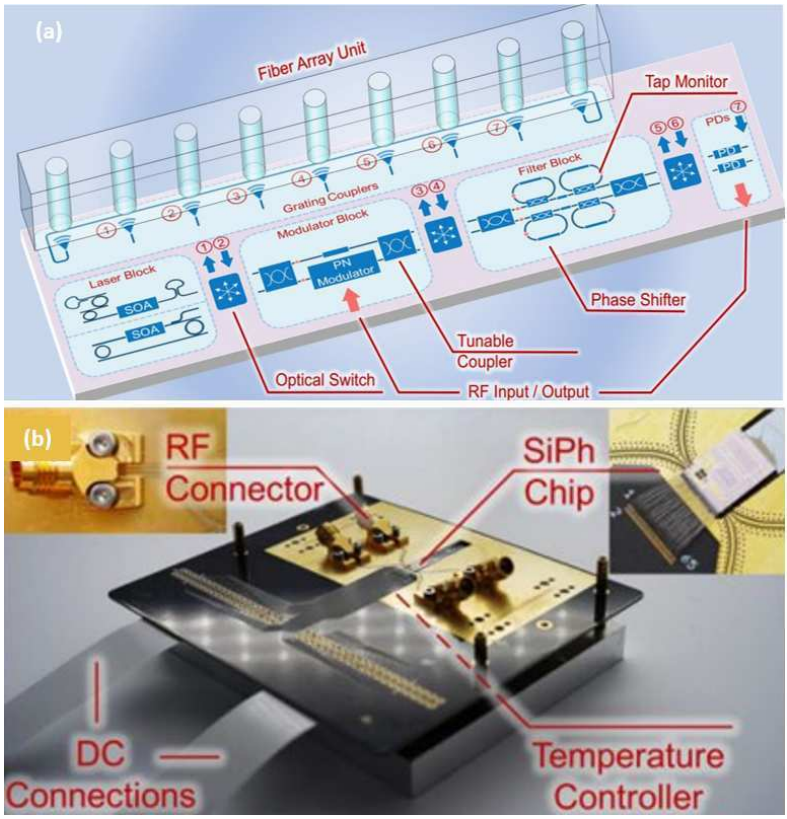



*Figure 2.65: (a) Conceptual schematic of the fully integrated programmable photonic engine, highlighting its modular building blocks: μTP-integrated lasers and SOAs, high-speed modulators, optical switches, tunable couplers, phase shifters, and tap monitors, all interfaced via a fiber array unit. (b) Packaged photonic engine mounted on a PCB with integrated DC, RF, and thermal control interfaces. The SiPh chip, containing all active and passive components, is wirebonded for external interfacing and control [82].*

lishing its viability as a general-purpose photonic signal processor.

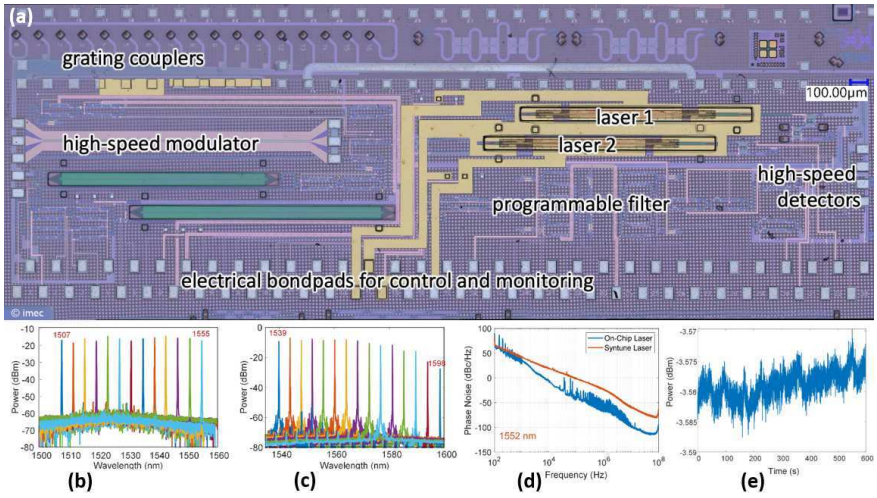



*Figure 2.66: (a) Microscope image of the fabricated iSiPP50G photonic engine chip with labeled components: µTP-integrated tunable lasers, SOAs, high-speed modulators, programmable filter, detectors, and grating couplers. (b–c) Optical spectra demonstrating wide tunability of the on-chip lasers across 1507–1598 nm. (d) Phase noise comparison between the µTP laser and a commercial Syntune laser, showing competitive noise performance. (e) Time-domain power stability trace of the µTP-integrated laser output, confirming suitability for coherent signal processing applications [82].*

## 2.6 Conclusion

In this chapter, we demonstrated, for the first time, a heterogeneous III-V-on-Si laser on the IMEC 400nm+ platform that simultaneously meets the demanding specifications of both ultra-wide tunability and narrow linewidth. The laser was realized via µTP of pre-fabricated InP-based SOAs onto a passive Si photonic circuit, resulting in a modular integration strategy that retains flexibility in laser design while remaining scalable. Extensive design, fabrication, and characterization steps were undertaken, including linewidth measurements, tunability assessment, and spectral analysis.

Beyond meeting the technical targets for data communication standards like 400G-ZR, we showed that this laser architecture could be extended to a broader set of photonic applications. Through a series of demonstrators, we adapted the same or slightly modified versions of the laser for biomedical sensing, spectroscopy in the SWIR range, gas detection using integrated wavelength monitoring, and coherence-critical systems like LiDAR. We also highlighted the integration of multiple µTP lasers and SOAs into a fully programmable photonic engine for general-purpose microwave photonic signal processing. These demonstrations collectively illustrate the versatility of the developed platform and reinforce the viability of

$\mu$TP as an enabling technology for scalable, high-performance, and multifunctional integrated photonic systems.

# References

[1] Wikipedia contributors. *Optical Internetworking Forum*. https://en.wikipedia.org/wiki/Optical_Internetworking_Forum. Accessed 10 August 2025.

[2] OIF. *Member Companies*. https://www.oiforum.com/about-oif/member-companies/. Accessed 10 August 2025.

[3] Optical Internetworking Forum (OIF). *About OIF*. https://www.oiforum.com/about-oif/. Accessed 10 August 2025.

[4] Optical Internetworking Forum (OIF). *OIF*. https://www.oiforum.com/. Accessed 10 August 2025.

[5] Optical Internetworking Forum (OIF). *100G Ultra Long Haul DWDM: Framework Document*. https://www.oiforum.com/wp-content/uploads/2019/01/OIF-FD-100G-DWDM-01.0.pdf, 2019. Accessed: 2025-08-10.

[6] *Implementation Agreement 400ZR*. OIF Implementation Agreement, March 2020.

[7] Optical Internetworking Forum (OIF). *800G Coherent*. Web page, oct 2024. Defines interoperable single-lambda 800G coherent line specs; references release of OIF-800ZR-01.0 (Oct 30, 2024) and 400ZR updates.

[8] Optical Internetworking Forum (OIF). *1600G Coherent*. https://www.oiforum.com/technical-work/hot-topics/1600g-coherent/, 2024. Accessed: 2025-08-10.

[9] FS Community. *How 400G Coherent Optical Communication Accelerating Data Centres*, 04 2024. Updated Apr 7, 2024.

[10] Optical Internetworking Forum (OIF). *400ZR Interoperability White Paper – OFC 2023 Plugfest*. https://www.oiforum.com/wp-content/uploads/OIF_400ZR_OFC2023_Interop_WhitePaper_Plugfest.pdf, 2023. Accessed: 2025-09-08.

[11] Ciena Corporation. *What is 400ZR?*, n.d. Accessed: 2025-08-10.

[12] FS Community. *400G ZR vs. Open ROADM vs. ZR+: What's the Difference?*, 2022. Updated: 2022-01-01. Accessed: 2025-08-10.

[13] Coherent Corp. *Coherent to Showcase Award-Winning 100G and 400G Coherent Transceivers at OFC 2023*. Press release, March 2023. Accessed: 2025-08-10.

[14] Coherent Corp. *II-VI Incorporated Ships 400G ZR+ QSFP-DD-DCO Transceivers to Windstream Wholesale*. Press release, 02 2022. Accessed: 2025-08-10.

[15] Zhang, Jing. *III-V-on-Si transceivers based on micro-transfer-printing*. PhD thesis, Ghent University, 2021.

[16] Alexander W. Fang, Erica Lively, Ying-Hao Kuo, Di Liang, and John. E. Bowers. *A distributed feedback silicon evanescent laser*. Opt. Express, 16(7):4413–4419, Mar 2008.

[17] Stevan Stankovic, Richard Jones, Matthew N. Sysak, John M. Heck, Günther Roelkens, and Dries Van Thourhout. *Hybrid III–V/Si Distributed-Feedback Laser Based on Adhesive Bonding*. IEEE Photonics Technology Letters, 24(23):2155–2158, 2012.

[18] Alexander W. Fang, Hyundai Park, Ying hao Kuo, Richard Jones, Oded Cohen, Di Liang, Omri Raday, Matthew N. Sysak, Mario J. Paniccia, and John E. Bowers. *Hybrid silicon evanescent devices*. Materials Today, 10(7):28–35, 2007.

[19] Rahimi Vaskasi, Javad. *InP-on-Si DFB laser diodes with high wall-plug efficiency, large modulation bandwidth and low noise*. PhD thesis, Ghent University, 2022.

[20] S. Keyvaninia, S. Verstuyft, L. Van Landschoot, F. Lelarge, G.-H. Duan, S. Messaoudene, J. M. Fedeli, T. De Vries, B. Smalbrugge, E. J. Geluk, J. Bolk, M. Smit, G. Morthier, D. Van Thourhout, and G. Roelkens. *Heterogeneously integrated III-V/silicon distributed feedback lasers*. Opt. Lett., 38(24):5434–5437, Dec 2013.

[21] Helene Duprez, Antoine Descos, Thomas Ferrotti, Corrado Sciancalepore, Christophe Jany, Karim Hassan, Christian Seassal, Sylvie Menezo, and Badhise Ben Bakir. *1310 nm hybrid InP/InGaAsP on silicon distributed feedback laser with high side-mode suppression ratio*. Opt. Express, 23(7):8489–8497, Apr 2015.

[22] Amnon Yariv and Xiankai Sun. *Supermode Si/III-V hybrid lasers, optical amplifiers and modulators: A proposal and analysis*. Opt. Express, 15(15):9147–9151, Jul 2007.

[23] Haq, Bahawal. *III-V-on-Si SOAs and DFB/DBR lasers realised using micro-transfer printing*. PhD thesis, Ghent University, 2021.

[24] Dirk Englund, Hatice Altug, and Jelena Vučković. *Low-threshold surface-passivated photonic crystal nanocavity laser*. Applied Physics Letters, 91(7):071124, 08 2007.

[25] Sonja Sioncke, Dennis Lin, Laura Nyns, Annelies Delabie, Aaron Thean, Naoto Horiguchi, Herbert Struyf, S. De-Gendt, and Matty Caymax. *Passivation Challenges with Ge and III/V Devices*. ECS Transactions, 45(4):97, apr 2012.

[26] Camiel Op de Beeck. *Heterogeneous Integration of III-V Semiconductor Light Sources on Low-Refractive-Index Platforms*. Phd thesis, Ghent University, Ghent, Belgium, 2022. Promotors: Bart Kuyken and Gunther Roelkens.

[27] Xin Guo, Emadreza Soltanian, Jing Zhang, Senbiao Qin, Nicolas Vaissière, Delphine Néel, Joan Ramirez, Jean Decobert, Sarah Uvin, and Gunther Roelkens. *Micro-transfer-printed short-wave infrared InP-on-silicon tunable laser*. Opt. Lett., 50(5):1589–1592, Mar 2025.

[28] Albert van Rees. *Widely-tunable and ultra-stable hybrid-integrated diode lasers*. Phd thesis - research ut, graduation ut, University of Twente, Netherlands, January 2024.

[29] Albert van Rees, Youwen Fan, Dimitri Geskus, Edwin J. Klein, Ruud M. Oldenbeuving, Peter J. M. van der Slot, and Klaus-J. Boller. *Ring resonator enhanced mode-hop-free wavelength tuning of an integrated extended-cavity laser*. Opt. Express, 28(4):5669–5683, Feb 2020.

[30] Jens Buus, Markus-Christian Amann, and Daniel J. Blumenthal. *Tunable Laser Diodes and Related Optical Sources*. Wiley, Hoboken, N.J., 2nd edition, 2005. Revised edition of: Tunable Laser Diodes / Markus-Christian Amann, Jens Buus. Boston: Artech House, 1998.

[31] Michael G. Littman. *Single-mode operation of grazing-incidence pulsed dye laser*. Opt. Lett., 3(4):138–140, Oct 1978.

[32] Keisuke Kasai, Masataka Nakazawa, Yasunori Tomomatsu, and Takashi Endo. *1.5μm, mode-hop-free full C-band wavelength tunable laser diode with a linewidth of 8 kHz and a RIN of -130 dB/Hz and its extension to the L-band*. Opt. Express, 25(18):22113–22124, Sep 2017.

[33] K. Kobayashi and I. Mito. *Single frequency and tunable laser diodes*. Journal of Lightwave Technology, 6(11):1623–1633, 1988.

[34] L.A. Coldren. *Monolithic tunable diode lasers*. IEEE Journal of Selected Topics in Quantum Electronics, 6(6):988–999, 2000.

[35] Dominik Gerhard Rabus and Cinzia Sada. *Ring Resonators: Theory and Modeling*, pages 3–46. Springer International Publishing, Cham, 2020.

[36] Ansys Inc. *Ring resonator getting started – Design and initial simulation*. `https://tinyurl.com/mudszryy`, 2020. Accessed: 2025-08-11.

[37] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets. *Silicon microring resonators*. Laser & Photonics Reviews, 6(1):47–73, 2012.

[38] Minh A. Tran, Duanni Huang, and John E. Bowers. *Tutorial on narrow linewidth tunable semiconductor lasers using Si/III-V heterogeneous integration*. APL Photonics, 4(11):111101, 11 2019.

[39] D. S. Elliott, Rajarshi Roy, and S. J. Smith. *Extracavity laser band-shape and bandwidth modification*. Phys. Rev. A, 26:12–18, Jul 1982.

[40] G. M. Stéphan, T. T. Tam, S. Blin, P. Besnard, and M. Têtu. *Laser line shape and spectral density of frequency noise*. Phys. Rev. A, 71:043809, Apr 2005.

[41] Gianni Di Domenico, Stéphane Schilt, and Pierre Thomann. *Simple approach to the relation between laser frequency noise and laser line shape*. Appl. Opt., 49(25):4801–4807, Sep 2010.

[42] A. L. Schawlow and C. H. Townes. *Infrared and Optical Masers*. Phys. Rev., 112:1940–1949, Dec 1958.

[43] K. Kikuchi. *Effect of 1/f-type FM noise on semiconductor-laser linewidth residual in high-power limit*. IEEE Journal of Quantum Electronics, 25(4):684–688, 1989.

[44] K. Kikuchi. *Impact of 1/f-type FM noise on coherent optical communications*. Electronics Letters, 23:885–887, 1987.

[45] G. Dandé, J. Pennanech, C. Charliac, V. Kemlin, V. Crozatier, I. Ghorbel, V. Billault, B. Pan, E. Soltanian, J. Zhang, G. Roelkens, M. Dahlem, J. Song, S. Dwivedi, D. Carbajal Altamirano, C. Cummins, S. Seema Saseendran, P. Helin, J. Ramirez, D. Néel, H. Guillet De Chatellus, and J. Bourderionnet. *Narrow linewidth III-V-on-SiN laser with extended frequency chirp capability based on micro-transfer printing for high resolution distributed acoustic sensing*. Opt. Express, 33(8):17192–17202, Apr 2025.

[46] III-V Lab. *III-V Lab – Research in Semiconductor Devices and Integration with Silicon*. `https://www.3-5lab.fr/index.php`, 2025. Accessed: 2025-08-11.

[47] III-V Lab. *III-V Lab LinkedIn Page*. https://www.linkedin.com/company/iii-v-lab/posts/?feedView=all, 2025. Accessed: 2025-08-11.

[48] Cognex Corporation. *VisionPro Software – PC-based Vision Software for 2D and 3D Applications*. https://www.cognex.com/products/machine-vision/vision-software/visionpro-software, 2025. Accessed: 2025-08-11.

[49] Zhenxu Bai, Zhongan Zhao, Yaoyao Qi, Jie Ding, Sensen Li, Xiusheng Yan, Yulei Wang, and Zhiwei Lu. *Narrow-Linewidth Laser Linewidth Measurement Technology*. Frontiers in Physics, Volume 9 - 2021, 2021.

[50] Zujie Fang, Haiwen Cai, Gaoting Chen, and Ronghui Qu. *Fundamentals of Semiconductor Lasers*, pages 9–39. Springer Singapore, Singapore, 2017.

[51] Hemant More. *Formation of Beats – Meaning, Conditions, and Frequency*. https://thefactfactor.com/facts/pure_science/physics/formation-of-beats/6682/, 2020. Accessed: 2025-08-11.

[52] Wikipedia contributors. *Mach-Zehnder-Interferometer – Wikipedia*. https://de.wikipedia.org/wiki/Mach-Zehnder-Interferometer, 2025. Accessed: 2025-08-11.

[53] G. B. Hocker. *Fiber-optic sensing of pressure and temperature*. Appl. Opt., 18(9):1445–1448, May 1979.

[54] Evandro Conforti, Mareli Rodigheri, Tiago Sutili, and Flavio J. Galdieri. *Acoustical and 1/f noises in narrow linewidth lasers*. Optics Communications, 476:126286, 2020.

[55] *A Novel Scheme for Hundred-Hertz Linewidth Measurements with the Self-Heterodyne Method*. Chinese Physics Letters, 30(8):084208, aug 2013.

[56] L.B. Mercer. *1/f frequency noise effects on self-heterodyne linewidth measurements*. Journal of Lightwave Technology, 9(4):485–493, 1991.

[57] OEwaves Inc. *OEwaves – State of the Art Lasers and Microwave Sources*. https://www.oewaves.com/, 2025. Accessed: 2025-08-11.

[58] OEwaves Inc. *HI-Q® Optical Phase Noise Measurement Equipment & Analyzer System*. https://www.oewaves.com/opnts, 2025. Accessed: 2025-08-11.

[59] OEwaves Inc. *OE4000 HI-Q® Laser Linewidth / Phase Noise Analyzer Datasheet*. https://morephotonics.com/wp-content/uploads/2022/06/OE4000.pdf, 2022. Accessed: 2025-08-11.

[60] OEwaves Inc. *HI-Q® Optical Phase Noise Measurement Equipment & Analyzer System*. https://www.oewaves.com/_files/ugd/d39cf0_40b713a3e11c4c6c8d919ace3696572d.pdf, 2025. Accessed: 2025-08-11. Datasheet for OE4000 Phase Noise Analyzer.

[61] Optical Internetworking Forum. *Implementation Agreement for 400ZR*. Technical Report OIF-400ZR-01.0, OIF, 2020. Accessed: 2025-08-11.

[62] Sylwester Latkowski, Andreas Hänsel, Nandini Bhattacharya, Tjibbe De Vries, Luc Augustin, Kevin Williams, Meint Smit, and Erwin Bente. *Novel widely tunable monolithically integrated laser source*. IEEE Photonics Journal, 7(6):1–9, 2015.

[63] Yasuhiro Matsui, Urban Eriksson, Jan-Olof Wesstrom, Yitong Liu, Stefan Hammerfeldt, Martin Hassler, Björn Stoltz, Niclas Carlsson, Salehe Siraj, and Edgard Goobar. *Narrow linewidth tunable semiconductor laser*. In 2016 Compound Semiconductor Week (CSW)[Includes 28th International Conference on Indium Phosphide & Related Materials (IPRM) & 43rd International Symposium on Compound Semiconductors (ISCS), pages 1–2. IEEE, 2016.

[64] Keith A. McKinzie, Cong Wang, Abdullah Al Noman, David L. Mathine, Kyunghun Han, Daniel E. Leaird, Gloria E. Hoefler, Vikrant Lal, Fred Kish, Minghao Qi, and Andrew M. Weiner. *InP high power monolithically integrated widely tunable laser and SOA array for hybrid integration*. Opt. Express, 29(3):3490–3502, Feb 2021.

[65] Yongkang Gao, Jiann-Chang Lo, Shing Lee, Ronak Patel, Likai Zhu, Jocelyn Nee, Diana Tsou, Rob Carney, and Jibin Sun. *High-power, narrow-linewidth, miniaturized silicon photonic tunable laser with accurate frequency control*. Journal of Lightwave Technology, 38(2):265–271, 2020.

[66] Joan Manel Ramírez, Pierre Fanneau de la Horie, Jean-Guy Provost, Stéphane Malhouitre, Delphine Néel, Christophe Jany, Claire Besancon, Nicolas Vaissière, Jean Decobert, Karim Hassan, et al. *Low-threshold, high-power on-chip tunable III-V/Si lasers with integrated semiconductor optical amplifiers*. Applied Sciences, 11(23):11096, 2021.

[67] Claudio Bruschini, IVAN ANTOLOVIC, Frédéric Zanella, Arin Ulku, Scott Lindner, Alexander Kalyanov, Tommaso Milanese, Ermanno Bernasconi, Vladimir Pesic, and Edoardo Charbon. *Challenges and Prospects for Multi-chip Microlens Imprints on front-side illuminated SPAD Imagers*. 2 2023.

[68] CSEM. *Microlens Array and On-Chip Lens Foundry Services*, 2025. Accessed: 2025-08-14.

[69] VTT Technical Research Centre of Finland. *Integrated Photonic Chips for Sensing & Data*, 2025. Accessed: 2025-08-14.

[70] Polar Electro. *Hartslagmeter, activiteitentracker en fietscomputers — Polar België*, 2025. Accessed: 2025-08-14.

[71] Gameel Saleh, Fatimah Alkaabi, Noor Al-Hajhouj, Fatimah Al-Towailib, and Safa Al-Hamza. *Design of non-invasive glucose meter using near-infrared technique*. Journal of Medical Engineering & Technology, 42(2):140–147, 2018.

[72] Emadreza Soltanian, Grigorij Muliuk, Sarah Uvin, Dongbo Wang, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Stefan Ertl, Johanna Rimböck, Nicolas Vaissiere, Delphine Néel, Joan Ramirez, Jean Decobert, Bart Kuyken, Jing Zhang, and Gunther Roelkens. *Micro-transfer-printed narrow-linewidth III-V-on-Si double laser structure with a combined 110 nm tuning range*. Opt. Express, 30(22):39329–39339, Oct 2022.

[73] OnePlanet Research Center. *Sensor Technology Innovation*, 2025. Accessed: 2025-08-14.

[74] PHIX Photonics Assembly. *PHIX Photonics Assembly – Packaging Foundry for Photonic ICs*, 2025. Accessed: 2025-08-14.

[75] OnePlanet Research Center. *Sensor Technology – Innovation at OnePlanet*. `https://www.oneplanetresearch.com/innovation/sensor-technology/`, 2025. Accessed: 2025-08-11.

[76] Joanna Marshall, George Stewart, and Gillian Whitenett. *Design of a tunable L-band multi-wavelength laser system for application to gas spectroscopy*. Measurement Science and Technology, 17(5):1023, apr 2006.

[77] Ramya Selvaraj, Abdul Nasir K.T., Nilesh J. Vasa, and Shiva Nagendra S.M. *Monitoring of CO2 and CH4 composition in a biogas matrix from different biomass structures*. Sensors and Actuators B: Chemical, 249:378–385, 2017.

[78] Chunhui Hao, Xiao Fu, Xiaoyong Jiang, Yutong Li, Juyi Sun, Haitao Wu, He Zhu, Qing Li, Yunhai Li, Zhangcheng Huang, Fang Zhong, Ting He, Jinshui Miao, and Weida Hu. *Greenhouse Gas Detection Based on Infrared Nanophotonic Devices*. IEEE Open Journal of Nanotechnology, 4:10–22, 2023.

[79] Chilas BV. *Chilas ATLAS – Wavelength Tunable Laser*. https://chilasbv.com/chilas-atlas-wavelength-tunable-laser/, 2025. Accessed: 2025-08-11. Ultra-narrow linewidth laser with wide tunability range across multiple wavelengths (685 nm, 850 nm, 1550 nm, 1600 nm, 1700 nm).

[80] Chilas BV. *Hybrid-Integration External Cavity Laser (ECL) Technology*. https://chilasbv.com/technology/, 2025. Accessed: 2025-08-11. Describes the use of InP RSOA gain medium and $Si_3N_4$ waveguide circuit with Vernier-effect micro-ring resonators for ultra-narrow linewidth lasers.

[81] Biwei Pan, Jerome Bourderionnet, Vincent Billault, Guenole Dande, Marcus Dahlem, Jeong Hwan Song, Sarvagya Dwivedi, Diego Carbajal Altamirano, Cian Cummins, Sandeep Seema Saseendran, Philippe Helin, Joan Ramirez, Delphine Néel, Emadreza Soltanian, Jing Zhang, and Gunther Roelkens. *III-V-on-Si3N4 widely tunable narrow-linewidth laser based on micro-transfer printing*. Photon. Res., 12(11):2508–2520, Nov 2024.

[82] Hong Deng, Jing Zhang, Emadreza Soltanian, Xiangfeng Chen, Chao Pang, Nicolas Vaissiere, Delphine Neel, Joan Ramirez, Jean Decobert, Nishant Singh, Guy Torfs, Gunther Roelkens, and Wim Bogaerts. *Single-chip silicon photonic engine for analog optical and microwave signals processing*. Nature Communications, 16(1):60100, 2025.

# 3

# Micro-Transfer Printing Compatible High Saturation Power SOA

This chapter is organized into five sections as follows:

- Aiming for $\mu$TP-compatible High Saturation Power SOA (3.1): This section explains the necessity and importance of high saturation power Semiconductor Optical Amplifiers (SOAs), especially as power boosters for integrated III-V-on-Si lasers, and why achieving this through $\mu$TP integration is a key goal.
- Design (3.2): This section outlines the fundamentals of increasing the saturation power level of an integrated SOA. It then introduces a novel generic design scheme that combines the discussed methods into a unified approach. A schematic layout with specific dimensions, based on simulations, will be provided to prepare the layout mask for fabrication.
- Fabrication (3.3): This section details the fabrication and $\mu$TP integration processes of the proposed high saturation power SOAs.
- Characterization (3.4): This section presents the performance of the integrated SOAs, including the extraction of gain, saturation power level, and wall-plug efficiency.
- Conclusion and Future Works (3.5): This final section highlights the significance of the demonstration and compares it with the state-of-the-art heterogeneously integrated high saturation power SOAs. Moreover, three more

$\mu$TP-friendly schemes are provided as alternatives; hence, the feasibility of design and fabrication are discussed.

## 3.1 Aiming for $\mu$TP-compatible High Saturation Power SOA

Photonic integrated circuits (PICs) have experienced rapid development in recent years, leading to a growing number of applications. Silicon Photonics (SiPh) enables the fabrication of PICs on 200 mm or 300 mm SOI wafers with high uniformity and yield, leveraging existing CMOS fabrication infrastructure. Since silicon cannot provide optical gain, III-V semiconductors have been integrated into SiPh, as discussed in Chapters 1 and 2. Consequently, SiPh-based PICs have been demonstrated for various applications, including integrated III-V-on-silicon two-dimensional optical beam scanners with over 100 integrated optical components, such as lasers and amplifiers [1, 2], microwave photonics circuits [3–7], general-purpose programmable photonics [7–9], and optical communication modules [10–13]. Although PICs are typically small, in the $mm^2$ range [14], their performance is often limited by the availability of high-gain and high-output power optical amplifiers that can be integrated into such PICs [4, 15], as there is a need for these PIC-enabled devices to emit relatively high optical power, even in the hundreds of milliwatts (mW) range [14]. For instance, the OIF 400G-ZR standard for coherent communications, mentioned in Chapter 2, specifies an output optical power range of -10 dBm to 0 dBm for the transmitter, but does not specify a power range for the laser module itself within the transmitter. Therefore, it is essential to consider all possible insertion losses within a transmitter across different modules to ensure sufficient optical power from the integrated laser. Consequently, we aim for an output power range of 14.5-17 dBm (30-50 mW) for the laser module to meet the requirements of most applications.

Although some demonstrations have shown that lasers can emit well into the hundreds of milliwatts power range in a single transverse mode [16], relying solely on laser power is often not favorable for several reasons. First, downstream losses, both linear and nonlinear, can significantly reduce the delivered power, making this approach energy-inefficient and thus favoring the use of a booster SOA. Second, high-power laser operation might compromise performance, which often occur in widely tunable and mode-locked lasers that have limited operating regimes where the spectrum is not compromised by gain compression [14]. Third, using a separate booster amplifier can help address several potential reliability concerns that may arise when relying solely on high-power laser sources, for example, thermal and power management challenges within a confined footprint.

Despite the development of several SOAs on both the InP platform and the hy-

brid III-V-on-silicon platform, achieving high gain and high output power remains challenging [17]. The highest output power from a C-band InP discrete SOA was achieved using a slab-coupled optical waveguide (SCOW) design [18]. Although this design provides watt-level output power, it requires a dedicated layer stack and an amplifier length of 1 cm, making co-integration with other photonic components challenging [17]. Moreover, the hybrid III-V-on-Si platform offers the advantage of tailoring the SOA design by modifying the hybrid III-V/Si cross-section, in addition to the purely InP-based platforms, which allows modifications to length and width parameters [14]. Another demonstration reported a discrete InP/InGaAsP SOA with a 3-quantum-well chip, achieving a saturation output power of 19.6 dBm and a gain exceeding 15 dB [17, 19]. However, in monolithic integration, many different components must be integrated together, and specific integration for high-power SOAs is not trivial [17, 20, 21]. On the other hand, $\mu$TP offers the advantage of integrating pre-fabricated and tailored devices from different native substrates onto the same target SiPh wafer/chip.

III-V-on-Si SOAs have also been developed in the Phtonics Research Group (PRG) of UGent-IMEC over the past years, using both DVS-BCB adhesive die-to-wafer bonding [15, 17, 22] and $\mu$TP-compatible methods [23–25]. The former provides 27 dB gain with over 17 dBm output power. Although it is based on die-to-wafer bonding, the design can be modified to be $\mu$TP-compatible by incorporating a selective release etch layer in the epitaxial structure (such as AlInAs sandwitched between the n-InP and substrate InP) as well as introducing tethers to make the devices suspended on the native InP substrate. In the latter cases, the focus has been on developing SOAs as the gain medium for integrated III-V-on-Si lasers and lossless switches, which provide higher gain and modest saturation power. This is also observed in [23], where the saturation output power is limited to 15 mW/9 mW (11.7 dBm/9.6 dBm) while providing small signal gain up to 17 dB/23 dB.

Therefore, this chapter focuses on combining different methods of achieving high saturation power in SOAs into a unified approach and proposing a novel generic $\mu$TP-compatible scheme to enable designers to tailor the SOA based on the requirements of specific applications. This will be followed by providing a specific design of a high saturation power SOA based on simulations as a booster for the previously demonstrated III-V-on-Si lasers in chapter 2, while keeping the epitaxial structure similar to the SOAs of the lasers. This approach allows both the laser's SOA and the booster's SOA to be fabricated simultaneously on the same native substrate, reducing the need for different epitaxial structures and processing steps, and facilitating more straightforward integration. This strategy supports the scalability potential of the $\mu$TP integration method, making it ready for wafer-scale integration. All the aforementioned considerations align with the roadmap of the $\mu$TP integration method, aiming to provide generic integrated active compo-

nents like lasers and booster amplifiers as part of the PDK of SiPh platforms like imec iSiPP50G, Si-400 nm, and 400nm+. This allows the final circuit designer to choose the PDK components based on the wavelength range and the type of the device in line with the desired application.

## 3.2 Design

An optical amplifier generally provides gain to the input optical power, enhancing it. However, as the input optical power increases, the gain provided by the amplifier decreases. At a specific input power level, the gain reduces to half of its maximum or unsaturated value, known as the input saturation power of the SOA. The material gain saturation power ($P_s$) in an optical amplifier is given by Eq. 3.1 [17]:

$$P_s = \frac{hc\sigma_{xy}}{\lambda a \tau \Gamma_{xy}}, \quad g = \frac{g_0}{1 + \frac{P}{P_s}} \tag{3.1}$$

Where $h$ is the Planck constant, $c$ is the speed of light, $\lambda$ is the wavelength in vacuum, $\sigma_{xy}$ is the cross-sectional area of the active material, $a$ is the differential gain, $\tau$ is the carrier lifetime, $\Gamma_{xy}$ is the confinement factor of the optical mode in the active region, $g_0$ is the maximum gain coefficient, and $P$ is the optical power. For further details on saturation effects of optical amplifiers, refer to existing literature [26, 27].

To increase the saturation power level of an SOA, one can reduce the optical power density in the active region of the SOA, essentially expanding the mode as much as possible throughout the SOA's active region. This is derived from the aforementioned equation (Eq. 3.1), which relates the saturation power of the SOA to the cross-section and the confinement factor in the active region. Based on this, there are two strategies to increase the saturation power:

- Increasing the active region cross-section: This expands the optical mode profile and reduces the optical power density in the active region.
- Lowering the confinement in the active region: This also reduces the optical power density in the active region.

This chapter focuses on providing a high saturation power SOA based on the hybrid III-V-on-Si model, which already lowers the confinement in the active region of the SOA, specifically in the quantum wells (QWs), leading to higher saturation power as per the mentioned formula. This is illustrated in the following figure (Fig. 3.1), which shows the optical mode profile of an SOA with and without the Si waveguide underneath. The confinement of the mode profile reduces in

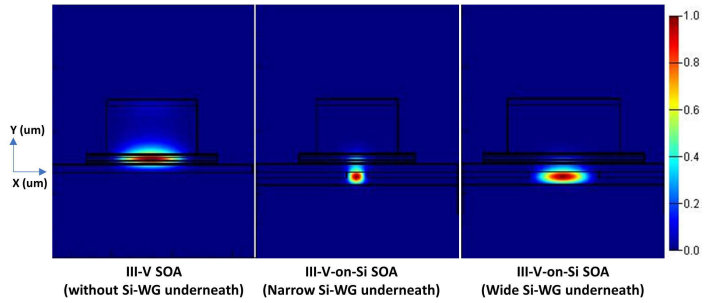



*Figure 3.1: A comparison of optical mode profile confinement in the QWs of SOAs based on III-V and hybrid III-V-on-Si structures. By incorporating the underlying Si waveguide and making it wider, the confinement in the QWs reduces as the mode gets pushed down into the Si waveguide.*

the QWs by incorporating the underlying Si waveguide and making it wider as the mode gets pushed down into the Si waveguide.

To further increase the saturation power of a hybrid SOA, we can widen the active region cross-section. This results in lower power density and increased saturation power. However, a significantly larger active region cross-section in a hybrid SOA can push the mode towards the active region due to an increased effective index in the III-V, leading to higher confinement, which contradicts the goal of reducing confinement and limits the increase in saturation power or even decreases it.

Conversely, a too narrow active region pushes the mode profile more into the Si waveguide underneath, providing significantly lower confinement in the active region but with the cost of significantly reduced gain provided by the SOA, which is the primary function of the amplifier.

Therefore, it is not feasible to widen the active region cross-section or lower the confinement without consequences, as these strategies will conflict beyond a certain point. Thus, a compromise is needed in the design to provide sufficient gain while increasing the saturation power. Conventional hybrid designs are not ideal for this purpose, so we propose the hybrid III-V-on-Si tapered design, as illustrated in the following schematic (Fig. 3.2). This design allows more control over the cross-section and confinement to provide both sufficient gain and increased saturation power. The proposed scheme provides higher gain in the first half (left side) of the SOA, where light enters through a Si waveguide and partially couples to the III-V active region (QWs) through a III-V/Si taper structure. This setup provides higher power density and higher confinement in the active region. Gradually, by increasing the cross-section of the active region towards the second half of the SOA (right side), the confinement and optical power density decrease, leading to higher saturation power. Meanwhile, the width of the underlying Si waveguide is

also increased along the SOA to maintain a relatively low confinement in the active region. By maintaining a balanced ratio of widening the III-V and the underlying Si waveguide, the SOA can provide sufficient gain initially without getting saturated towards its end, where the light exits through a Si waveguide using an inverse hybrid taper.

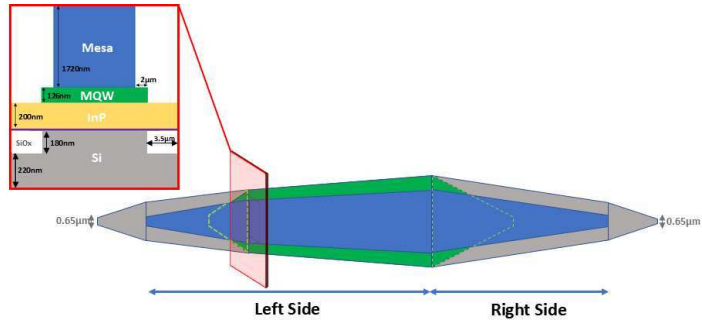



*Figure 3.2: The proposed tapering scheme for the III-V-on-Si integrated SOA to increase the optical saturation power level, while maintaining enough optical gain.*

To reduce interactions between the confined mode and the sidewalls, the QW region is set to be 2 $\mu$m wider on each side than the p-InP mesa [17], while the underlying Si waveguide is tapered up/down from/to a 650 nm single-mode rib waveguide, as the SOA is intended for use in a PIC on the Si-400 nm platform with a 180 nm partial etch step.

Considering $\mu$TP as the intended integration method, making the underlying Si waveguide 2 $\mu$m wider than the QWs on each side, provides sufficient room for lateral misalignment. According to [23] and the Fig. 2.20 (left) in the section 2.2 of chapter 2 as well as Fig. 2.24(b), the coupling between the Si and III-V waveguides through the hybrid adiabatic taper remains effective for misalignments of up to 1.5 $\mu$m. This will however reduce the overall confinement in the SOA, leading to higher saturation power at the cost of lower overall gain.

The modified proposed scheme is shown in Fig. 3.3 and simulated using Ansys Lumerical MODE as shown in Fig. 3.4. Simulations show the minimum/maximum optical confinement of 0.050%/0.052% per well (excluding the coupling tapers). Notably, all tapering transitions occur adiabatically. Due to the large confinement in the silicon waveguide, the mode mismatch between the silicon waveguide and the hybrid III-V/Si waveguide is small. The coupling efficiency of the taper and back-reflections at its tip were simulated, showing coupling losses below 0.05 dB per taper and reflections at the III-V taper tip below -45 dB, respectively.

The mask for the III-V high saturation power SOAs, covering an area of $3.65 \times 3.53$ mm² on a 2-inch InP epitaxial wafer, is shown below in Fig. 3.5.

The mask for SOI fabrication is illustrated in the Fig. 3.6. To minimize the

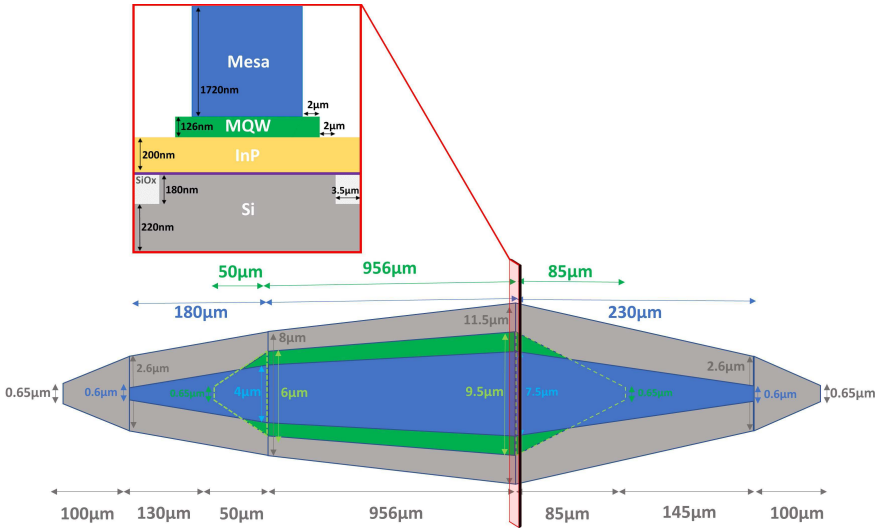



*Figure 3.3: The modified tapering scheme for the III-V-on-Si integrated SOA to increase the optical saturation power level, while maintaining sufficient optical gain, reducing side wall interactions, and enhancing the tolerance to lateral misalignment.*

external reflections back to the micro-transfer-printed SOA, reflectionless grating couplers with a simulated back-reflection less than -40 dB are incorporated in the PIC [28]. The fabrication of the SOI circuit was performed using electron-beam lithography (EBL) for rapid prototyping. Two modes of EBL writing are incorporated in the design:

- Vector Scan Mode (VSM): In this mode, the electron beam is deflected to write the pattern by scanning over the surface in a series of small, discrete steps. This method involves moving the beam to specific coordinates to expose the resist point-by-point, which is ideal for creating complex and detailed patterns like grating couplers, as shown in Fig. 3.6. This mode has a maximum range of 500 $\mu$m x 500 $\mu$m in the RAITH VOYAGER EBL tool used in the PRG. Consequently, structures larger than this may suffer from stitching errors due to misalignment at field boundaries, known as Field-Stitching.

- Fixed Beam Moving Stage (FBMS): This mode allows for continuous writing of elongated, straight, or curved paths without stitching errors. It is particularly useful for fabricating structures like optical waveguides, where precision and continuity are crucial, as used for the tapering Si waveguides in the mask shown in Fig. 3.6.

The overall schematic GDS layout of the III-V coupons on top of the Si waveg-

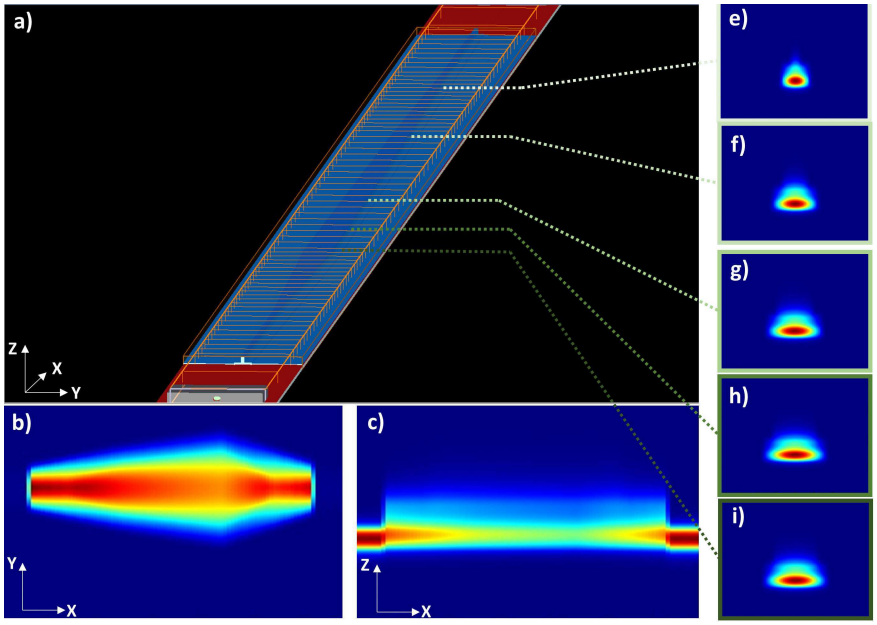



*Figure 3.4: Simulation of the hybrid optical modes in the proposed amplifier using Ansys Lumerical MODE. (a) Perspective of the simulated tapered hybrid SOA. Top-view and side-view of the propagation over the SOA are shown in (b) and (c), respectively. Optical mode profiles from the narrowest to the widest part of the tapered SOA waveguide is shown in (e)-(i), excluding the coupling tapers to the single-mode Si waveguides.*

uide circuits, along with the final metallization mask, is shown in Fig. 3.7. To better manage the injected electrical power density across the two sides of the SOA, enhancing gain on the left and preventing saturation on the right, we incorporated an electrical isolation trench in the middle of the SOA. This allows for the simultaneous and separate injection of pump current.

## 3.3 Fabrication

In this section, we will delve into the fabrication and integration steps of the proposed III-V-on-Si high saturation power SOA using the $\mu$TP method. This section is divided into the following subsections: SOI Fabrication to create the Si waveguide circuit, SOA Fabrication, and the Integration and Post-Processing of the SOAs on the SiPh circuit.

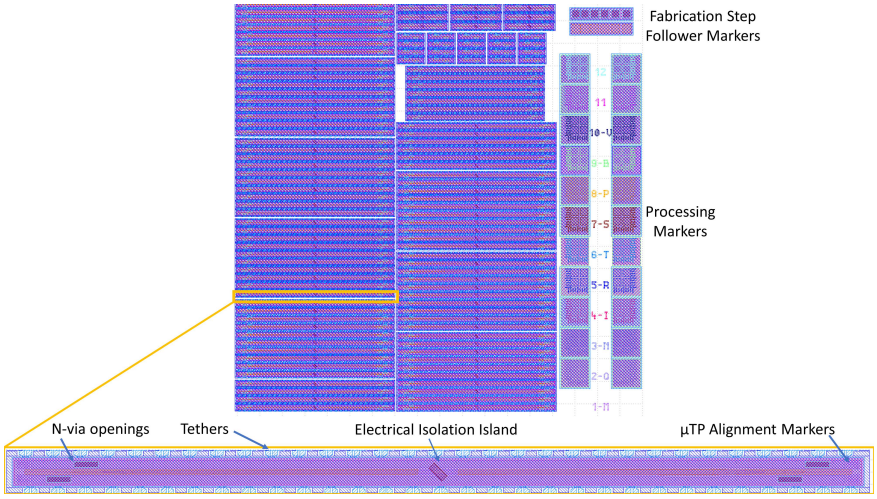



*Figure 3.5: The GDS mask prepared for the fabrication of the proposed InP-based SOA coupons.*

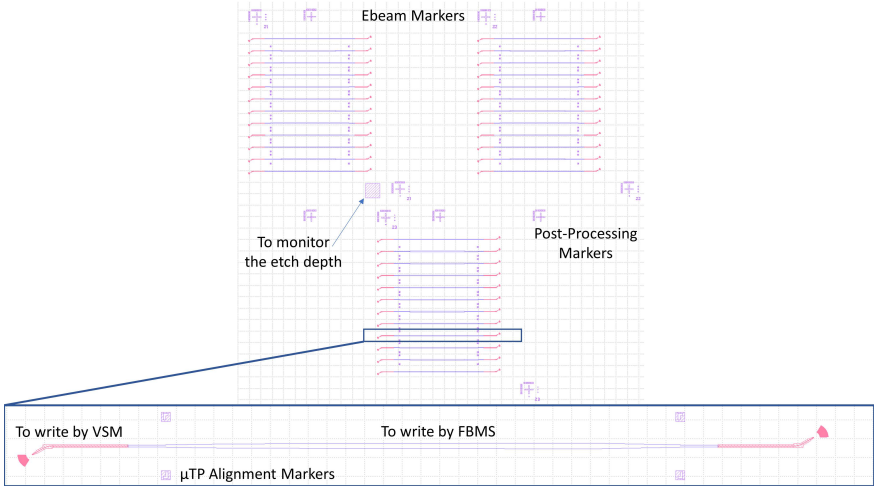



*Figure 3.6: The GDS mask prepared for patterning the Si waveguide circuits by e-beam lithography.*

### 3.3.1 SOI Fabrication

The SOI fabrication process, carried out in the PRG cleanroom facility, begins with an SOI wafer featuring a 400 nm thick crystalline silicon device layer atop a 2 $\mu$m buried oxide layer. Waveguide circuits are defined using electron beam lithography (EBL), followed by a partial 180 nm etch step via reactive ion etching (RIE), as

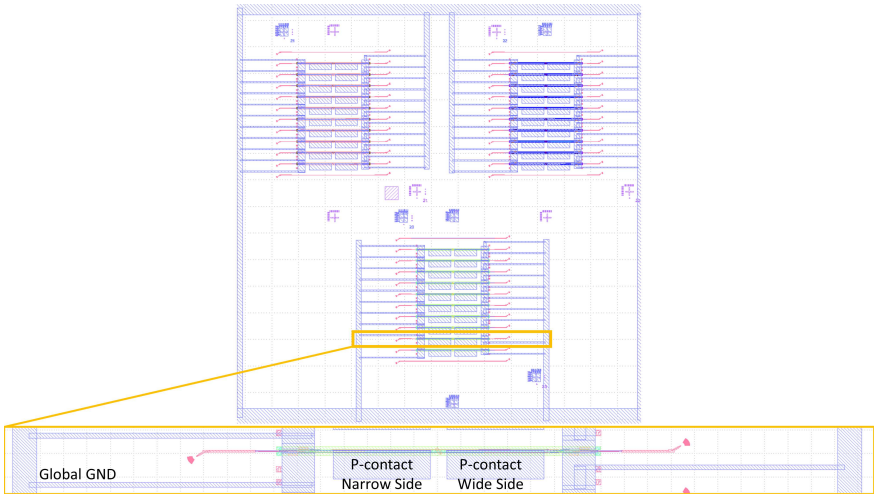



*Figure 3.7: The GDS mask showing the InP based SOA coupon on top of the Si waveguide with the final metal on top.*

shown in Fig. 3.8. The resulting waveguide cross-section closely resembles that of the imec 400 nm silicon photonics platform, indicating compatibility. If this demonstration proves successful, the device could serve as a building block within the imec 400 nm platform. The use of EBL in this context is intended to shorten the turnaround time during prototyping.

Next, a thin DVS-BCB adhesive layer (BCB diluted with Mesitylene in a ratio of 1:5) is spin-coated to achieve a thickness of 40 nm, enhancing the bonding strength between the III-V SOA and the underlying Si waveguide. This is followed by a soft bake at 150 °C for 20 minutes, then gradually cooling to room temperature just before the $\mu$TP, as shown in Fig. 3.8. A microscope image of the fabricated SiPh chip is shown in Fig. 3.9.

### 3.3.2 SOA Fabrication

The fabrication steps for the SOAs are shown schematically in Fig. 3.10, which are carried out in the PRG cleanroom as well. The process flow as well as the epitaxial InP structure used here is similar to what described in 2.3, with a few minor differences:

- The photoluminescence (PL) peak of the epitaxial structure is at 1495 nm.
- All patterning steps were done using contact photolithography (instead of EBL for SOA mesa patterning in 2.3).
- The electrical isolation trench between the narrow and wide sides of the

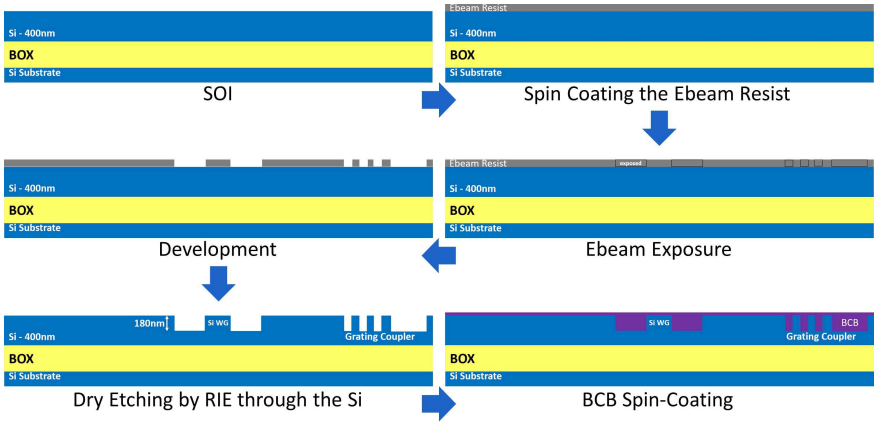



*Figure 3.8: Waveguide circuit fabrication steps.*

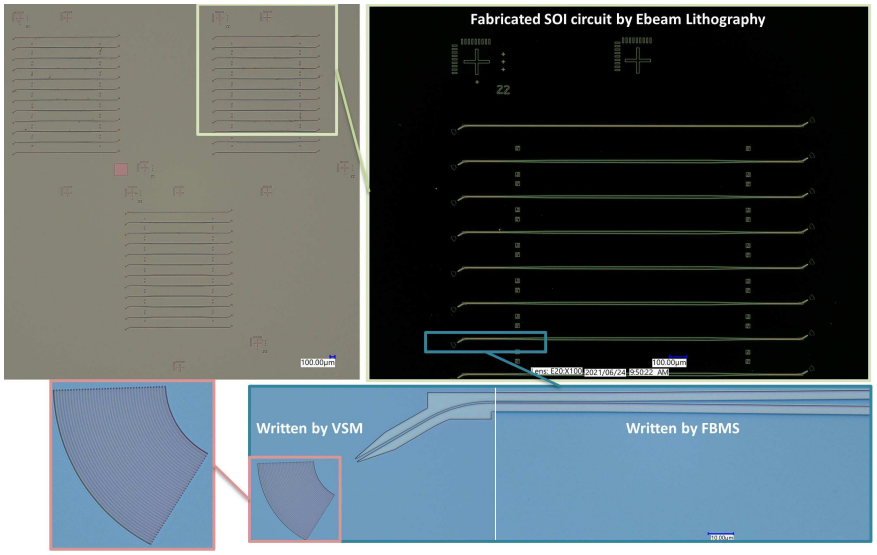



*Figure 3.9: The microscope image of the fabricated waveguide circuit.*

SOA, which is created by ICP etching 200 nm of cladding p-InP mesa before p-metal deposition as illustrated in Fig. 3.10(k1).

Figure 3.11 shows a microscope image of the fabricated coupons and cross-sectioning FIB images of the electrical isolation island, a wide section of the SOA, and the taper tip of the SOA, accompanied by side-view SEM images of the tapers and isolation island in Fig. 3.12.

Figure 3.13 shows a side-view SEM image of the suspended coupons after

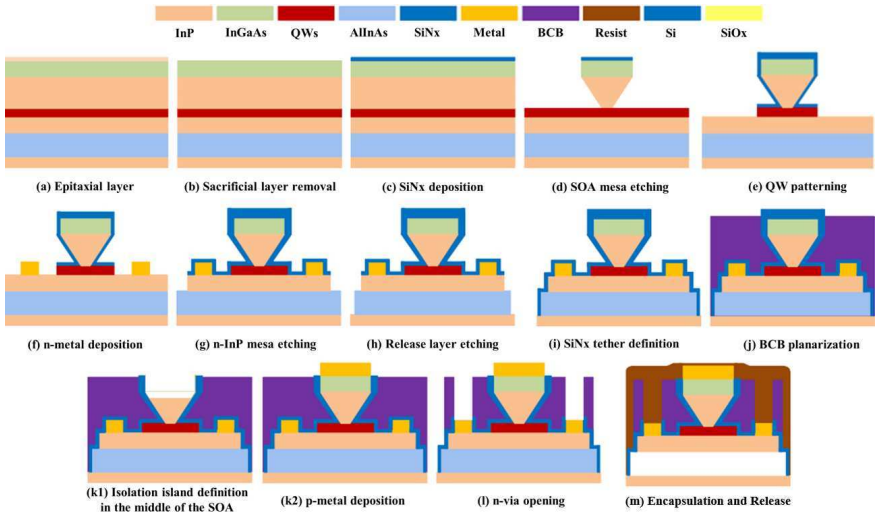



*Figure 3.10: InP-based SOA coupon fabrication steps.*

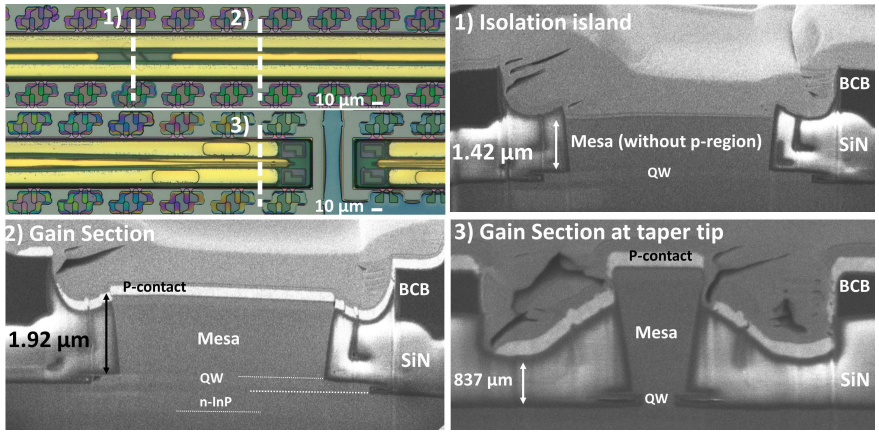



*Figure 3.11: FIB cross-section images of the fabricated InP SOA coupons. Places where the FIB images were taken are marked on the top left microscope image which shows a top-view of the SOA coupons.*

release on the InP substrate, as well as the remaining parts of the tethers after the coupon is picked up.

### 3.3.3 Integration and Post-Processing

As described in 2.3 and shown in Fig. 3.14, $\mu$TP was performed using an X-Celeprint $\mu$TP-100 lab-scale printer with a PDMS stamp featuring a post of 1450

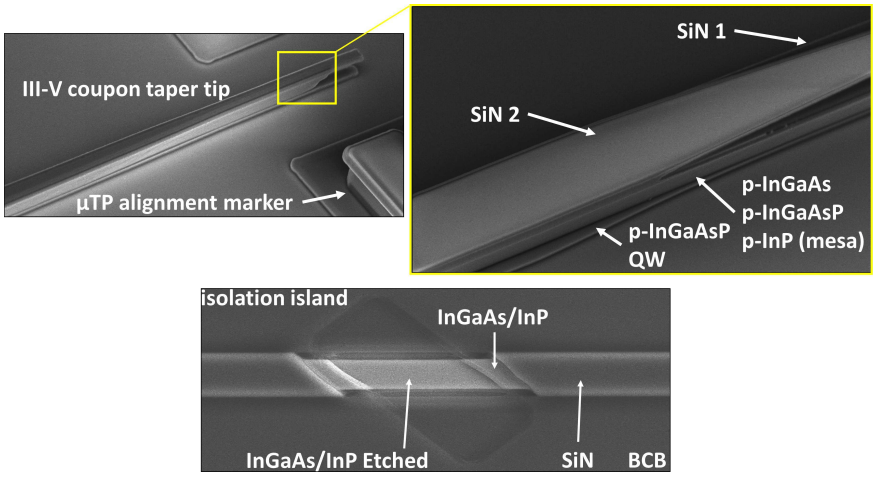



*Figure 3.12: Side view SEM images of the taper and the electrical isolation island of the SOA coupons.*

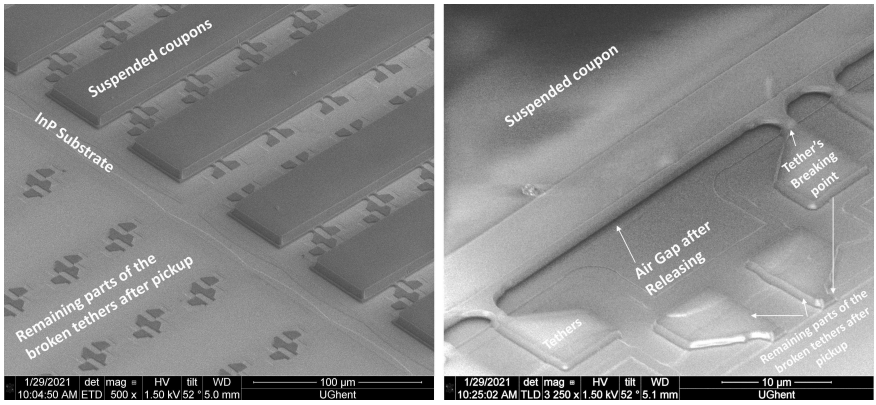



*Figure 3.13: Side view SEM images of the encapsulated SOA coupons after release, showing the suspended coupons on their tethers as well as the breakage point of the remaining tethers after pickup.*

× 50 $\mu$m² and a height of 50 $\mu$m, used for printing 1420 × 47.5 $\mu$m² SOA coupons. Fig. 3.15 displays a microscope image of a printed coupon on the Si waveguide.

The process continues with an Oxygen-plasma etch using RIE to remove the PR encapsulation on the printed coupons (Fig. 3.14(e)). This is followed by fully curing the BCB bonding layer at 270°C for about 2 hours, with a gradual temperature profile taking approximately 6 hours in total. Post-printing processing concludes with completing the electrical circuit by depositing 40 nm Ti and 1 $\mu$m Au on top of the SiPh chip (Fig. 3.14(f)). A microscope image in Fig. 3.16 shows

an array of resulting devices.

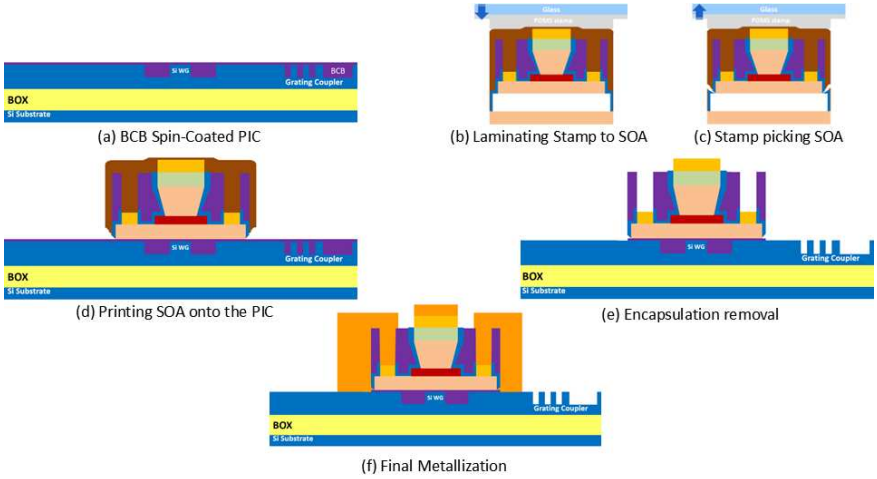



*Figure 3.14: Process flow of micro-transfer printing and post processing.*

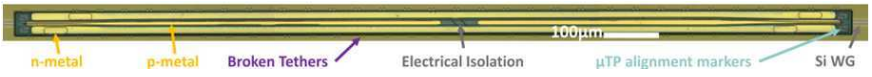



*Figure 3.15: Microscope image of a printed SOA coupon on the Si waveguide.*

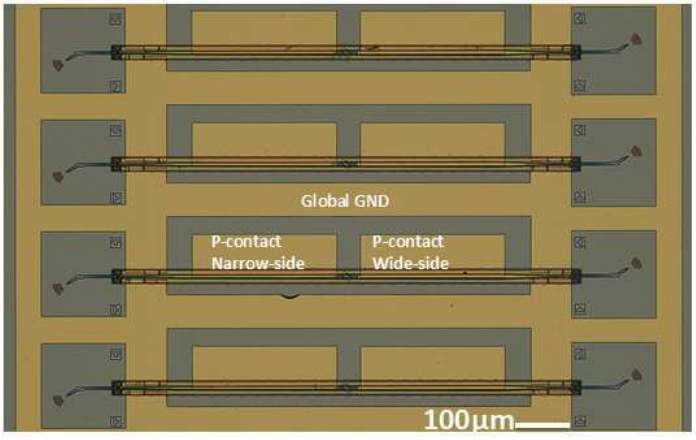



*Figure 3.16: Microscope image of a printed array of SOA coupons on the SiPh chip with the final metallization on top to complete the circuit.*

## 3.4 Characterization

To characterize the SOA, the sample was placed on a temperature-controlled stage set to 20 °C for all measurements. The device under test was optically probed using cleaved standard single-mode fibers (SMFs) on a fiber stage angled at 10°, as shown in Fig. 3.17.

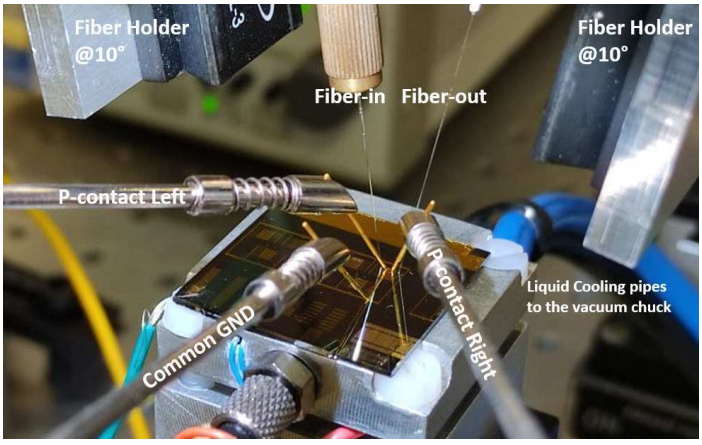



*Figure 3.17: Measurement setup of the integrated high saturation power SOA.*

To better control the narrow and wide sides of the SOA, which are electrically separated by the isolation trench, two Keithley 2400 SourceMeters were used to drive each side of the amplifier simultaneously and independently through separate probe needles. The left/right SOA sections with 3960/6719 $\mu$m² of surface area have differential resistances of 11/9 Ω, respectively. A bias current of 100 mA corresponds to an injection current density of 2.525kA/cm² and 1.488 kA/cm² for each segment.

To accurately characterize the on-chip gain of the amplifier, the grating coupler losses must be known as a function of wavelength. Therefore, reference passive silicon waveguides were placed on the chip, at the top and bottom of the SOA arrays, ensuring that the reference waveguides undergo the same processing as the passive waveguides and grating couplers of the SOAs. The losses of the grating couplers were measured using a Santec TSL-510 tunable laser and a YOKOGAWA AQ6370 optical spectrum analyzer (OSA). To determine the gain of the amplifiers, the output power of the SOA was measured with the OSA in a 1 nm band centered at the input laser wavelength, ensuring that the measured output power was not distorted by amplified spontaneous emission (ASE) [17]. The gain spectrum for 2 dBm waveguide-coupled input power is shown in Fig. 3.18, with pump currents of 114/130 mA (2.878/3.282 kA/cm²) applied to the left side while maintaining 140 mA (2.083 kA/cm²) on the right side. The dip in the gain curves (around

1550 nm) could be attributed to the interference of two propagating modes in the SOA [29], potentially caused by slight misalignment of the transfer-printed SOA or the formation of a Fabry-Perot cavity in the isolation island due to fabrication errors.

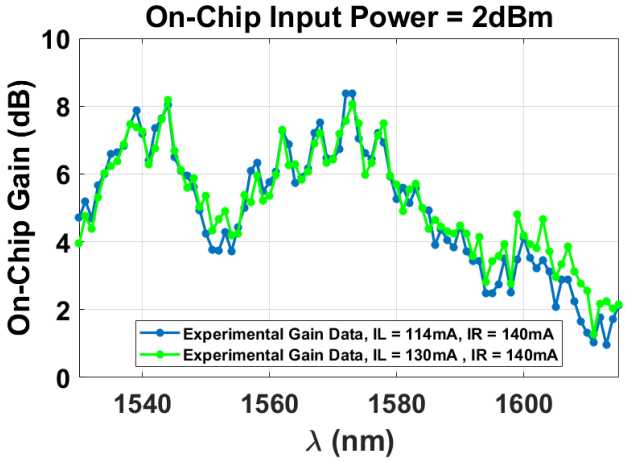



*Figure 3.18: On-chip gain as a function of wavelength, while the waveguide-coupled input power is 2.0 dBm and the pump currents of the left and right sides are 114/130 mA and 140 mA, respectively.*

At wavelengths of 1544 nm and 1573 nm, corresponding to the maximum optical gain for left-side pump currents of 130 mA and 114 mA (Fig. 3.18), the on-chip gain of 8.3 dB and 9.4 dB and output saturation power of 18.4 dBm and 15.4 dBm with the total power consumption of 564 mW and 623 mW, respectively, were extracted by fitting a curve to the experimental data according to Eq. 3.2, as shown in Fig. 3.19 and Fig. 3.20. Although the exact 3-dB saturation level of the SOA was not observed in the experiments while increasing the input optical power, a decrease in the SOA's optical gain of about 2 dB was noted in both cases, confirming the experiment's validity.

$$G(P_{in}) = G_0 \frac{1 + \frac{P_{in}}{P_s}}{1 + \frac{G_0 P_{in}}{P_s}} \tag{3.2}$$

Equation 3.2 relates the SOA gain factor $G$ to the input power $P_{\text{in}}$, material gain saturation power $P_s$, and small-signal gain $G_0$ [17, 26].

A key performance metric for an optical amplifier, particularly in communication applications, is the wall-plug efficiency (WPE). This efficiency is defined as the ratio of the net optical power to the electrical input power and is expressed mathematically as Eq. 3.3 [15, 30]:

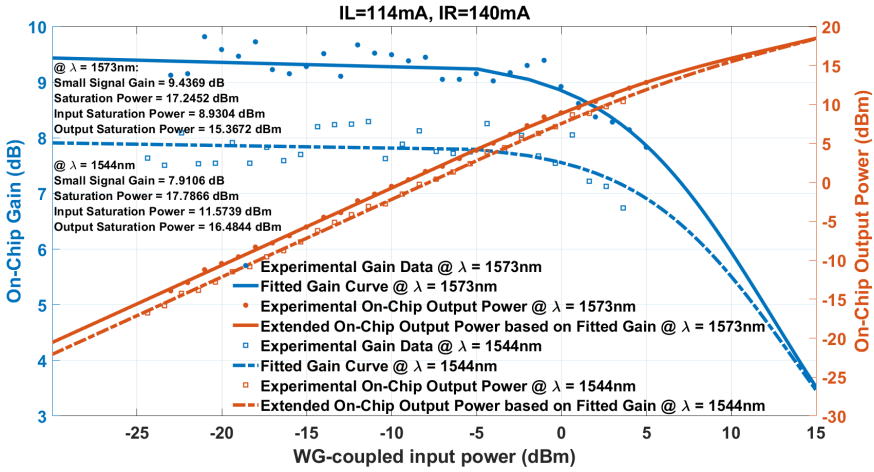



*Figure 3.19: The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves. The pump currents of the left and right sides are 114 mA and 140 mA, respectively.*

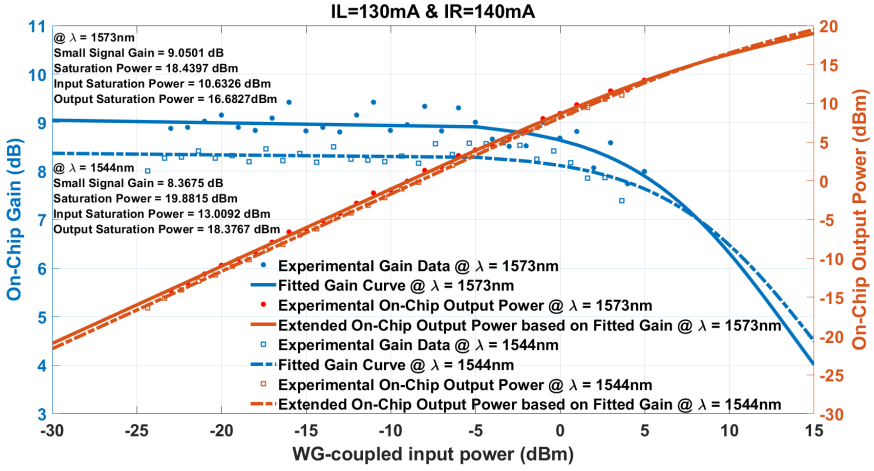



*Figure 3.20: The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves. The pump currents of the left and right sides are 130 mA and 140 mA, respectively.*

$$WPE(\%) = 100 \times \frac{P_{\text{out}} - P_{\text{in}}}{I_{\text{bias}} V_{\text{bias}}} \tag{3.3}$$

We evaluated the WPE at 1544 nm and 1573 nm, using pump currents of

114/130 mA on the left side and 140 mA on the right side, as illustrated in Fig. 3.21.

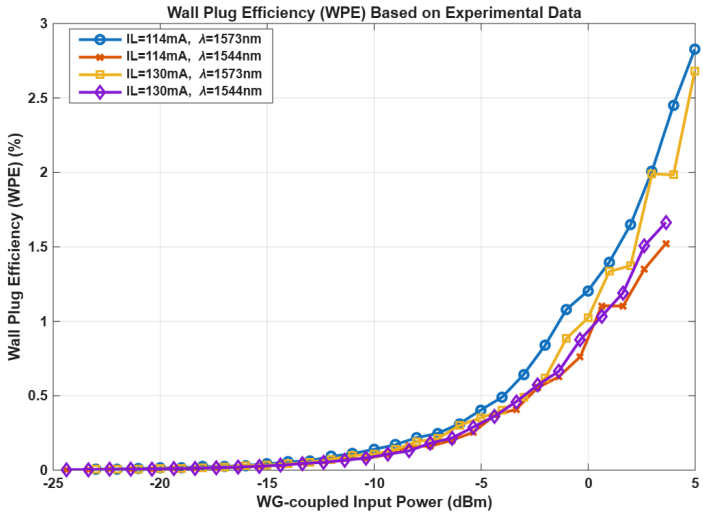



*Figure 3.21: The measured wall-plug efficiency of the SOAs as a function of the on-chip optical input power.*

## 3.5 Conclusion and Future Works

In this work, we proposed a novel tapered design for III-V-on-Si integrated SOAs aimed at increasing the saturation output power. The concept leverages the manipulation of the optical mode distribution and the cross-sectional area of the active region (QWs waveguide). The input optical signal first undergoes amplification in the narrower section of the SOA, resulting in high gain. As the signal progresses through the device, it reaches the wider section, where the lower power density results in higher saturation power. This design has been validated through fabrication and experimental testing.

Although actual saturation was not reached even with input powers as high as 5 dBm, extrapolated performance suggests a saturation power of approximately 19.9 dBm, with input and output saturation power levels around 13 dBm and 18.4 dBm, respectively.

Figure 3.22 presents a comparison of this work against state-of-the-art references [23] and [17], with the latter currently holding the highest reported saturation power for a $\mu$TP-compatible III-V-on-Si SOA. Both reference designs use a fixed cross-section in the III-V-on-Si platform. Reference [17] improves on [23] by reducing the confinement factor and increasing the cross-sectional area, which

leads to enhanced saturation performance. As shown, [17] achieves a higher small-signal gain than both this work and [23], whereas our tapered design demonstrates superior saturation output power while maintaining optical gain as the optical input power increases.

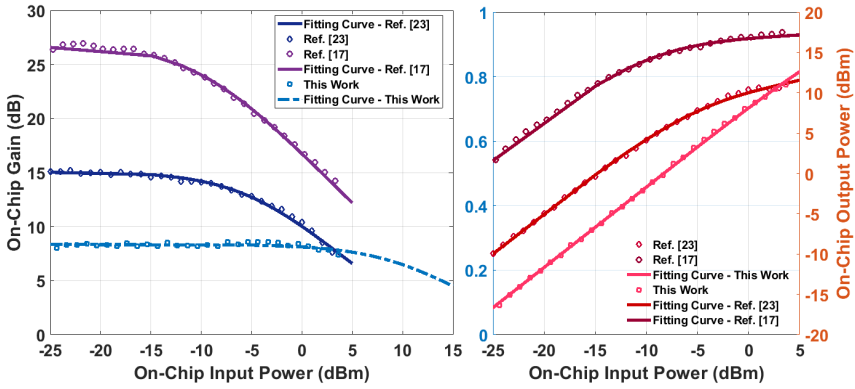



*Figure 3.22: Comparison of this work against state of the art references [17, 23]. The gain as a function of on-chip optical input power (left side). The on-chip output power as a function of the input power (right side). The points are measured values, the lines are fitted curves.*

This trend is consistent with [17]'s approach, where reduced confinement and a larger fixed cross-sectional active area outperform a conventional hybrid waveguide design in terms of saturation power. Table 3.1 summarizes the key performance metrics, small-signal gain, saturation power, input/output saturation power, WPE, power consumption, and footprint.

| **Parameter** | **This Work** | **[17]** | **[23]** |
|---|---|---|---|
| Small Signal Gain (dB) | 8.36 | 27 | 15.13 |
| 1 dB Gain Bandwidth (nm) | ∼30 (est. w/o interferences) | 20 | N.A. (∼20–30) |
| Saturation Power (dBm) | +19.88 | +17.2 | +11.15 |
| Input Sat. Power (dBm) | +13 (calculated) | -9.92 | -3.7 |
| Output Sat. Power (dBm) | +18.37 (calculated) | +14.08 | +8.43 |
| Power Consumption (mW) | 623 | 540 | N.A. (∼330–400) |
| Max. WPE (%) | 2.83 | 10.2 | N.A. |
| Footprint (mm × $\mu$m) | 1.420 × 40 | 1.450 × 40 | 1.350 × 40 |

*Table 3.1: Comparison of Hybrid III-V-on-Si SOAs*

As the Table 3.1 shows, the tapered hybrid design effectively enhances the saturation performance, making it a strong candidate for use as a booster amplifier.

However, one challenge observed in our design is a dip in the gain spectrum, potentially caused by fabrication defects or misalignment during integration,

which could result in mode beating, leading to destructive interference at certain wavelengths. While the exact cause remains unclear, the results highlight the need for precise fabrication and integration in this tapering approach. Notably, even with a 2 $\mu$m wider Si waveguide beneath the III-V layer, intended to improve alignment tolerance, sensitivity to fabrication errors remains significant. However, the use of high-precision integration tools, such as the Amicra Nano Printer with an alignment accuracy of 0.5 $\mu$m, could significantly mitigate these challenges.

In light of these findings, two alternative design strategies for achieving high saturation power in booster amplifiers can be considered:

1. SOA Design Based on Silicon Waveguide Tapering:

   To simplify the simulation, design, and fabrication of SOAs, an alternative approach involves maintaining a fixed III-V active cross-sectional area and varying only the width of the underlying silicon waveguide to control optical mode confinement. However, mode converters, required to enable adiabatic transitions between the silicon and hybrid modes, are not included in Fig. 3.23. This concept, demonstrated in [14], has been shown through numerical analysis to offer improved energy efficiency compared to conventional designs.

   While this method sacrifices one degree of freedom, namely, the ability to further optimize confinement by tapering the III-V structure, it offers several advantages. It simplifies the confinement factor calculations as well as the fabrication, since the III-V layer can be manufactured similarly to standard fixed-geometry designs. Furthermore, a wider III-V region than the tapered silicon waveguide beneath it enhances tolerance to $\mu$TP integration misalignment. However, these benefits come at a cost of the increased average confinement factor across the active region, resulting in a lower saturation power compared to the tapered design introduced in this work.


*Figure 3.23: Schematic illustration of an alternative SOA design utilizing a tapered silicon waveguide. Transitions between the silicon and hybrid waveguides, which are not shown here, are designed to be adiabatic. At the output, the wider silicon waveguide is gradually tapered back to a single-mode waveguide [14].*

2. Coherent Beam Combining SOA Configuration: To maintain the use of conventional $\mu$TP-compatible SOAs for easier fabrication and smoother $\mu$TP

integration, without the need for a separate design solely for boosters, we propose the coherent beam combining SOA configuration, as illustrated in Fig. 3.24.

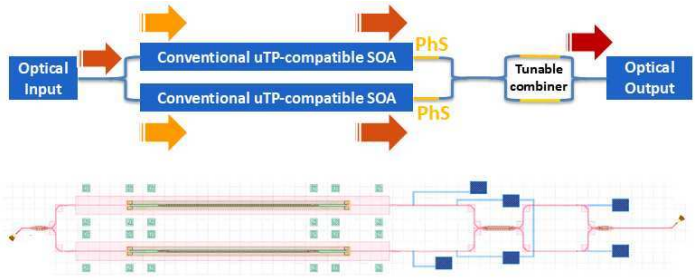



*Figure 3.24: Schematic illustration of the coherent beam combining SOA configuration (top). Screenshot of the GDS layout of the proposed III-V-on-Si integrated circuit (bottom).*

To prevent saturation in a conventional SOA, the input signal is divided into two branches using a 50/50 splitter. Each branch then amplifies the signal, which passes through a heater-based phase section. The signals are then coherently combined using a tunable combiner before being output. By splitting the input signal into two branches, we can utilize conventional SOAs with lower saturation power but higher gain. Coherently combining the outputs of these branches effectively doubles the amplification of the input signal without causing saturation. However, this approach requires at least twice the footprint and involves more complex electrical tuning.

The concept is fabricated on the imec Passives+ platform, as shown in Fig. 3.24. Due to the multiple sections, such as phase shifters, tunable switches, and the SOAs themselves, which require electrical control, the sample is wire-bonded onto a PCB, as depicted in Fig. Future experiments as in Fig. 3.26 are planned to demonstrate this proof of concept.

Footprint can be minimized by integrating two SOAs on a single coupon. This strategy, proposed in [31], simplifies the design by reducing the number of printed elements, effectively halving them, and enables shared biasing through a double-ridge SOA structure. The configuration, implemented on a dual-silicon waveguide platform, is illustrated in Fig. 3.27(a-d).

This integrated tunable laser achieves a waveguide-coupled optical output power of 10 mW (10 dBm) over a tuning range of 51 nm, from 1526 nm to 1577 nm, as presented in Fig. 3.27(e). While it maintains excellent noise and spectral performance, with a relative intensity noise (RIN) as low as –140 dB/Hz and a narrow linewidth of 1.6 kHz (Fig. 3.27(f)), the structure is not optimized for high saturation power. Although 10 mW is sufficient for many use cases, certain applications,

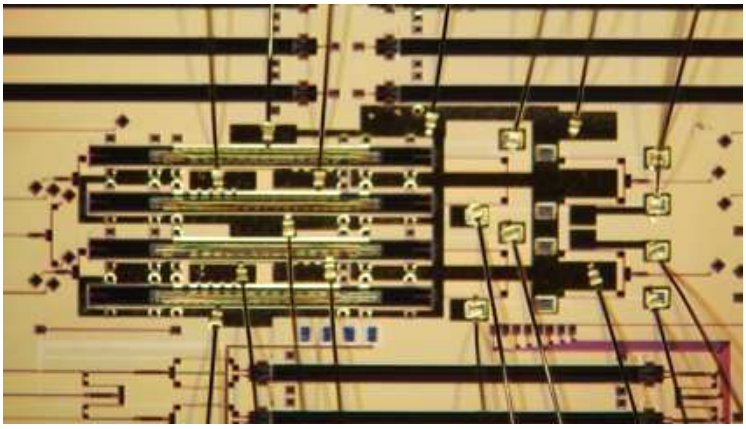


*Figure 3.25: Microscope image of the wire-bonded sample of coherent beam combining SOA configuration to PCB.*

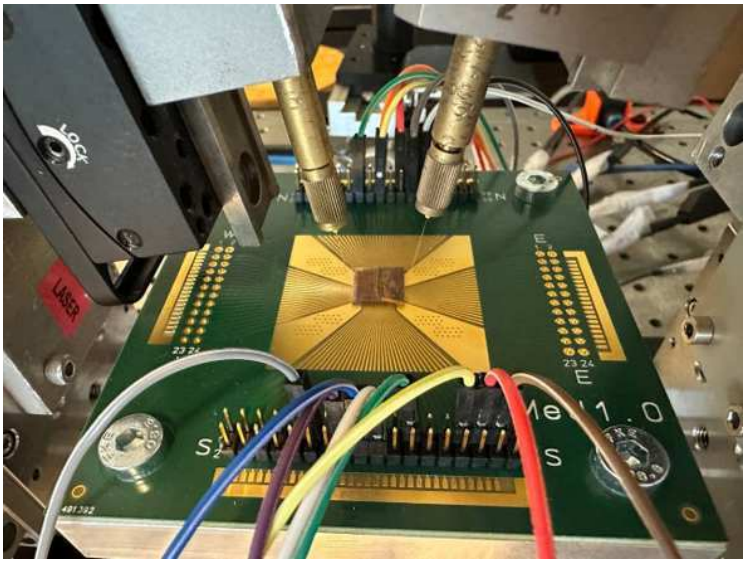



*Figure 3.26: Wire-bonded sample of coherent beam combining SOA configuration to PCB on a measurement setup.*

such as coherent optical communications, may require higher output power levels in the range of 30–50 mW (15–17 dBm).

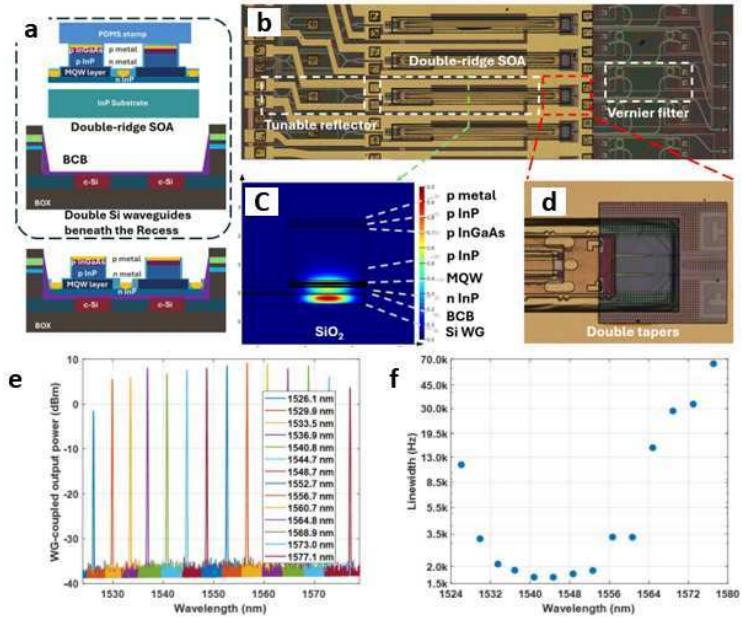



*Figure 3.27: Double-Ridge SOA configuration, providing the laser's gain and booster SOAs into a single encapsulated coupon [31].*

# References

[1] J. C. Hulme, J. K. Doylend, M. J. R. Heck, J. D. Peters, M. L. Davenport, J. T. Bovington, L. A. Coldren, and J. E. Bowers. *Fully integrated hybrid silicon two dimensional beam scanner*. Opt. Express, 23(5):5861–5874, Mar 2015.

[2] Christopher V. Poulton, Ami Yaacobi, David B. Cole, Matthew J. Byrd, Manan Raval, Diedrik Vermeulen, and Michael R. Watts. *Coherent solid-state LIDAR with silicon photonic optical phased arrays*. Opt. Lett., 42(20):4091–4094, Oct 2017.

[3] Jared Hulme, MJ Kennedy, Rui-Lin Chao, Linjun Liang, Tin Komljenovic, Jin-Wei Shi, Bogdan Szafraniec, Doug Baney, and J. E. Bowers. *Fully integrated microwave frequency synthesizer on heterogeneous silicon-III/V*. Opt. Express, 25(3):2422–2431, Feb 2017.

[4] Daryl T. Spencer, Tara Drake, Travis C. Briles, Jordan Stone, Laura C. Sinclair, Connor Fredrick, Qing Li, Daron Westly, B. Robert Ilic, Aaron Bluestone, Nicolas Volet, Tin Komljenovic, Lin Chang, Seung Hoon Lee, Dong Yoon Oh, Myoung-Gyun Suh, Ki Youl Yang, Martin H. P. Pfeiffer, Tobias J. Kippenberg, Erik Norberg, Luke Theogarajan, Kerry Vahala, Nathan R. Newbury, Kartik Srinivasan, John E. Bowers, Scott A. Diddams, and Scott B. Papp. *An optical-frequency synthesizer using integrated photonics*. Nature, 557(7703):81–85, 2018.

[5] Jianping Yao. *Microwave Photonic Systems*. Journal of Lightwave Technology, 40(20):6595–6607, 2022.

[6] Matthew Partridge. *Spectra evolution during coating*. 4 2014.

[7] Hong Deng, Jing Zhang, Emadreza Soltanian, Xiangfeng Chen, Chao Pang, Nicolas Vaissiere, Delphine Neel, Joan Ramirez, Jean Decobert, Nishant Singh, Guy Torfs, Gunther Roelkens, and Wim Bogaerts. *Single-chip silicon photonic engine for analog optical and microwave signals processing*. Nature Communications, 16(1):60100, 2025.

[8] Wim Bogaerts, Yu Zhang, Xiangfeng Chen, Hong Deng, Lukas Van Iseghem, Yichen Liu, Adam Barzanji, Iman Zand, Antonio Ribeiro, Umar Khan, and Najarjun KP. *General-Purpose Programmable Photonic Circuits*. In 2024 IEEE Photonics Society Summer Topicals Meeting Series (SUM), pages 01–02, 2024.

[9] Wim Bogaerts, Hong Deng, Xiangfeng Chen, Lukas Van Iseghem, Iman Zand, Yu Zhang, Yichen Liu, Aladdin Alhaffar, Pierre Edinger, Gaehun Jo,

Alain Yuji Takabayashi, Arun Kumar Mallik, Cleitus Antony, Jing Zhang, Emadreza Soltanian, Peter Verheyen, Jeroen Beeckman, Günther Roelkens, Niels Quack, Frank Niklaus, Kristinn B. Gylfason, and Umar Khan. *Building general-purpose programmable photonic chips: opportunities and challenges*. In Sailing He and Laurent Vivien, editors, Smart Photonic and Optoelectronic Integrated Circuits 2024, volume PC12890, page PC128900T. International Society for Optics and Photonics, SPIE, 2024.

[10] Wu, Yingchen and Huang, Qiangsheng and Keyvaninia, Shahram and Katumba, Andrew and Zhang, Jing and Xie, Weiqiang and Morthier, Geert and He, Jian-Jun and Roelkens, Günther. *All-optical NRZ wavelength conversion based on a single hybrid III-V/Si SOA and optical filtering*. OPTICS EXPRESS, 24(18):20318–20323, 2016.

[11] Gunther Roelkens, Amin Abassi, Paolo Cardile, Utsav Dave, Andreas De Groote, Yannick De Koninck, Sören Dhoore, Xin Fu, Alban Gassenq, Nannicha Hattasan, Qiangsheng Huang, Sulakshna Kumari, Shahram Keyvaninia, Bart Kuyken, Lianyan Li, Pauline Mechet, Muhammad Muneeb, Dorian Sanchez, Haifeng Shao, Thijs Spuesens, Ananth Z. Subramanian, Sarah Uvin, Martijn Tassaert, Kasper Van Gasse, Jochem Verbist, Ruijun Wang, Zhechao Wang, Jing Zhang, Joris Van Campenhout, Xin Yin, Johan Bauwelinck, Geert Morthier, Roel Baets, and Dries Van Thourhout. *III-V-on-Silicon Photonic Devices for Optical Communication and Sensing*. Photonics, 2(3):969–1004, 2015.

[12] Alberto Cordero-Dávila, Rafael Izazaga-Pérez, and Jorge González-García. *Model for frictional forces to reproduce the dragging forces in the polishing process*. In Imaging and Applied Optics Technical Papers, page JTu5A.7. Optica Publishing Group, 2012.

[13] Jing Zhang, Amin Abassi, Andreas De Groote, Ruggero Loi, James O'Callaghan, Brian M Corbett, António José Trindade, Christopher A Bower, and Gunther Roelkens. *Silicon photonic transceiver array based on the transfer printing of III-V O-band photodetectors*. European Conference on Integrated Optics, 2017.

[14] Martijn J. R. Heck. *Energy-efficient semiconductor optical amplifier with longitudinally varying confinement factor*. Opt. Lett., 50(2):301–304, Jan 2025.

[15] Van Gasse, Kasper. *Heterogeneous silicon photonic devices and subsystems for microwave photonics*. PhD thesis, Ghent University, 2019.

[16] Yaxin Zhang, Shen Qiao, Linlin Sun, Qi Wu Shi, Wanxia Huang, Ling Li, and Ziqiang Yang. *Photoinduced active terahertz metamaterials with nanostructured vanadium dioxide film deposited by sol-gel method*. Opt. Express, 22(9):11070–11078, May 2014.

[17] Kasper Van Gasse, Ruijun Wang, and Gunther Roelkens. *27 dB gain III–V-on-silicon semiconductor optical amplifier with ¿ 17 dBm output power*. Opt. Express, 27(1):293–302, Jan 2019.

[18] Paul W. Juodawlkis, Jason J. Plant, William Loh, Leo J. Missaggia, Frederick J. O'Donnell, Douglas C. Oakley, Antonio Napoleone, Jonathan Klamkin, Juliet T. Gopinath, Daniel J. Ripin, Sangyoun Gee, Peter J. Delfyett, and Joseph P. Donnelly. *High-Power, Low-Noise 1.5-/mum Slab-Coupled Optical Waveguide (SCOW) Emitters: Physics, Devices, and Applications*. IEEE Journal of Selected Topics in Quantum Electronics, 17(6):1698–1714, 2011.

[19] K. Morito, S. Tanaka, S. Tomabechi, and A. Kuramata. *A broad-band MQW semiconductor optical amplifier with high saturation output power and low noise figure*. IEEE Photonics Technology Letters, 17(5):974–976, 2005.

[20] Meint Smit, Xaveer Leijtens, Huub Ambrosius, Erwin Bente, Jos van der Tol, Barry Smalbrugge, Tjibbe de Vries, Erik-Jan Geluk, Jeroen Bolk, Rene van Veldhoven, Luc Augustin, Peter Thijs, Domenico D'Agostino, Hadi Rabbani, Katarzyna Lawniczuk, Stanislaw Stopinski, Saeed Tahvili, Antonio Corradi, Emil Kleijn, Dzmitry Dzibrou, Manuela Felicetti, Elton Bitincka, Valentina Moskalenko, Jing Zhao, Rui Santos, Giovanni Gilardi, Weiming Yao, Kevin Williams, Patty Stabile, Piet Kuindersma, Josselin Pello, Srivathsa Bhat, Yuqing Jiao, Dominik Heiss, Gunther Roelkens, Mike Wale, Paul Firth, Francisco Soares, Norbert Grote, Martin Schell, Helene Debregeas, Mohand Achouche, Jean-Louis Gentner, Arjen Bakker, Twan Korthorst, Dominic Gallagher, Andrew Dabbs, Andrea Melloni, Francesco Morichetti, Daniele Melati, Adrian Wonfor, Richard Penty, Ronald Broeke, Bob Musk, and Dave Robbins. *An introduction to InP-based generic integration technology*. Semiconductor Science and Technology, 29(8):083001, jun 2014.

[21] Francisco M. Soares, Moritz Baier, Tom Gaertner, Mike Feyer, Martin Möhrle, N. Grote, and M. Schell. *High-Performance InP PIC Technology Development based on a Generic Photonic Integration Foundry*. In 2018 Optical Fiber Communications Conference and Exposition (OFC), pages 1–3, 2018.

[22] Kasper Van Gasse, Ruijun Wang, and Gunther Roelkens. *High-Power III-V-on-Silicon Semiconductor Optical Amplifier (> 50 mW) for Integrated Mode-Locked Lasers*. In 2019 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC), pages 1–1, 2019.

[23] Bahawal Haq, Sulakshna Kumari, Kasper Van Gasse, Jing Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, and Gunther Roelkens. *Micro-Transfer-Printed III-V-on-Silicon C-Band Semiconductor Optical Amplifiers*. Laser & Photonics Reviews, 14(7):1900364, 2020.

[24] Jing Zhang, Laurens Bogaert, Clemens Krückel, Emadreza Soltanian, Hong Deng, Bahawal Haq, Johanna Rimböck, Joris Van Kerrebrouck, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Peter Ossieur, Dries Van Thourhout, Geert Morthier, Wim Bogaerts, and Gunther Roelkens. *Micro-transfer printing InP C-band SOAs on advanced silicon photonics platform for lossless MZI switch fabrics and high-speed integrated transmitters*. Opt. Express, 31(26):42807–42821, Dec 2023.

[25] Emadreza Soltanian, Grigorij Muliuk, Sarah Uvin, Dongbo Wang, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Stefan Ertl, Johanna Rimböck, Nicolas Vaissiere, Delphine Néel, Joan Ramirez, Jean Decobert, Bart Kuyken, Jing Zhang, and Gunther Roelkens. *Micro-transfer-printed narrow-linewidth III-V-on-Si double laser structure with a combined 110 nm tuning range*. Opt. Express, 30(22):39329–39339, Oct 2022.

[26] Michael L. Davenport, Sandra Skendžić, Nicolas Volet, Jared C. Hulme, Martijn J. R. Heck, and John E. Bowers. *Heterogeneous Silicon/III–V Semiconductor Optical Amplifiers*. IEEE Journal of Selected Topics in Quantum Electronics, 22(6):78–88, 2016.

[27] Peter Kaspar, Guilhem de Valicourt, Romain Brenot, Miquel A. Mestre, Philippe Jennevé, Alain Accard, Dalila Make, François Lelarge, Guang-Hua Duan, Nicola Pavarelli, Marc Rensing, Cormac Eason, Peter O'Brien, Ségolène Olivier, Stéphane Malhouitre, Christophe Kopp, Chirstophe Jany, and Sylvie Menezo. *Hybrid III-V/Silicon SOA in Optical Network Based on Advanced Modulation Formats*. IEEE Photonics Technology Letters, 27(22):2383–2386, 2015.

[28] D. Vermeulen, Y. De Koninck, Y. Li, E. Lambert, W. Bogaerts, R. Baets, and G. Roelkens. *Reflectionless grating couplers for Silicon-on-Insulator photonic integrated circuits*. Opt. Express, 20(20):22278–22283, Sep 2012.

[29] Michael L Davenport, Sandra Skendžić, Nicolas Volet, Jared C Hulme, Martijn JR Heck, and John E Bowers. *Heterogeneous silicon/III–V semiconductor optical amplifiers*. IEEE Journal of Selected Topics in Quantum Electronics, 22(6):78–88, 2016.

[30] Stanley Cheung, Yasumasa Kawakita, Kuanping Shang, and S. J. Ben Yoo. *Theory and Design Optimization of Energy-Efficient Hydrophobic Wafer-bonded III–V/Si Hybrid Semiconductor Optical Amplifiers*. J. Lightwave Technol., 31(24):4057–4066, Dec 2013.

[31] Yang Liu, Ye Chen, Laurens Bogaert, Emadreza Soltanian, Evangelia Delli, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Geert Morthier, Gunther Roelkens, and Jing Zhang. *Widely tunable narrow-linewidth lasers with booster amplification on silicon photonics*. Opt. Express, 33(10):22078–22086, May 2025.

# 4

# Towards Wafer Scale $\mu$TP Integration

This chapter is organized into four sections as follows:

- Introduction (4.1): This section presents the motivation for scaling up micro-transfer printing ($\mu$TP) technology from chip-level demonstrations to wafer-scale integration. It highlights the technological and ecosystem challenges that must be addressed to enable $\mu$TP as a scalable and manufacturable solution. The section also discusses the importance of standardization and the ongoing efforts within European initiatives to establish a sustainable $\mu$TP ecosystem.

- Essential Tools and Processes for Wafer-Scale $\mu$TP Integration (4.2): This section introduces two critical enablers for wafer-scale $\mu$TP: the spray coating process for adhesive bonding layers (e.g., BCB) and the micro-transfer printing tool itself. These tools form the technological backbone of the $\mu$TP pilot line and are essential for achieving a high-yield integration process.

- Initial Demonstration of Wafer-Scale $\mu$TP (4.3): In this section, we describe the first steps in wafer-scale $\mu$TP. This includes achieving uniform BCB spray coating over planar wafers and the first demonstration of wafer-scale integration of III–V active components on a SiPh wafer, carried out at the TRANSVERSE pilot-line.

- Conclusion and Future Work (4.4): This section summarizes the key contributions of the chapter and outlines future directions for yield optimization,

standardization, reliability testing, and expansion of $\mu$TP integration capabilities toward industrial-scale deployment.

## 4.1 Introduction

The previous chapters in this thesis have demonstrated the functional viability and performance of heterogeneous photonic active components such as narrow-linewidth tunable lasers and semiconductor optical amplifiers (SOAs), as well as numerous application-driven demonstrators enabled by micro-transfer printing ($\mu$TP). In parallel, significant advancements by the Photonics Research Group (PRG) have showcased numerous type of lasers [1, 2], photodiodes [1, 2], Lithium Niobate (LN) based modulators [1–3], and other critical photonic building blocks, collectively confirming the potential of $\mu$TP to complement and enhance the capabilities of silicon photonics (SiPh) platforms. These accomplishments clearly establish the readiness of $\mu$TP for more than proof-of-concept experimentation, signaling a timely need to shift focus toward scalable integration and industrialization. To make this transition, the next frontier lies in enabling wafer-scale micro-transfer printing, as shown in Fig. 4.1. Wafer-scale capabilities will not only simplify the integration of III-V and other active materials on silicon, but also allow for efficient and repeatable processing compatible with foundry workflows. This shift is aligned with the goal of progressing from Technology Readiness Level (TRL) 3–4, where $\mu$TP-based devices have been validated in a lab setting, to TRL 6–7, where reliable, reproducible, and scalable integration becomes feasible. Future work will include reliability testing, essential for qualification.

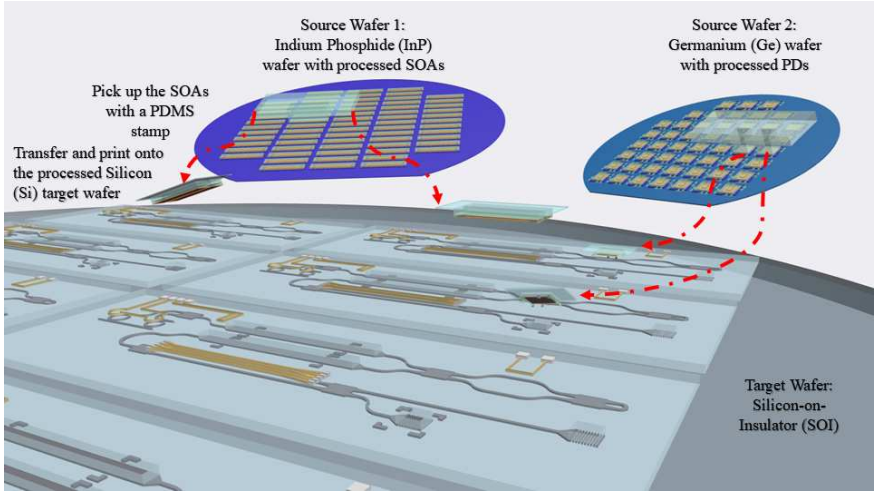



*Figure 4.1: Wafer-scale $\mu$TP integration schematic.*

Realizing this vision requires more than scaling equipment and processes, it demands the establishment of a complete $\mu$TP ecosystem. This includes coordination across source wafer providers, transfer-printing pilot lines, and target wafer manufacturers. Furthermore, there is a pressing need for standardization such as optical and electrical interfaces, coupon dimensions and layouts, test structures for process control monitoring (PCM), and electrical/optical probing and packaging. Without such harmonization, widespread interoperability across vendors and platforms remains difficult. These challenges are already being addressed through collaborative European initiatives like PhotonixFAB [4] (Fig. 4.2), which aims to accelerate the industrial uptake of advanced photonic integration technologies. Within this context, imec plays a pivotal role in both R&D and the technology transfer of $\mu$TP processes to industrial foundries such as XFAB [5]. Integration on 200 mm wafers and alignment with established platforms like iSiPP50G/iSiPP200 are pursued. On the other hand, SMART PHOTONICS [6] is developing InP-based coupon fabrication and the TRANSVERSE group [7] is actively establishing a pilot line for wafer-scale $\mu$TP integration, enabling and supporting the development of $\mu$TP components as part of future process design kits (PDKs). Such PDKs will define not only the building blocks but also the design rules (DRCs) necessary to ensure robust integration into SiPh circuits. The goal is to make $\mu$TP components as easy to use in design environments as existing SiPh elements, bridging the gap between heterogeneous integration and EDA-compatible design workflows, developed by Luceda Photonics [8]. This chapter presents the initial steps taken toward this goal.

## 4.2 Essential Tools and Processes for Wafer-Scale $\mu$TP Integration

To realize wafer-scale micro-transfer printing ($\mu$TP) integration, all backend processes, from backend opening of the SiPh wafers to coating of adhesive bonding layer, $\mu$TP, and metallization, must support full wafer formats. Among these steps, two tools are particularly essential to enable scalable $\mu$TP: the spray coater for uniform adhesive deposition and the $\mu$TP printer for precise transfer of optoelectronic chips. These tools are key assets within the TRANSVERSE integration pilot line.

### 4.2.1 Spray Coater – EVG®101

The EVG®101 spray coater [9] shown in Fig. 4.3 is the primary tool used in TRANSVERSE for depositing thin and uniform films of BCB (benzocyclobutene), serving as the adhesive bonding layer for $\mu$TP integration. Although the tool can also handle photoresist spraying for lithography, this thesis focuses solely on its application for BCB coating.

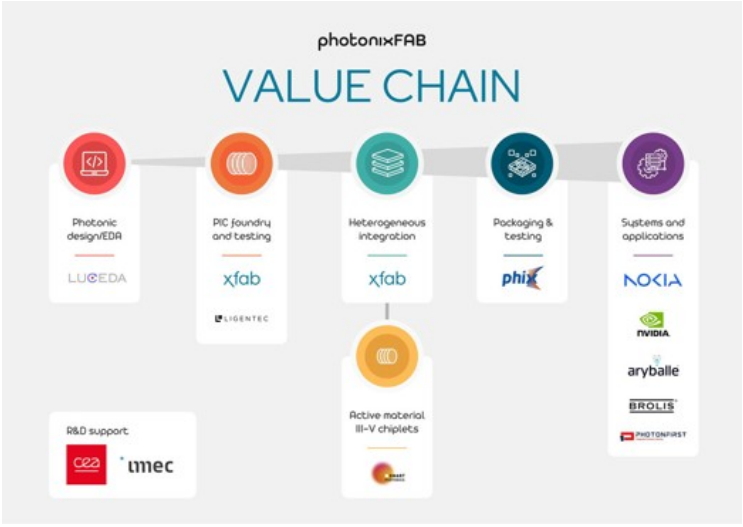



*Figure 4.2: PhotonixFAB value chain, to establish a European photonics device value chain and initial industrial manufacturing capabilities, providing a path to scalable high-volume manufacturing for innovative product developers [4].*

Key Specifications:

- Wafer size compatibility: up to 200 mm.
- Process materials: BCB (adhesive), photoresists.
- Coating method: ultrasonic nozzle programmable spray system.

A core advantage of the EVG®101 is its compatibility with wafers that contain topographical features, such as $\mu$TP trenches. Unlike spin coating, which suffers from poor step coverage over recessed or patterned areas, spray coating offers excellent conformity, making it the method of choice for reliable adhesive preparation prior to $\mu$TP.

The EVG®101 uses an ultrasonic nozzle mounted on a programmable gantry arm. The arm traverses the wafer in a meander motion, as shown in Fig. 4.4. The distance between the nozzles and the wafer, along with the movement speed and dispense rate, is carefully controlled to deposit a uniform adhesive layer.

The tool's programmable parameters include:

- Traverse speed of the gantry (known as line speed)
- Dispense rate from the nozzle
- Scan pitch (known as linefeed distance, which is the distance between adjacent spray lines)


*Figure 4.3: EVG®101 spray coater installed at Ghent University cleanroom for wafer-scale thin-film BCB deposition.*

- Start/stop timing delays at wafer edges
- Edge Overshoot (the start/stop point of spraying as a distance before/after the wafer edges)
- Vertical Distance (between the nozzle and the wafer)

By tuning these variables, BCB layers can be deposited with precise target thicknesses tailored for subsequent $\mu$TP steps. This is especially critical for integration

across $\mu$TP trenches, where maintaining thickness uniformity and surface flatness is crucial for successful printing and bonding, ensuring proper evanescent coupling between the coupon and the target waveguide.

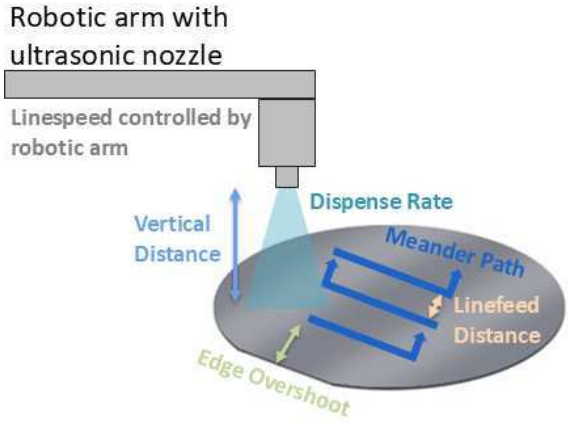



*Figure 4.4: Spray coating scheme, mentioning the important controllable parameters of EVG101.*

### 4.2.2 $\mu$TP Printer – ASMPT Amicra NANO

The ASMPT Amicra NANO [10] as shown in Fig. 4.5 at TRANSVERSE is a high-precision printer customized specifically for $\mu$TP processes. It enables the accurate and repeatable transfer of micro-devices from a source wafer to a target wafer, across full wafer scales.

The $\mu$TP printer comprises three main functional parts as shown in Fig. 4.6:

- Source wafer chuck: holds III-V or other source wafers with coupon arrays.
- Target wafer chuck: accommodates wafers from 100 mm to 300 mm, including SiPh, SiN, or LN platforms.
- Transfer head: features a magnetic holder for PDMS stamps and handles pick-up and placement of the coupons with sub-micron accuracy.

Tool Capabilities:

- Alignment precision: ±0.5 $\mu$m ($3\sigma$) across large areas.
- Z-axis overdrive control: ensures optimal bonding pressure and minimizes BCB layer compression variability.


*Figure 4.5: ASMPT Amicra Nano printer installed at Ghent University Cleanroom for wafer-scale $\mu$TP.*

- Flexible chuck support: accommodates different wafer sizes for both source and target.

The transfer head movement is fully automated using precise image processing controls and optimized for rapid, reliable coupon transfer across a full wafer. Combined with the uniform BCB layer provided by the spray coater, the Amicra NANO ensures high-yield, wafer-scale $\mu$TP integration suitable for scaling up heterogeneous SiPh integration.

## 4.3 Initial Demonstration of Wafer-Scale $\mu$TP

The quality of the intermediate BCB bonding layer has a significant impact on the success of the $\mu$TP process. Specifically, its surface smoothness and thickness uniformity directly affect the printing yield and optical coupling efficiency between

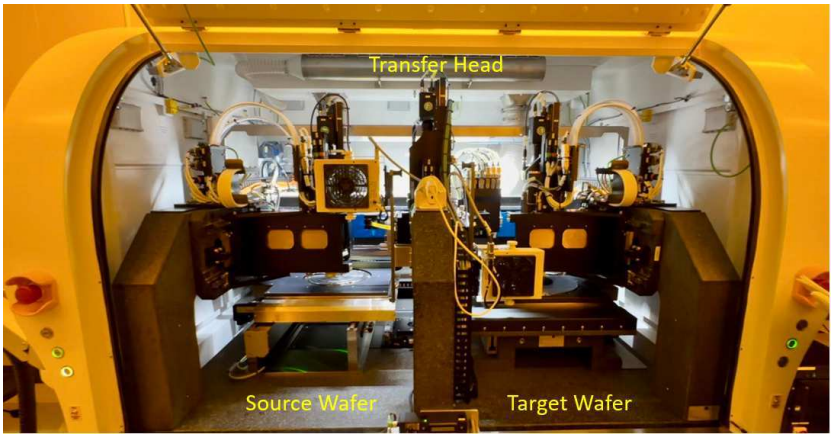



*Figure 4.6: ASMPT Amicra Nano printer with opened door showing source chuck, target chuck, and the transfer head*

the transferred coupon and the target waveguide. In particular, the thickness of the BCB layer plays a critical role in enabling efficient evanescent optical coupling, which is sensitive to variations in vertical alignment. These acceptable limits can be defined by optical simulations of evanescent coupling between the III-V coupon and the target waveguide tapers, as a function of BCB thickness. To address these constraints, we aim to precisely control the BCB spray coating over full planar wafers. The goal is to achieve minimal thickness non-uniformity while keeping the BCB thickness within the range dictated by optical coupling requirements. This section outlines the first steps toward building this infrastructure and optimizing the $\mu$TP platform for scalable wafer-level integration. Finally, we present results from the first wafer-scale $\mu$TP integration of III-V coupons on a SiPh wafer, achieved as part of the TRANSVERSE team effort. This milestone demonstrates the viability of wafer-scale $\mu$TP integration and serves as a proof of concept for future pilot-line developments. This subsection is structured as follows:

- BCB Spray Coating Optimization on Blank Si Wafers (4.3.1): Optimization of spray coating parameters on blank Si wafers to produce smooth, uniform BCB films with target thickness.

- Demonstration of Wafer-Scale $\mu$TP of IIIV on Si (4.3.2): Demonstration of the first wafer-scale $\mu$TP integration, transferring pre-fabricated III-V SOA coupons onto a Si wafer.

### 4.3.1 BCB Spray Coating Optimization on Blank Si Wafers

Establishing standardized, repeatable spray-coating process recipes on blank wafers is a foundational requirement for any wafer-scale integration line. These standard recipes not only enable reliable control of the desired BCB thickness and uniformity, but also serve as a baseline to monitor the overall health and consistency of the spray coating process and tool, even when the final target wafers contain complex photonic layouts with trenches and other features. To this end, TRANSVERSE focused on developing robust standard operating procedures for BCB spray coating. These include:

- Pre-cleaning steps for both the wafer and spray coater tool, such as the chuck and chemical injection lines to the nozzle.
- Preparation of the BCB solution, including controlled dilution with mesitylene to tune the final film thickness.
- Choosing between the spray nozzle heads of wide angle and focused appropriate for the target thickness and uniformity.
- Optimization of key spray parameters shown in Fig. 4.4, such as linefeed distance, dispense rate, and linespeed, to achieve predictable and controllable film properties.
- Post-bake conditions, including temperature, timing, and whether the bake is performed on the tool chuck, hotplate, or a combination of both.

Even though the end goal is often to coat wafers with $\mu$TP trenches, all recipes are first to be validated on blank Si wafers to provide a controlled environment for benchmarking and troubleshooting.

In general, a trade-off exists between BCB thickness and film uniformity. Thinner BCB coatings tend to exhibit higher non-uniformity, making them more sensitive to process fluctuations. Each dilution ratio of BCB:Mesitylene corresponds to a specific window of achievable thicknesses with acceptable uniformity, provided the spray parameters are also well-tuned. To streamline this, TRANSVERSE created a lookup table mapping dilution ratios to expected thickness ranges and optimized spray conditions. When thicker BCB layers are required, two main strategies are possible: either using a less diluted BCB solution or applying multiple spray passes on the same wafer. Of the two, the first approach is generally preferred due to better control over uniformity and fewer complications in post-processing, as illustrated in Fig. 4.7.

Process factors, such as line speed, linefeed distance, dispense rate, edge overshoot, and post-bake behavior, also impact coating results. These were carefully optimized to ensure uniform coating on the wafer, depending on the desired BCB thickness.


*Figure 4.7: (Left) 1st layer of 100 nm BCB spray coated on a blank Si wafer, (Middle) 2nd layer of 100 nm BCB spray coated on the same wafer to reach 200 nm of BCB in total. (Right) One time of spray coating less diluted BCB on a blank Si wafer to reach 200 nm of thickness.*

### 4.3.2 Demonstration of Wafer-Scale $\mu$TP of IIIV on Si

To demonstrate the scalability and alignment precision of $\mu$TP for III-V devices onto SiPh wafers, a wafer-scale printing trial was carried out using the customized Amicra NANO printer. In this demonstration, pre-fabricated InP-based coupons were sourced from a 3-inch epitaxial III-V wafer. These coupons were printed onto a quarter section of a 200 mm Si target wafer, fabricated using the imec Si-400 nm platform. Each reticle on the wafer included blocks of devices such as Fabry–Pérot (FP) lasers and semiconductor optical amplifiers (SOAs), with each functional block containing an array of eight $\mu$TP sites planarized. Figure 4.8 shows the full layout view of the 200 mm SiPh wafer, including a zoomed-in view of a representative reticle where $\mu$TP integration was performed. Each block in the reticle is composed of standardized SOA/FP laser circuit building blocks defined in the $\mu$TP-PDK, with tunable design parameters such as cavity length, coupon length, bend radius, and directional coupler splitting ratio for either C-band or O-band. Prior to $\mu$TP, the wafer underwent spray-coating of an 80 nm BCB bonding layer, optimized for evanescent optical coupling.

Figure 4.9 illustrates the uniform placement of coupons and the successful integration of InP dies across the $\mu$TP sites of SOA and laser blocks, demonstrating the feasibility of wafer-scale $\mu$TP for scalable hybrid photonic integration.

The III-V coupons featured metallized alignment markers, enhancing image contrast and recognition for the vision-based alignment algorithm of the printing tool. This approach significantly improved image processing accuracy, and consequently, the lateral placement precision. In total, 128 coupons were successfully transfer-printed automatically across a quarter of the Si wafer. The process was carried out using single-coupon transfer printing per integration cycle, with an average cycle time of approximately 30 seconds, measured from picking to printing, including stamp cleaning before the next cycle. This cycle time was further optimized to as low as 7 seconds per cycle by refining the shear-force sub-steps, both lateral and vertical, and by implementing conditional stamp cleaning only when

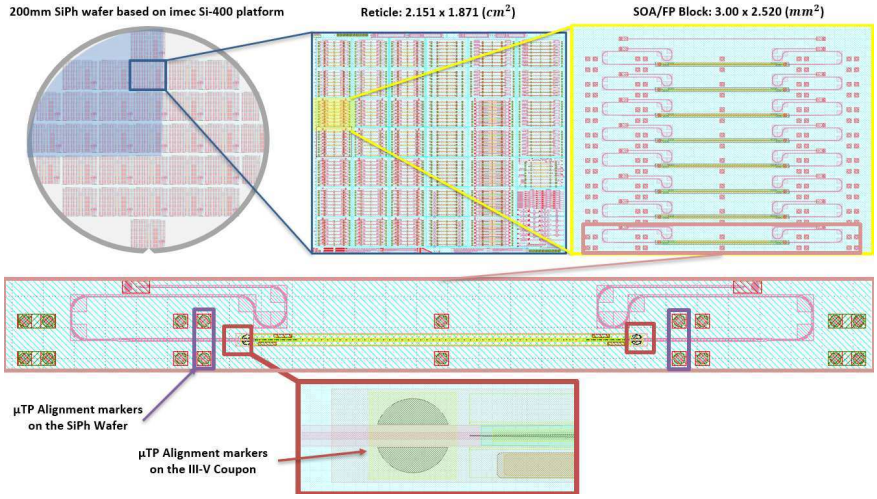



*Figure 4.8: Full layout of the 200 mm SiPh wafer, highlighting a zoomed-in view of a representative reticle used for $\mu$TP integration. Each block within the reticle consists of standardized SOA/FP laser building blocks from the $\mu$TP-PDK, featuring tunable design parameters such as cavity and coupon lengths, waveguide bend radius, and directional coupler splitting ratio, configurable for both C-band and O-band operation.*

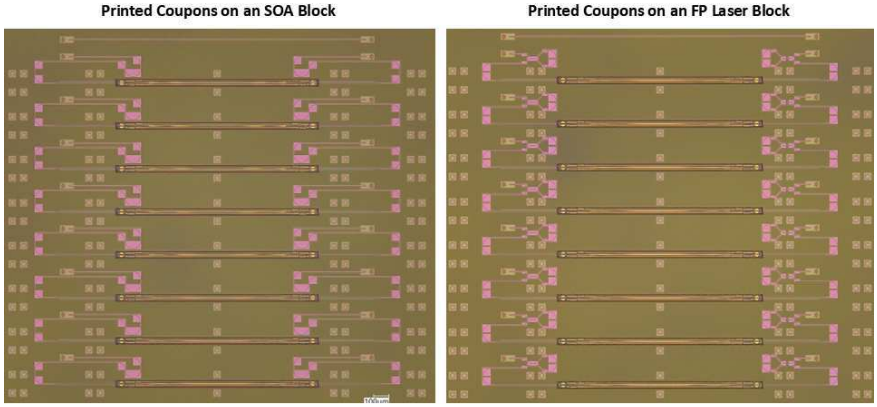



*Figure 4.9: Printed coupons on the SOA (left) and FP laser (right) blocks using wafer-scale printer.*

necessary. The printing process relied on the setup of wafer maps, reticle maps, and image-processing jobs (IP-jobs), enabling the system to detect, pick, and place the coupons accurately onto the designated $\mu$TP sites.

This method resulted in an overall printing yield of 100%, with no observed failures. A statistical analysis of lateral alignment error showed a mean misalign-

ment of 0.256 $\mu$m and a 3$\sigma$ deviation of 0.283 $\mu$m, confirming the deep sub-micron placement accuracy of the $\mu$TP process. Further improvements in IP job optimization and system calibration could help reduce the mean offset toward zero. The 3D optical microscope reconstruction shown in Fig. 4.10 further confirms the surface topology integrity of the printed coupons and surrounding photonic structures, verifying high-fidelity transfer and accurate alignment.

To evaluate the alignment accuracy in more detail, two approaches can be considered. In principle, the Amicra Nano printer IP jobs rely on image processing of both $\mu$TP alignment markers patterned on the Si target wafer and those fabricated on the III-V coupons. These markers are detected twice: first during the alignment phase before printing, and again after the bonding phase once the coupon has been placed. By comparing the intended placement coordinates (from pre-bonding detection) with the actual position (from post-bonding detection), an error-correction coefficient can be extracted. This coefficient can then be applied in subsequent IP jobs to introduce a corrective shift in the placement, thereby reducing misalignment between the III-V coupon and the Si waveguide. However, this error-correction method was not employed in the present demonstration.

Instead, the alignment accuracy was validated using a Critical Dimension (CD) measurement instrument after printing was completed. In this case, the CD tool does not rely on $\mu$TP markers but rather on edge detection: the edge lines of the Si rib waveguide and the taper tip of the SOA are identified, the geometric centers of both features are calculated, and the lateral offset between them is extracted as the misalignment, as shown in Fig. 4.11. The statistical results reported above are based on this CD measurement method, confirming the high alignment precision achieved in this demonstration.

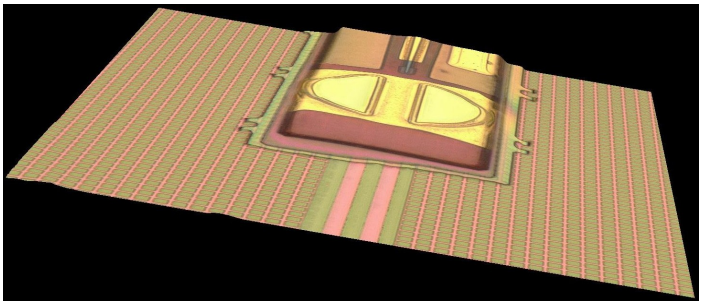


*Figure 4.10: The 3D optical microscope reconstruction of an InP SOA coupon printed on a Si waveguide using a wafer-scale printer, showing the sub-micron alignment precision.*

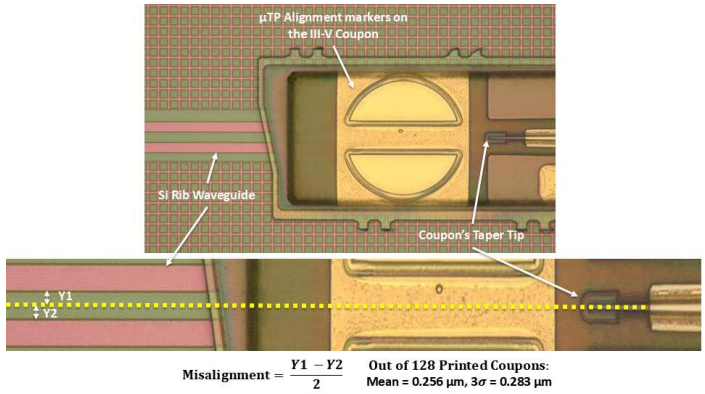



*Figure 4.11: Implementation of metallized donut-shape $\mu$TP alignment markers on the coupons to ensure high alignment precision. A zoomed-in view, illustrating the way of lateral misalignment measurement.*

## 4.4 Conclusion and Future Work

In this chapter, we have outlined the foundational steps toward enabling wafer-scale micro-transfer printing ($\mu$TP) as a scalable and reliable integration technology for heterogeneous photonic integrated circuits. Building on the successful proof-of-concept demonstrations presented in earlier chapters, and complemented by achievements from the broader Photonics Research Group (PRG), this work shifts the focus from feasibility to manufacturability, process standardization, and ecosystem development. The demonstrated experiments involving spray coating of BCB bonding layers and wafer-scae $\mu$TP forms the basis for high yield $\mu$TP. The chapter situates these developments within a broader European industrialization effort, specifically the PhotonixFAB initiative, where imec and PRG-TRANSVERSE play key roles in technology transfer, R&D support, and the setup of a wafer-scale $\mu$TP pilot line. These activities are intended to bridge the current gap between TRL 3–4 academic prototypes and TRL 6–7 industrial solutions, accelerating the path toward commercial adoption.

As future work, several parallel development tracks are essential:

- Yield Optimization: Further investigation is required to quantify and enhance the yield at every stage of the $\mu$TP process, device fabrication, release, pick-up, and printing. Particular attention will be paid to minimizing void formation at bonding interfaces and ensuring sub-micron alignment accuracy.

- Standardization and PDK Development: Efforts are needed to formalize optical and electrical interface standards, coupon dimensions, and DRC-

compatible layout rules. The aim is to enable seamless integration of $\mu$TP components into existing SiPh platforms such as iSiPP50G, and iSiPP200.

- Reliability Assessment: Long-term reliability studies, including thermal cycling, damp-heat testing, high-temperature operating life (HTOL) testing, and accelerated aging, will be initiated to validate $\mu$TP's readiness for commercial applications.
- Expanding Functional Scope: While the current focus remains on active photonic components, future directions include the transfer printing of e.g. electronic ICs.
- Industrialization and Scale-Up: Continued collaboration with industrial partners such as XFAB will be vital to scale the $\mu$TP pilot line into a robust, repeatable, and high-volume process line.

Altogether, these efforts aim not only to mature $\mu$TP into a manufacturing-grade technology but also to democratize access. The eventual vision is a heterogeneous photonic ecosystem where $\mu$TP components are as accessible and trusted as conventional building blocks, unlocking new levels of flexibility and functionality in integrated photonics.

# References

[1] Gunther Roelkens, Jing Zhang, Laurens Bogaert, Emadreza Soltanian, Maximilien Billet, Ali Uzun, Biwei Pan, Yang Liu, Evangelia Delli, Dongbo Wang, Valeria Bonito Oliva, Lam Thi Ngoc Tran, Xin Guo, He Li, Senbiao Qin, Konstantinos Akritidis, Ye Chen, Yu Xue, Margot Niels, Dennis Maes, Max Kiewiet, Tom Reep, Tom Vanackere, Tom Vandekerckhove, Isaac Luntadila Lufungula, Jasper De Witte, Luis Reis, Stijn Poelman, Ying Tan, Hong Deng, Wim Bogaerts, Geert Morthier, Dries Van Thourhout, and Bart Kuyken. *Present and future of micro-transfer printing for heterogeneous photonic integrated circuits*. APL Photonics, 9(1):010901, 01 2024.

[2] Gunther Roelkens, Jing Zhang, Laurens Bogaert, Maximilien Billet, Dongbo Wang, Biwei Pan, Clemens J. Kruckel, Emadreza Soltanian, Dennis Maes, Tom Vanackere, Tom Vandekerckhove, Stijn Cuyvers, Jasper De Witte, Isaac Luntadila Lufungula, Xin Guo, He Li, Senbiao Qin, Grigorij Muliuk, Sarah Uvin, Bahawal Haq, Camiel Op de Beeck, Jeroen Goyvaerts, Guy Lepage, Peter Verheyen, Joris Van Campenhout, Geert Morthier, Bart Kuyken, Dries Van Thourhout, and Roel Baets. *Micro-Transfer Printing for Heterogeneous Si Photonic Integrated Circuits*. IEEE Journal of Selected Topics in Quantum Electronics, 29(3: Photon. Elec. Co-Inte. and Adv. Trans. Print.):1–14, 2023.

[3] Margot Niels, Tom Vanackere, Tom Vandekerckhove, Stijn Poelman, Tom Reep, Günther Roelkens, Maximilien Billet, and Bart Kuyken. *Centimetre-scale micro-transfer printing to enable heterogeneous integration of thin film lithium niobate with silicon photonics*. Opt. Mater. Express, 15(3):531–540, Mar 2025.

[4] PhotonixFAB Consortium. *PhotonixFAB - Enabling a Sovereign European Industrial Silicon Photonics Value Chain*, 2025. Accessed: 2025-08-13.

[5] X-FAB Silicon Foundries. *X-FAB Leads EU-funded Consortium to Industrialize the European Silicon Photonics Value Chain*. `https://tinyurl.com/42xnndb5`, June 2023. Accessed: 2025-08-15.

[6] SMART Photonics. *SMART Photonics - Foundry for Photonic Integrated Circuits*. `https://smartphotonics.nl/`, 2025. Accessed: 2025-08-15.

[7] imec and Ghent University. *Transverse Technology – Pilot Line for Wafer-Scale Micro-Transfer Printing*, 2025. Accessed: 2025-08-13.

[8] Luceda Photonics. *Luceda Photonics – Photonic IC Design Software*, 2025. Accessed: 2025-08-13.

[9] EV Group. *EVG®101 Advanced Resist Processing System*, 2025. Accessed: 2025-08-13.

[10] ASMPT AMICRA. *AMICRA NANO – Ultra-High Precision Die Bonder and Flip Chip Bonder*, 2025. Accessed: 2025-08-13.

# 5
# Conclusion and Outlook

This thesis focused on the development of ultra-wide tunable and narrow-linewidth III–V-on-Si lasers via micro-transfer printing ($\mu$TP), and their extension toward scalable photonic systems. The work was organized into three major technical directions:

- **Chapter** 2 introduced the motivation for advanced laser integration and presented the design, fabrication, and characterization of a $\mu$TP-based hybrid laser on the IMEC 400nm+ platform. The resulting laser demonstrated both ultra-wide tunability and narrow linewidth, meeting the requirements of advanced telecom standards such as 400G-ZR. Beyond this, a series of demonstrators adapted the same laser platform for a range of applications, including biomedical sensing, SWIR spectroscopy, gas sensing with wavelength locking, coherent-critical systems, and programmable microwave photonic signal processing, highlighting its flexibility and platform potential.

- **Chapter** 3 addressed the need for higher optical output power by developing and integrating a high-saturation-power SOA using $\mu$TP. A novel tapered SOA structure was proposed and characterized, demonstrating enhanced saturation behavior and output power. The chapter also compared this design with the state of the art and proposed alternative booster strategies for future development.

- **Chapter** 4 shifted focus toward wafer-scale $\mu$TP integration, establishing essential tools and process optimizations (e.g., BCB spray coating, $\mu$TP

printer setup) and performing the first full-wafer $\mu$TP demonstration of III–V components on an imec SiPh platform.

## 5.1 Key Contributions

This thesis presents a broad range of technologies and application-driven laser platforms. Below, the candidate's specific contributions are outlined across core developments, extended use cases, and collaborative efforts.

### Core Technological Contributions

- First demonstration of a hybrid III–V-on-Si laser achieving ultra-wide tunability and narrow linewidth on the IMEC 400 nm+ platform using $\mu$TP.
- Design and realization of application-specific laser variants for biomedical, sensing, coherence-critical systems, and programmable photonics use cases.
- Development and demonstration of a $\mu$TP-compatible high-saturation-power SOA for laser boosting.
- Foundational work on wafer-scale $\mu$TP processing, including process design, adhesive optimization, and alignment analysis.

### Practical Contributions in Design, Fabrication, and Characterization

- **Ultra-wide tunable narrow-linewidth III-V-on-Si laser:** Design by candidate; SOI wafer fabrication by IMEC; III-V SOA fabrication by III-V Lab; full integration (pre-, $\mu$TP, post-processing) and characterization by candidate.
- **High-saturation-power SOA:** The overall design, fabrication, integration, and characterization were led and primarily carried out by the candidate, with specific support from PRG colleagues on selected process steps.
- **Wafer-scale integration:** SOA and FP block design by candidate; SOI wafer fabrication by IMEC; III-V coupon fabrication by III-V Lab; adhesive DOE design and recipe selection by candidate; spray coating by TRANSVERSE team; wafer-scale printing and alignment analysis by candidate.
- **Heartbeat monitoring laser:** Based on the core laser developed by the candidate; additional contributions included support for lens integration (CSEM), PCB design and wirebonding/assembly (Philips), and laser driving setup for the use case (VTT).

- **Spectroscopy laser:** Based on the core laser developed by the candidate; the first trial, including design, integration, characterization, and diagnostic analysis, was led and executed by the candidate. The second trial, including integration and characterization, was carried out by the PRG team.

- **Gas sensing laser:** Based on the core laser developed by the candidate; additional contributions included support for PCB and packaging design, wirebonding, and assembly (PhiX), and laser driving setup for the use case (OnePlanet).

- **Linewidth-reduced laser for coherence-critical applications:** Based on the core laser developed by the candidate, excluding the SiN PIC design; pre-integration of III-V coupons and wafer-scale integration were performed by the candidate. Only sample-scale results are reported in the related publication.

- **Programmable photonics:** SOI PIC design by PRG; SOI wafer fabrication by IMEC; III-V coupon fabrication by III-V Lab; candidate collaborated on process flow preparation, integration, and post-processing. PCB design, wirebonding, assembly, and characterization were carried out by PRG in collaboration with IDLab.

## 5.2 Towards an Ecosystem for Wafer-Scale $\mu$TP Integration

An essential driver of this work is the ambition to make micro-transfer printing a scalable and manufacturable technology, not just at the device level, but across an ecosystem of interoperable platforms and suppliers. This ambition is now being realized within the European PhotonixFAB initiative, which aims to build a full-stack silicon photonic ecosystem capable of integrating non-native components, such as III–V gain blocks and photodiodes, and LN modulators, into advanced photonic platforms in a wafer-scale, high-volume, and cost-efficient manner.

Within PhotonixFAB, key players include:

- Non-native component providers: SMART Photonics (III–V)

- SiPh platform providers: imec (iSiPP200), Ligentec (SiN)

- Wafer-scale integration fabs: X-Fab

- Design and software partners: Luceda Photonics

- R&D and pilot line providers for $\mu$TP integration: TRANSVERSE

In this context, TRANSVERSE plays a central role, not only in developing the wafer-scale $\mu$TP pilot line but also in defining design rules, PDKs, and integration recipes to make III–V (and potentially other non-native) components available as standardized building blocks.

To build on the current work, several directions are envisioned:

- Laser performance optimization: Enhancing output power, thermal stability, and wavelength control can be pursued through several concrete measures. One key strategy is reducing the thermal impedance between the active region and the heat sink. This can be achieved by improving the internal thermal vias within the SOA and PIC layers to facilitate more efficient heat extraction. Additionally, flip-chip bonding the entire SiPh chip directly onto a thermally conductive submount or heat sink, rather than relying solely on localized TEC contact, can significantly lower the overall thermal resistance. These improvements would enable higher bias currents and sustained optical output without compromising wavelength stability or device reliability.

- $\mu$TP process standardization: Establishing design rules, coupon formats, and bonding specs that work across multiple fabs and platforms.

- Reliability and qualification: Performing accelerated ageing testing, environmental stress testing, and yield optimization for industrial deployment.

- Expansion to other materials and functions: Extending $\mu$TP to integrate photodetectors, modulators, and other active elements using diverse materials such as LN or even CMOS electronics.

- Industrialization: Supporting the translation of research to manufacturing through a living ecosystem (such as PhotonixFAB) where foundries, packaging houses, and designers collaborate around $\mu$TP as a shared integration approach.

This thesis lays a foundation for realizing modular, wafer-scale, and high-performance photonic systems using micro-transfer printing, a technology with the potential to transform how hybrid photonics are designed, fabricated, and scaled across communication, sensing, and computing markets.