Monolithic heterogeneous integration of PbS colloidal quantum dot photodiode on silicon nitride

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Abstract: Monolithic integration of PbS colloidal quantum dot photodiodes on silicon nitride waveguides is demonstrated for the first time. Waveguide width and top cladding thickness are designed to meet the low saturation threshold of optical power.

1. Introduction

Colloidal quantum dots (CQD) are emerging as an attractive material for photodetectors due to their strong and tunable absorption at infrared wavelengths [1], cheap chemical-based synthesis, solution-based processing, and good compatibility with different kinds of substrates. The performance of CQD-based photodiodes has improved greatly, with detectivity of $>10^{12}$ cm Hz^{1/2} W⁻¹ [2] and response time as fast as 10 ns [3] demonstrated. The good performance and compatibility with a wide range of substrates make CQD photodiodes a potential candidate for integration with photonic integrated circuits, especially in those cases where the active material cannot easily be grown epitaxially. Silicon nitride (SiN) is a promising integrated photonics platform due to its low propagation loss, high power handling, large transparency window and CMOS compatibility. However, the platform has no compatible active components like photodiodes and thus far their integration was based on hybrid heterogeneous methods, e.g. bonding [4] or transfer printing [5]. In this report, we demonstrate the integration of PbS CQD-based photodiodes on silicon nitride waveguides, operating around 1310nm.

2. Design and fabrication

On-chip waveguides can be very compact, with a typical cross-section area $< 1 \text{ um}^2$. This strong confinement results in an extremely high power density. Therefore, for on-chip photodiodes, carriers are generated at a high rate, and it is very easy saturate the photodiode. To ensure the proposed waveguide coupled photodiodes can work efficiently, we fabricated large-area photodiodes first and measured their saturation level. The large area photodiodes were built on a glass/ITO substrate, and consisted of a stack of 100 nm ITO / 60 nm ZnO / 60 nm PbS-PbI / 60 nm PbS-EDT / 100 nm Au. The ZnO-film forms the electron transport layer and is deposited by a sol-gel method. Two different types of PbS CQDs were used for absorption and hole transport respectively. PbS CQDs with an exciton peak around 1300 nm were used for absorption. The long oleic acid ligands were exchanged for iodine by solution-phase ligand exchange to increase the carrier mobility and make them slightly n-doped. PbS CQDs with excitonic absorption around 900 nm were spin-coated on top as the hole transport layer. The original oleic acid ligands were replaced by 1,2-ethanedithiol (EDT) using solid-phase ligand exchange to make the film p-doped. Au was thermally evaporated onto the film through a shadow mask. If we increase the optical power density in the photodiode, the efficiency (defined as the number of generated carriers divided by the number of photons) is constant at first and then goes down, as shown in Fig. 1(a). The turning point is where the photodiode saturation happens. To link the saturation threshold of large-area and waveguide integrated photodiodes, we introduce a new parameter instead of the simple power density, that is, the maximum integrated generation rate along the z-direction $G_{inte.z.max}$:

$$G = \frac{P_{abs}}{h\nu} = \frac{2\pi n\kappa \varepsilon_0}{h} |E(x, y, z)|^2, \qquad G_{intg,z} = \int Gdz, \qquad G_{intg,z,max} = max\{G_{intg,z}\}$$
(1)

where G is the carrier generation rate units of m⁻³s⁻¹, P_{abs} is the optical power absorbed per unit volume, hv is the photon energy, n and κ are the real and imaginary parts of the complex refractive index respectively, and E is the electrical field. $G_{intg,z}$ is related to the saturation of each pixel in the x-y plane of the photodiode. $G_{intg,z,max}$ determines the onset of saturation of the photodiode as a whole if the illumination is not uniform. The illumination on the large area photodiode has a gaussian shape for our measurement, so $G_{intg,z,max}$ is $G_{intg,z}$ at the gaussian peak position. For large area photodiodes, saturation is measured to start from $G_{intg,z,max} > 6e^{21} \text{ m}^{-2}\text{s}^{-1}$ as shown in Fig. 1(a).

Next, the photodiode was put on top of a SiN waveguide, as shown in Fig. 1(b). Here ZnO deposited by atomic layer deposition (ALD) was used as the electron transport layer, since it has a higher conductivity, allowing for long-distance electron transport. Ti/Au was used as the n-contact metal due to its low contact resistance with ZnO. The generation rate of on-chip photodiodes was simulated with the Lumerical FDE solver. The simulation result in Fig. 1(c) shows how $G_{intg,z,max}$ decreases with increasing SiO₂ cladding thickness and waveguide width. A top cladding thickness of 300 nm and waveguide width of 30 µm were chosen for the on-chip photodiode. For these parameters, $G_{intg,z,max} = 6.3e^{21} \text{ m}^{-3}\text{s}^{-1}$ for an input power of 1 µW, which is around the saturation threshold obtained for the large area detector.



Fig. 1. (a) Measured efficiency of large area photodiode vs. power density at a bias of -1V, with wavelength at 1275nm (b) Cross-section of waveguide integrated photodiode, (c) Simulated generation rate of waveguide integrated photodiode vs. waveguide width and top cladding thickness when the input optical power is 1μ W.

3. Results and discussion

The current-voltage curves for waveguide integrated photodiodes under dark conditions and illumination at 1275nm are shown in Fig. 2(a). The photodiode has a low dark current of ~1 nA at -1 V bias. Fig. 2(b) shows the efficiency of the photodiode at -1 V bias under different input optical powers. At optical powers below 10 nW, the efficiency is almost constant, which indicates a linear photocurrent response to optical power as shown in the inset. When the optical power > 10nW or $G_{intg,z,max} > 5e^{19} \text{ m}^{-2}\text{s}^{-1}$, the efficiency decreases fast. Hence, the saturation generation rate $G_{intg,z,max}$ is more than 2 orders lower than for the large area photodiode, which we believe is due to contamination of the material interfaces during fabrication. We are currently optimizing the process to get cleaner integration. Fig. 2(c) shows the efficiency of integrated photodiodes with different waveguide widths. The efficiency of the photodiodes is better for larger width, which is consistent with the simulation.



Fig. 2. (a) I-V curves of on-chip photodiode under dark conditions and illumination, (b) Efficiency vs. optical power at -1V bias, inset is the response at low optical power level, (c) Efficiency with different waveguide widths.

4. Reference

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