Graphene electro-absorption modulators integrated at wafer-scale in a CMOS fab

C. H. Wu[1,2], S. Brems[1], D. Yudistira[1], D. Cott[1], A. Milenin[1], K. Vandersmissen[1], A. Maestre[3], A. Centeno[3], J. Van Campenhout[1], C. Huyghebaert[1], M. Pantouvaki[1]

[1] imec, Kapeldreef 75, Leuven, Belgium.

[2] Ghent University-imec, Department of information Technology, Technologiepark-Zwijnaarde 15, Gent, Belgium

[3] Graphenea Semiconductor SLU, San Sebastian, Spain. Email: cheng.han.wu@imec.be, pantouvm@imec.be

Abstract

We demonstrate graphene electro-absorption modulators (EAM) integrated on 300mm wafers. The integration is based on imec's 300mm silicon photonics platform and the full integration sequence is using standard CMOS production tools expect for the 6-inch CVD graphene growth and transfer, transferred by Graphenea. 164x TE EAMs were measured per wafer and demonstrate 90% yield with modulation efficiency (ME) of 41±5.6 dB/mm for 8V voltage swing, after process optimization. The 3dB bandwidth of the EAMs is 14.9±1.2 GHz for the device with 50µm active length. Both parameters show comparable performance with lab-based devices, obtained on coupons using similar CVD graphene. This work paves the way to enable high-volume manufacturing of 2D-material-based photonics devices.

Keywords: Graphene, EAM, silicon photonics, integration

Introduction

Being manufactured by existing CMOS fabrication processes makes silicon photonics well-positioned for high-yield and high-volume production at low cost. It also offers a platform for the integration of novel materials using state-of-the-art equipment and process control. Single-layer graphene (SLG) EAMs with broadband ~70nm operating wavelength range have been reported in [1], while double-layer graphene (DLG) EAMs have achieved 50Gb/s high speed performance [2]. However, most of the graphene-based photonics devices are fabricated on coupons, using lab processing, such as ebeam lithography, metal lift-off and contact metals that are not compatible with CMOS technology. Here, we present for the first-time scalable graphene EAM integration in imec's 300mm fab.

Fab-level Integration

The process flow for inline graphene EAMs is shown in Fig. 1. First, standard modules are used for the patterning of Si waveguides on 300mm SOI wafers with 220nm thick Silicon and 2µm buried oxide (BOX) [3]. After oxide planarization of the waveguides, the device area is implanted using 3 doping levels, targeting to lower the contact and sheet resistance of the Si part of the device, without impacting waveguide optical loss. A gate oxide thickness of ~5nm is implemented on the waveguides, as a compromise between ME and 3dB bandwidth [1]. Commercial CVD graphene of 6-inch size is then transferred by Graphenea [4] on the 300mm wafer center as shown in Fig. 2. The wafers are then capped using a customized ALD AlO_x. Here we implement two deposition conditions, process A for wafer1 and an optimized process B to achieve uniform coating of a dielectric on a self-passivated graphene layer for wafer2. After AlO_x deposition, a SiO_x hardmask is deposited. Graphene patterning is done by dry etching the SiO_x hardmask, followed by resist strip and dry etching of the AlO_x cap and the graphene in a single step. This sequence is critical to avoid graphene delamination. Pre-metal dielectric is deposited and planarized by chemical mechanical polishing (CMP) to a final thickness of 600nm. The 250nm-diameter contacts to graphene and to the doped Si are dry etched separately through the oxide and AlO_x layers, ending up with side contacts for graphene. Ti/TiN/W metallization is used to fill the contacts followed by W-CMP. Finally, the Metal-1 layer is formed using a conventional Cu-oxide module. Final device's images are shown in Fig.3.

Device results and Discussions

The EAM designs are based on C-band TE 500nm-wide waveguides with graphene length varying from 25 to 100µm. Fig. 4(a) and (b) show an example of the device's transmission spectra at different active lengths and linear fit vs length. Propagation loss ~82dB/mm is extracted for the graphene active section. The cumulative distribution function (CDF) of the graphene loss measured on unbiased devices is presented in Fig. 4(c) and (d) for two wafers. The slope of CDF curve indicates that graphene is uniformly integrated among 164 devices/wafer, albeit with local variations of graphene quality on top of the waveguide. We attribute this to local topography variations of the waveguide planarization process. Fig.5(a) shows the static transmission spectra from 1530nm to 1590nm when sweeping voltage between -4 and 4 V. Typical transmission variation with voltage is shown in Fig. 5(b). The extinction ratio (ER) CDF plot is shown in Fig. 4(c) and (d). The ER yield improves from ~50% on wafer 1 to ~90% on wafer2, which is attributed to the optimization of the AlOx deposition process. ME 41±5.6 dB/mm is achieved for wafer2 and is comparable with the similar device fabricated in the lab [1]. An example of S-parameter result performed on wafer2 at 1550nm wavelength is shown in Fig. 6. 3dB bandwidth of ~16, 14, 11, 10 GHz was obtained for device lengths of 25, 50, 75, and 100µm, respectively. The summary and the comparison with lab-based samples are listed in Table I.

To sum up, by optimizing the graphene encapsulation process, as well as the integration scheme for graphene contact, 90% yield of SLG EAM devices is achieved. The performance match with the similar devices fabricated in the lab. With a robust CMOS-compatible integration route, graphene EAMs could be further explored to improve device performance [5], paving the way for applying 2D technology in the industrial world.

Reference [1] C. Alessandri et al., JJAP., 59(5), p. 052008 (2020) ; [2] M. A. Giambra et al., Opt. Expr., 27(15), pp. 20145-20155 (2019) ; [3] M. Pantouvaki et al., J. Light. Tech., 35(4), pp. 631-638 (2017) ; [4] https://www.graphenea.com ; [5] L. A. Shiramin et al., IEEE J. Sel. Top. Quantum Electron., 23(1), pp. 94-100 (2016).

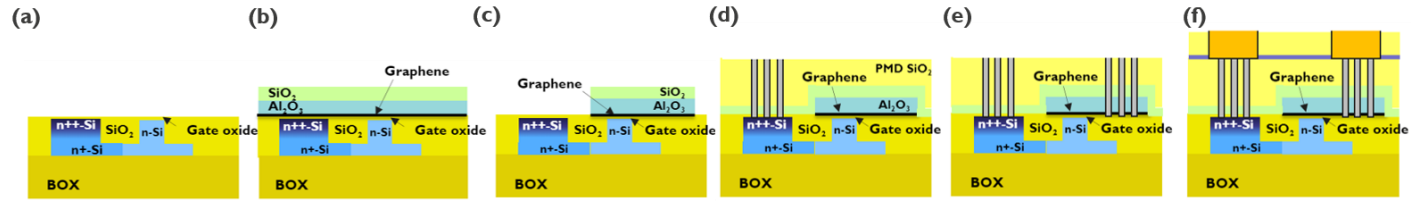


Fig. 1. The full in-line integration flow in this work. (a) Waveguide patterning, planarization, and implants. (b) Graphene transfer and encapsulation. (c) Graphene patterning. (d) PMD planarization and contact to Si. (e) Ti/TiN/W contacts to Graphene. (f) Metal (Cu/SiO_2).

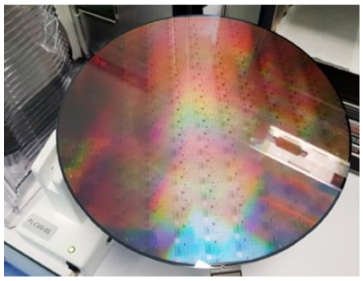


Fig. 2. Image after 6-inch graphene transfer at the center of 300mm wafer.

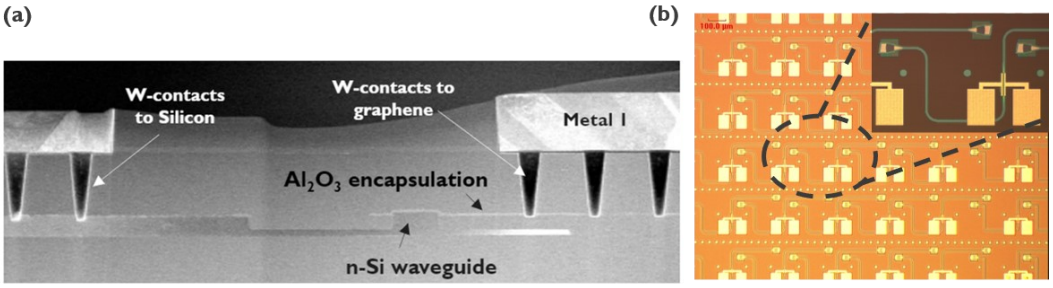


Fig. 3. (a) Cross-section STEM and (b) Top-down microscope image of the SLG EAM device after in-line fabrication.

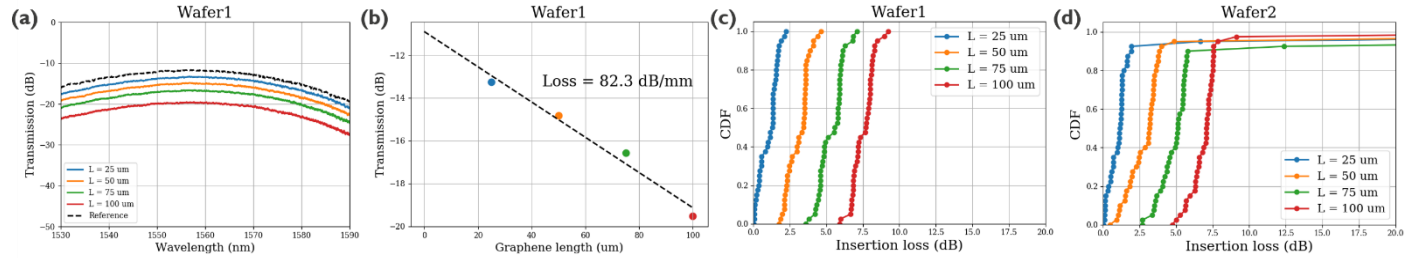


Fig. 4. (a) Transmission of unbiased C band TE mode SLG EAM on the device in wafer1 with active length varying from 25 to 100µm. (b) Propagation loss of the graphene active section is extracted from Fig. 4(a). The insertion loss CDF results for (c) wafer1 and (d) wafer2.

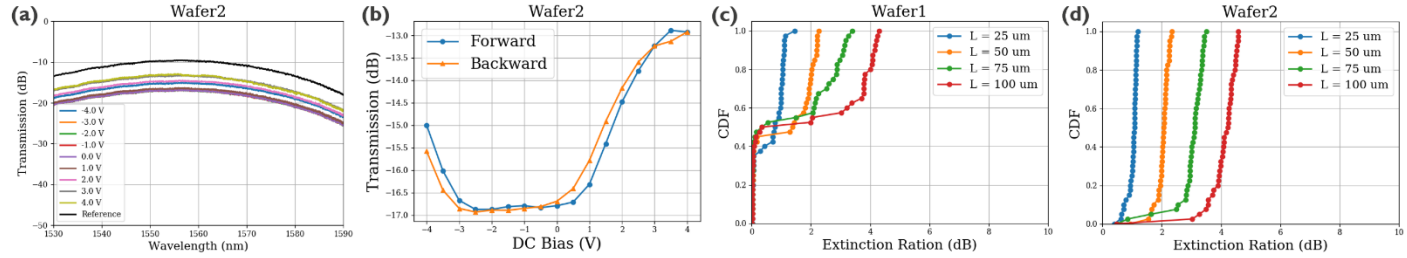
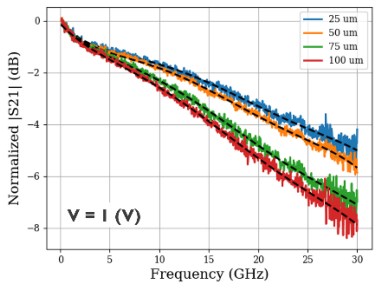


Fig. 5. (a) Transmission of C band TE mode SLG EAM on the device in wafer2 with 100µm active length under different bias conditions (from -4V to 4V). (b) Transmission modulation versus voltage based on Fig.4(a). The ER CDF results for (c) wafer1 and (d) wafer2.



Device(s)	Active length (µm)	IL @0V (dB)	Propagation loss @0V (dB/mm)	ME (dB/mm)	3dB bandwidth (GHz)
This work – Wafer1	25	1.0 ± 0.71	85 ± 8.4	17 ± 18.1	-
	50	3.1 ± 0.74			
	75	5.3 ± 0.85			
	100	7.5 ± 0.74			
This work – Wafer2	25	0.9 ± 1.27	83 ± 9.6	40 ± 8.2	16.4 ± 3.05
	50	2.7 ± 1.03			14.9 ± 1.18
	75	4.9 ± 1.51			11.5 ± 3.91
	100	6.8 ± 0.85			10.6 ± 2.35
Sample 1 [1]	75	~6	-	48	8.9
Sample 2 [1]	75	~4.4	-	36	16.1

Fig. 6. S21 frequency response from the device in wafer2. **Table I**: Summary and benchmarking the SLG EAM based on C-band TE mode.

Acknowledgements: The authors acknowledge funding from EU Horizon 2020 research and innovation program under grant agreement no. 785219 and from imec's industrial affiliation Optical I/O program.