Compound Semiconductor -

IN TODAY'S hyper-connected world silicon photonics has emerged as a key technology for delivering massive data transfer. Several foundries are now offering silicon photonics platforms for the manufacture of electro-optical transceivers with terabit-per-second capacity. These transceivers can serve the growing needs of data communication in hyperscale data centres, as well as in emerging high-performance computing and AI compute clusters.

Silicon photonics is well suited to these tasks, thanks to its high refractive index and transparency at telecom wavelengths, and its capability to carry light efficiently within sub-micron waveguides. These attributes enable photonic ICs (PICs) with a high integration density to offer a scaling path to multi-Tbit/s optical modules for datacom applications, and to provide a pathway for dense optical-phased arrays for future LiDAR systems.

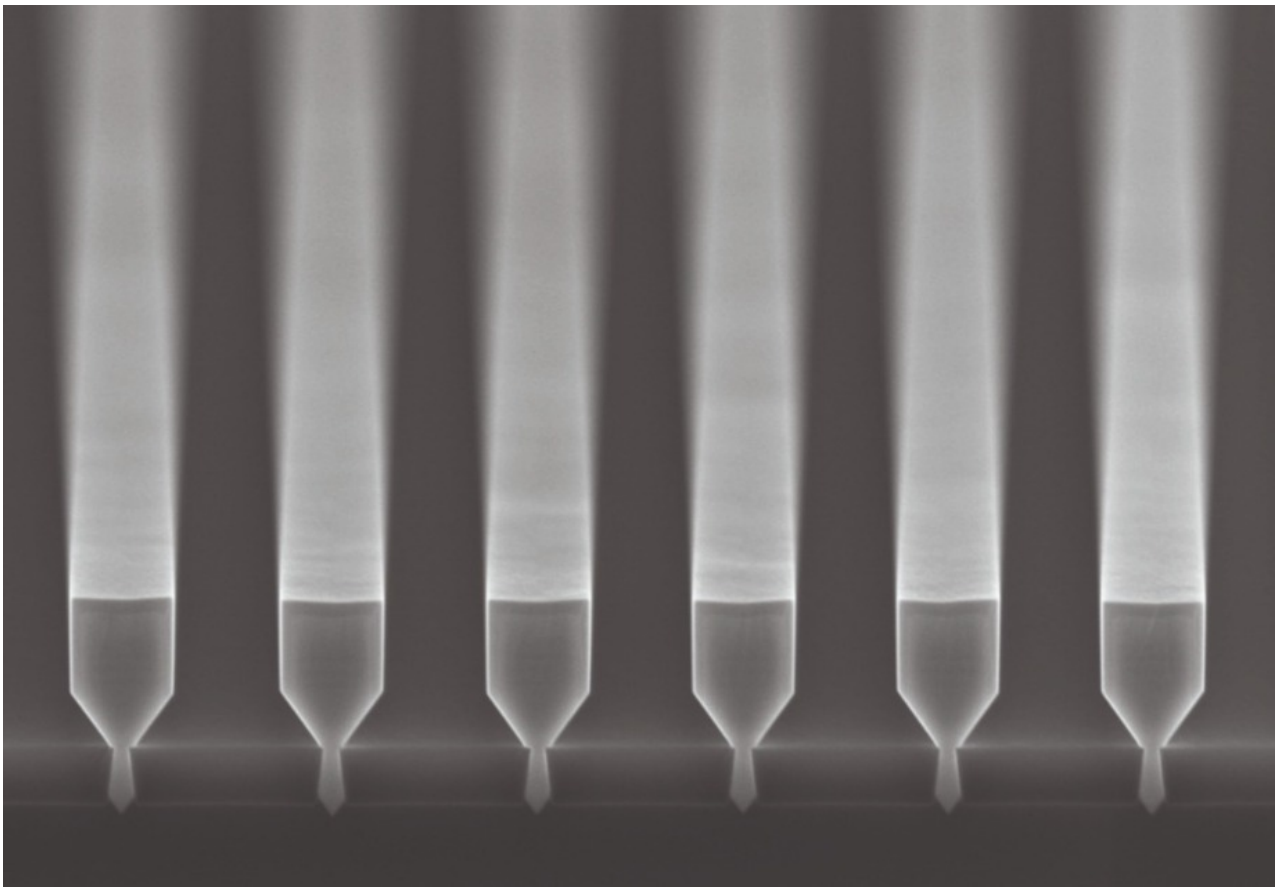

Figure 1. Tilted scanning electron microscopy (SEM) image of III-V nano-ridges grown on silicon.

Yet, despite all this promise, it should be noted that silicon is not a perfect material for making a PIC. Due to its indirect bandgap, it has limited capabilities for light modulation, detection and amplification.

All that functionality in today's silicon PICs is partially provided by the monolithic integration of other materials. One of them is germanium, which enables waveguide photodetectors with excellent responsivities out to 1550 nm and acceptable dark currents for high-speed data receivers. However, with germanium, light amplification is still missing from the PIC engineer's toolbox, as well as photodetection at longer wavelengths – these are valued attributes for a variety of emerging optical sensing applications.

A well-trodden path to overcoming this limitation is to integrate III-Vs onto a silicon photonics platform. Right now, two of the most popular approaches to hybrid III-V integration are flip-chip assembly and die-to-wafer bonding. Both are suitable for serving low to medium wafer volumes. However, in the longer run, arguably monolithic hetero-epitaxial growth of III-Vs directly on silicon offers a more promising pathway to the lowest cost, scalability, and the highest throughput.

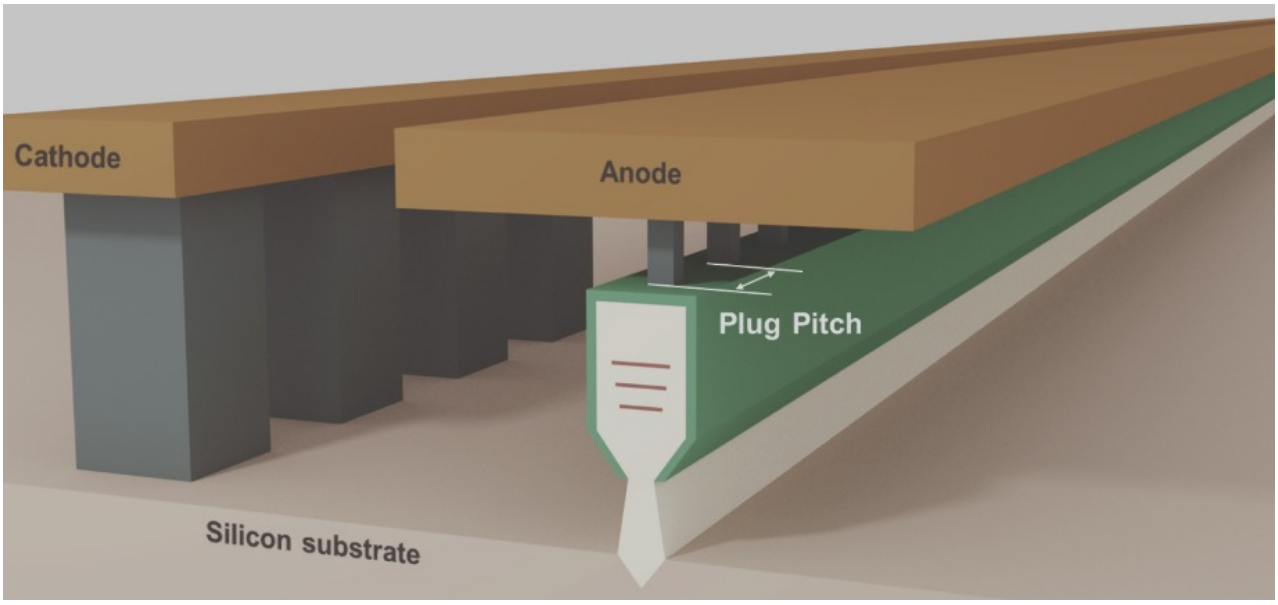

Figure 2. 3D figure of nano-ridge waveguide photodetector devices produced at imec.

While this approach has much potential, realising it is not easy. For several decades researchers have grappled with the difficulties of direct growth of high-quality III-V layers on silicon. There are challenges associated with mismatch in the crystal lattice constant, the thermal expansion coefficient and crystal polarity. Despite significant progress, even today state-of-the-art III-V layers that are directly grown on silicon have defectivity levels several orders of magnitude higher than those on native substrates. It is also worth noting that when these layers are added by the most common approach, blanket growth, buffer layers have to be several micrometres thick to accommodate crystal defects. That's not ideal, hampering scalability to large wafer sizes.

Shifting to nano-ridges

At imec, a globally renowned microelectronic research centre based in Belgium, our team is pioneering a unique approach to tackling this issue. With our way forward, which we refer to as nano-ridge engineering, our process for forming devices begins with the selective-area growth of III-Vs in narrow trenches that are patterned on a 300 mm silicon substrate. The high aspect ratio of these narrow trenches traps dislocation defects. After

filling the trench, growth of the III-V continues, forming a nano-ridge with an increased volume, an engineered nano-ridge shape, and a very low defect density. By avoiding the need for a thick III-V buffer, this approach results in III-V nano-ridges that are close to the underlying silicon.

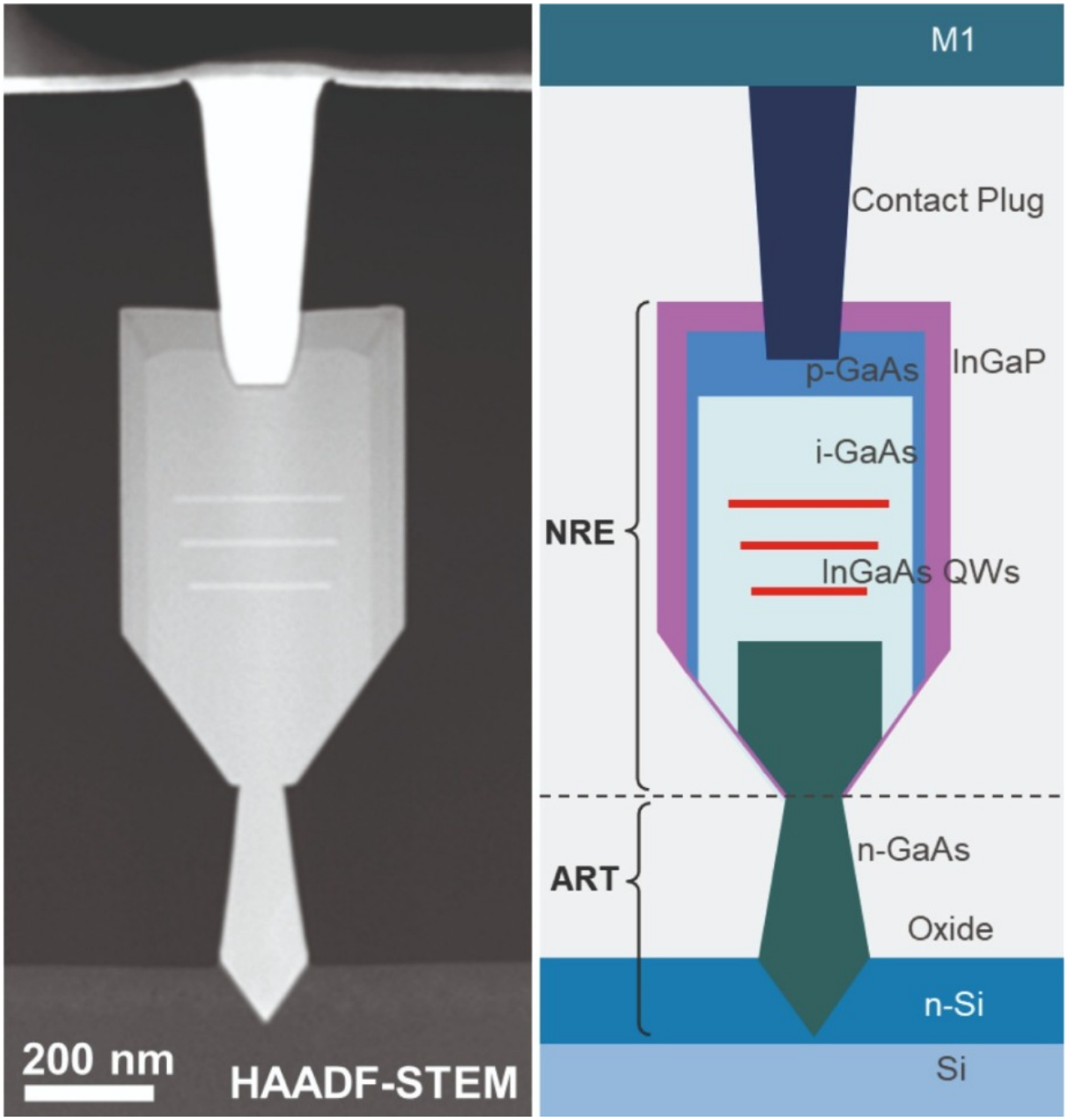

Figure 3. (Right) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) cross-sectional image of GaAs nano-ridge with three InGaAs quantum wells. (Far right) Description of the nano-ridge cross-section. For more details, see C. I. Ozdemir et al. Dec. 2020, pp. 1–4, doi: 10.1109/ECOC48923.2020.9333310

When we use nano-ridge engineering to integrate III-Vs with silicon, we form silicon {111} facets at the bottom of the trenches by applying an anisotropic etch. This creates a V-shape bottom, with the orientation of the facet preventing the formation of anti-phase domains (see Figure 1).

We control the profile of our nano-ridges by adjusting the growth parameters for MOCVD. We have learnt how to engineer a rectangular-shaped nano-ridge with a flat (001) surface, an architecture that provides a great platform for photonics as every ridge provides a waveguide for light and a foundation for making III-V devices.

In addition to controlling the shape of the nano-ridge, our engineering technology enables us to introduce different dopants and III-Vs. We can form diode junctions, introduce quantum wells, alternate between different combinations of III-Vs, and passivate our waveguides.

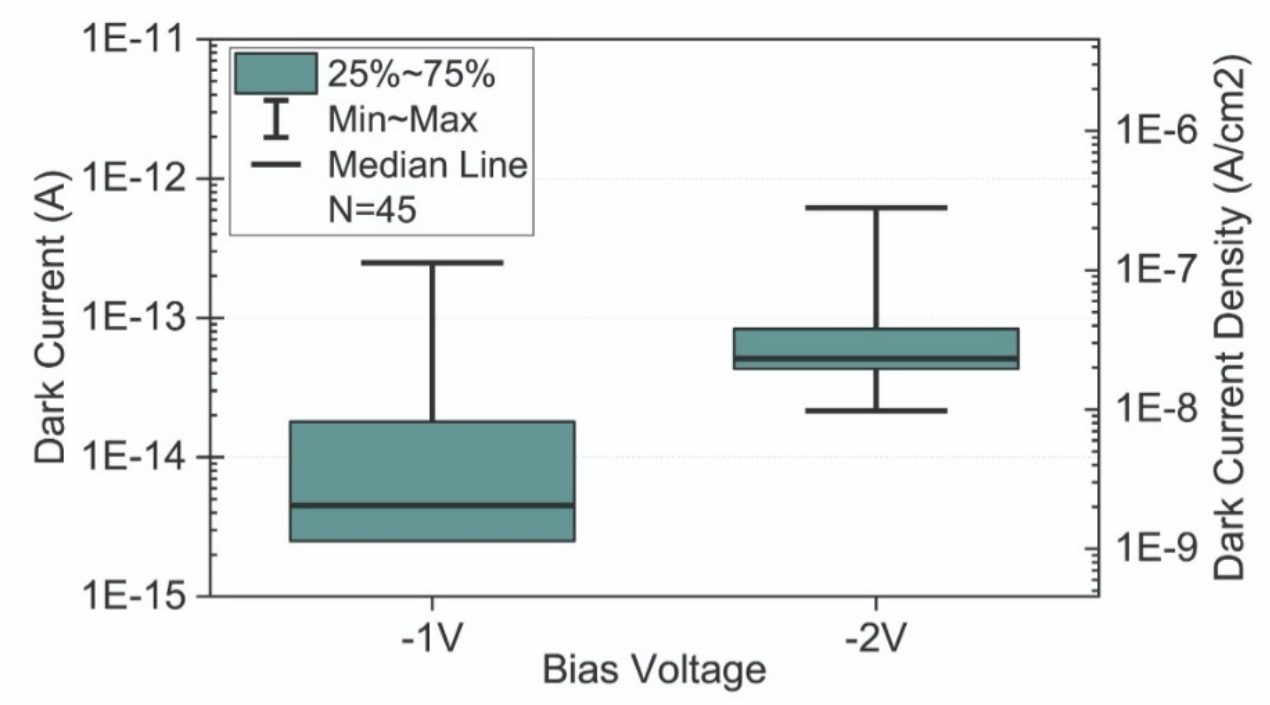

Figure 4. Dark current distribution at different bias voltages. For more details, see C. I. Ozdemir et al. Dec. 2020, pp. 1–4, doi: 10.1109/ECOC48923.2020.9333310

A starting point for our work has been the optically pumped lasing of nano-ridge waveguides, a feat demonstrated by our team several years' ago. Back then, using nano-ridge engineering, we compressively strained $In_{0.20}Ga_{0.80}As$/GaAs multi-quantum wells horizontally grown on the (001) plane of a nano-ridge in a nano-ridge waveguide. To ensure carrier confinement and surface passivation, we encapsulated the nano-ridge waveguide with a lattice-matched InGaP layer. Cavities were created by incorporating reflector gratings into nano-ridge waveguides, and the addition of out-coupler gratings enabled us to read out the laser response. Highlights from that time included lasing at 1028 nm, with the peak of the laser emission at a level 28 dB higher than the background. Initially we built on that success with simulations considering coupling into a regular silicon waveguide. These calculations underscored the promise of integrating our nano-ridge devices with an established silicon photonics platform.

We have used nano-ridge engineering to produce a wide variety of devices. Before our latest work on photodetectors, we developed HBTs. This class of transistor exploits the excellent mobility of the III-Vs for high-frequency RF applications, such as 5G and its

potential successors. The attractions of producing HBTs on silicon with nano-ridge engineering include greater flexibility of designs, lower cost and a smaller footprint.

Nano-ridge photodetectors

Recently, we have expanded the range of devices that can be produced on our nano-ridges to include high-quality photodetectors. A key requirement when designing these devices is to make sure that the bandgap of the absorbing material is low enough to capture the light of the desired wavelength. If the device is to have a small footprint, it is also critical that the absorption coefficient of the material is sufficiently high. There are also other potential requirements: if there is a need for a low-noise, highly sensitive detector, the absorbing material must have a low defect density; and if high-speed operation is a must, then the absorbing material needs to have high mobilities for electron and holes, as this enables carriers to be collected quickly. For the last few decades, conventional InGaAs photodetectors fulfilling all of these requirements have been produced in large quantities.

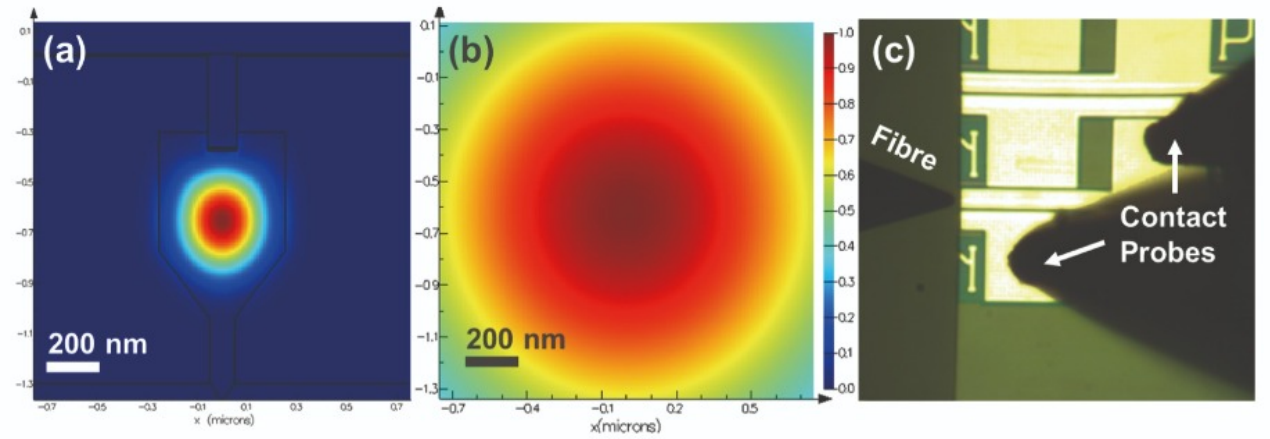

Figure 5. (a-b) Modal cross-sections of a nano-ridge waveguide and a 2.0 µm focused beam, using a linear colour scale. (c) Top view of measurement setup with cleaved facet and lensed fibre. For more details, see C. I. Ozdemir et al. Dec. 2020, pp. 1–4, doi: 10.1109/ECOC48923.2020.9333310

The most common architecture for the photodetector is a *p-i-n* diode, with light absorbed primarily in the intrinsic volume. With this design, diodes operating under reverse bias can attain very high electric fields in the intrinsic region, aiding effective collection of the generated carriers. Metal contacts at the *p-* and *n-* sides of the diode provide electrical connectivity to the outside world (see Figure 2).

In our latest study, we have evaluated the potential of using a nano-ridge to monolithically integrate high-quality III-V photodetectors on a silicon platform. Using structures for demonstrating optically pumped lasers as the foundation for our recent work, we have developed the expertise to introduce *p-i-n* doping and create a diode junction, and to add metal contacts to our devices.

We grow our InGaAs/GaAs photodetectors in imec's 300 mm CMOS line, using MOCVD to add III-Vs to *n*-doped silicon wafers. By growing these III-Vs in trenches 300 nm deep and 80 nm to 100 nm wide, we have an aspect ratio of more than 3.5, which is high enough to ensure efficient defect trapping. All the threading and misfit dislocation defects initiated at the interface between GaAs and silicon are effectively confined inside the trenches.

During the growth of GaAs, dopants are introduced to define the *p-i-n* diode, using doping concentrations of about 1.0 x 10^{19} cm^{-3} for *n*-type and *p*-type GaAs. Absorption of the incident light takes place in three 10 nm-thick $In_{0.20}Ga_{0.80}As$ quantum wells embedded in the *i*-GaAs layer, shown in Figure 3. To passivate the surface, we cap the rectangularly shaped nano-ridge waveguide with an InGaP layer. After oxide filling, local etching of the InGaP layer and the addition of tungsten contact plugs creates an electrical contact to the top *p*-GaAs layer. Also, tungsten plugs down to *n*-doped silicon substrate are formed to contact the *n*-GaAs end of the device. Standard CMOS copper metallization processing complete device fabrication.

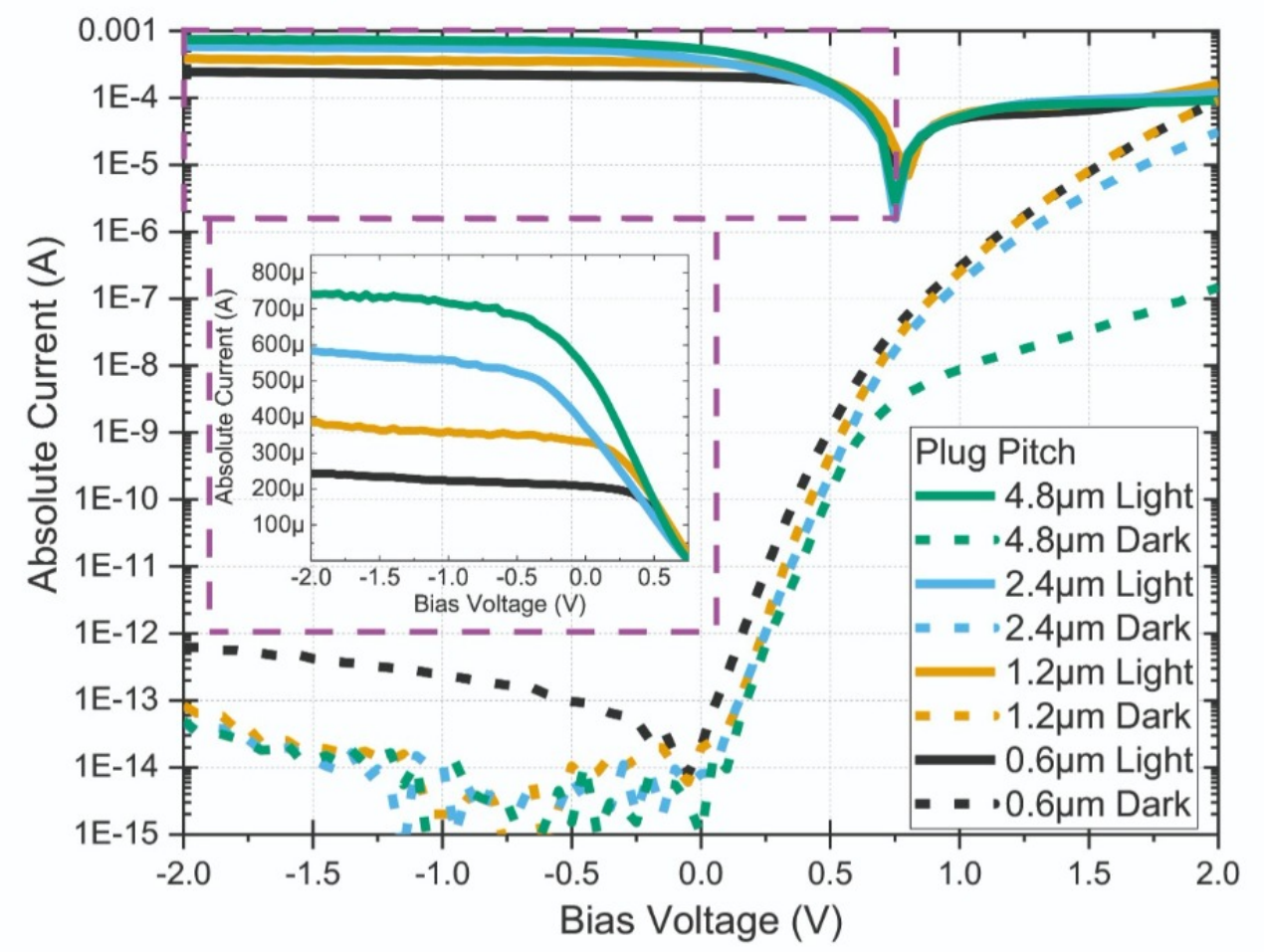

Figure 6. Dark and light measurements of current-voltage (I-V) characteristics of devices with different p-contact plug pitches, (inset) light I-V zoom in at linear scale. For more details, see C. I. Ozdemir et al. Dec. 2020, pp. 1–4, doi: 10.1109/ECOC48923.2020.9333310

With our design, light is strongly confined in the GaAs nano-ridge waveguide, thanks to the high refractive index of GaAs compared to its surrounding oxide layer. Due to the

small cross-section of our nano-ridge waveguides, it challenging to provide a good electrical connection to our devices. Part of the difficulty is that any metal that directly touches the nano-ridges introduces optical absorption losses, and in turn diminishes the responsivity of the photodetector. We have investigated the extent of this issue by varying the density and pitch of *p*-contact plugs landing on the top of the GaAs nano-ridges, and examining their correlation with the measured photodetector responsivity.

In our latest iteration, we cleaved one end of our nano-ridge waveguides to provide optical access from the chip edge to the cleaved optical facet. Cleaving one side of the InGaAs/GaAs nano-ridges yielded 500 µm-long devices.

Before directing light at our photodetectors, we measured their dark current performance under reverse bias. These measurements, carried out under dark conditions – as the name implies – provide an insight into device and material quality. Using typical reverse biases of -1 V and -2 V, we observed very low median dark currents (see Figure 4). For example, at -2 V, we recorded a value of just 0.05 pA, corresponding to a 1.98 x 10^{-8} A cm^{-2} dark current density, calculated by considering the width and the length of our devices. This figure breaks new ground for the dark current of photodetectors monolithically integrated on silicon. Note, however, that the devices we are comparing with operate at higher wavelengths, prone to higher dark currents. That is not to say that our low dark current is not encouraging – it provides a strong indication of good material quality, an essential ingredient for successful monolithic integration.

For our electro-optical measurements, we coupled light into the waveguide through the cleaved facet, using a lensed fibre to provide a beam size of 2.0 µm (see Figure 5). Employing a 1020 nm light source prevented absorption in GaAs, while ensuring absorption in the InGaAs quantum wells.

Due to the small size of our nano-ridge devices, they have a guided mode that is almost five times smaller than the impinging beam. Consequently, coupling losses are inevitable. We evaluated their extent with optical simulation software, which revealed a coupling efficiency of 21 percent. Determining this figure is crucial to estimating of the internal responsivity and quantum efficiency of our devices.

Responsivity is defined as the generated photocurrent, measured in amperes, for each watt of input light power. The maximum theoretical responsivity depends on the wavelength of the incident source, and for 1020 nm it is 0.82 A/W. Our nano-ridge waveguide photodetectors are not far from that upper limit, realising a median internal responsivity of 0.65 A/W at -1 V, recorded for devices with the highest contact plug pitch of 4.8 µm. This equates to an internal quantum efficiency of 79 percent, a high value that shows that even with a comparably small volume, InGaAs quantum wells are successful at absorbing light, while the *p-i-n* diode is effective at collecting the generated carriers and producing a strong photocurrent.

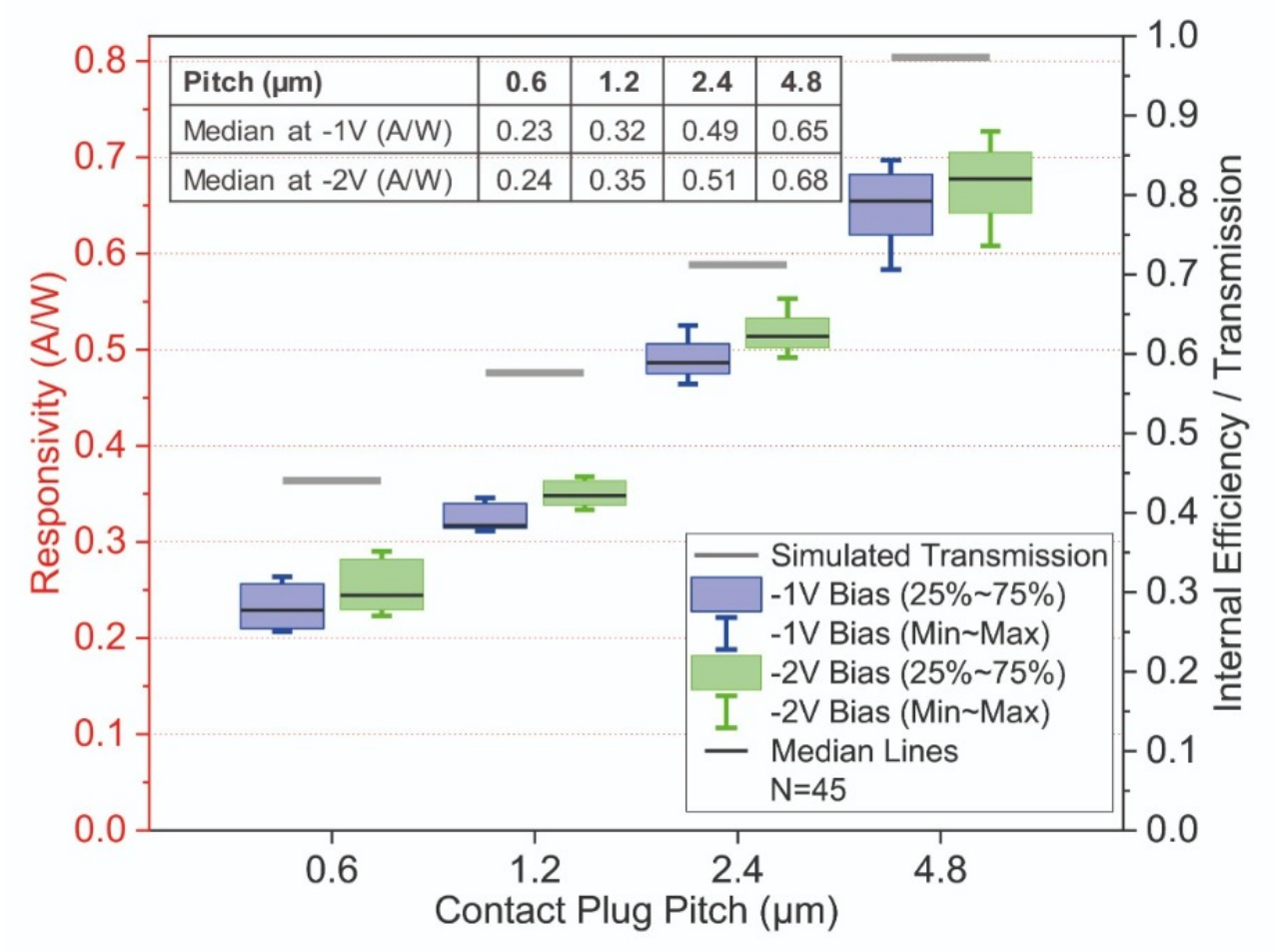

Figure 7. Responsivity distributions for different biases and p-contact plug pitches. Simulated transmission values for different p-contact plug pitches, scaled to right vertical axis. (Inset) Table of median responsivity values. For more details, see C. I. Ozdemir et al. Dec. 2020, pp. 1–4, doi: 10.1109/ECOC48923.2020.9333310

Investigating the performance of our photodetectors with different values for the top contact plug pitch showed that this distance has a strong correlation with the measured responsivity (see Figure 6). Decreasing the density of the contact plug – that is, increasing the pitch distance – cuts light absorption by the metal. This means that as the light propagates through the waveguide, more is absorbed by the InGaAs quantum wells. We have confirmed this behaviour with 3-dimensional optical simulations (see Figure 7).

Our successes to date highlight the great potential of our nano-ridge technology for enabling scalable monolithic integration of high-quality III-V optical devices on a silicon platform. With this approach, we have already enjoyed record-breaking performances. The strength of our architecture is that we have a range of building blocks for III-V devices on silicon. Highlighted here are our InGaAs/GaAs waveguides, operating as photodetectors, and InGaAs quantum wells, which are used as active absorbing media but have previously provided optically pumped lasing.

We continue to advance the capability of our technology. Very recently, we have expanded to ternary InGaAs nano-ridges, opening a pathway to integrating devices that function at longer wavelengths. This is yet another step towards the fabrication of optical

integrated circuits featuring monolithic integration of III-V devices, formed via nano-ridge engineering on a silicon photonics platform.

The authors are grateful to the fab, metrology and support teams of imec for their dedication in this work. This work was funded by the imec's industry-affiliation Optical I/O R&D Program