

# Novel adiabatic tapered coupler for small III-V lasers grown on SOI wafer

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## ABSTRACT

While III-V lasers epitaxially grown on silicon have been demonstrated, an efficient approach for coupling them with a Silicon Photonics platform is still missing. In this paper, we present a novel design for an adiabatic coupler for interfacing nanometer scale III-V lasers grown on SOI with other silicon photonics components. The starting point is a directional coupler, which achieves 100% coupling efficiency from the III-V lasing mode to the Si waveguide TE-like ground mode. To improve the robustness and manufacturability of the coupler, a more advance tapered coupler is designed, which is less sensitive to variations in III-V waveguide dimensions and temperature variations, and still reaches a coupling efficiency close to 100%. The proposed couplers are designed for the particular case of aspect-ratio-trapping (ART) based III-V epitaxy, but it is believed that it should also be compatible with other epitaxial III-V/Si integration platforms. The presented coupler is expected to pave the way to integrating III-V lasers epitaxially grown on SOI wafers with other photonics components, one step closer towards a fully functional Silicon Photonics platform.

**Keywords:** Tapered coupler, III-V epitaxy, SOI wafer, small laser, Si photonics

## 1 INTRODUCTION

The integration of III-V semiconductors on Silicon is one of the key processes needed to build a versatile Silicon Photonics platform incorporating active and passive components. The direct epitaxy of III-V materials on Si can be considered the ultimate strategy to achieve this, but, depending on the approach, still faces challenges in reaching sufficient crystalline quality, and/or interfacing with other silicon photonics components, and/or demonstrating electrical injection. Several groups have developed novel epitaxial processes providing high quality III-V materials directly grown on silicon substrates, demonstrating optically or electrically pumped lasing. An efficient scheme for interfacing these devices with standard silicon photonics devices has not been presented however. In this paper we present a novel adiabatic coupler design to bridge epitaxial III-V devices with Si waveguides. We focus on the case of III-V nano-ridges grown on Si using the aspect ratio trapping (ART) technique [1]. The quality of this material has been investigated in detail [2] and verified by the demonstration of lasing in our previous work [3]. The proposed Si coupler can be added in the silicon layer during the standard shallow trench isolation (STI) process carried out before the III-V growth. As such the adiabatic coupler requires no additional fabrication steps and is fully compatible with the current process.

The next section presents the design of a directional coupler, which illustrates that highly efficient optical coupling is indeed feasible. The following sections then present the design of a more robust tapered coupler, which is more tolerant to process variations.

## 2 DIRECTIONAL COUPLER

Figure 1(a) shows a cross-section of the proposed coupler. The fabrication process starts from an SOI wafer with a 350nm thick top Si layer. The Si couplers, waveguides (WG) and trenches for subsequent epitaxy are defined in this layer through a standard STI process, leaving a 50nm thick slab layer. Next follows a Si wet etch step to open up the Si trenches for GaAs growth. After the GaAs nano-ridge epitaxy, the structure is planarized with SiO<sub>2</sub>. This process fixes the height of the Silicon couplers and WGs to be 350nm. The GaAs ridge is set to be 350nm wide and 450nm high, in line with previous samples that showed laser operation [3]. The free variables for optimising the directional coupler are then the gap between the GaAs nanoridge and the Si WG (denoted as  $W_{Gap}$ , defined as the distance between the right edge of the GaAs trench and the left edge of the Si WG) and the width of the Si WG (denoted as  $W_{Si}$ ). To have full coupling from the TE-like lasing mode of the III-V nano-ridge, shown in the inset of Figure 1(b), to the TE-like mode of the Si WG, the two modes have to be phase-matched. In practice this means the width of the Si WG has to be chosen such that the effective refractive index  $n_{Si}$  of its TE-like ground mode is equal to that of the TE-like ground mode of the III-V nano-ridge,  $n_{III-V} = 2.64$ . From Figure 1(b), which shows the effective index of the first 2 eigenmodes of the Si WG as function of its width, we can derive this phase matching happens for  $W_{Si} = W_{match} = 295nm$  (for a wavelength of 1310 nm). Figure 1(c), which shows a top view of the propagating field for  $W_{Gap} = 240nm$ , shows the periodic exchange of power between both WGs, typically for a phase matched directional coupler.

The coupling length is  $45\mu\text{m}$ . To get full power exchange, the phase-matched condition has to be rigorously met however and the device length has to be exactly equal to the coupling length. Therefore a directional coupler can only be optimized for a single wavelength and is highly sensitive to process variations. To illustrate this, Figure 1 (d) shows how the coupling length and coupling efficiency vary when the wavelength deviates from the design wavelength (1310nm).

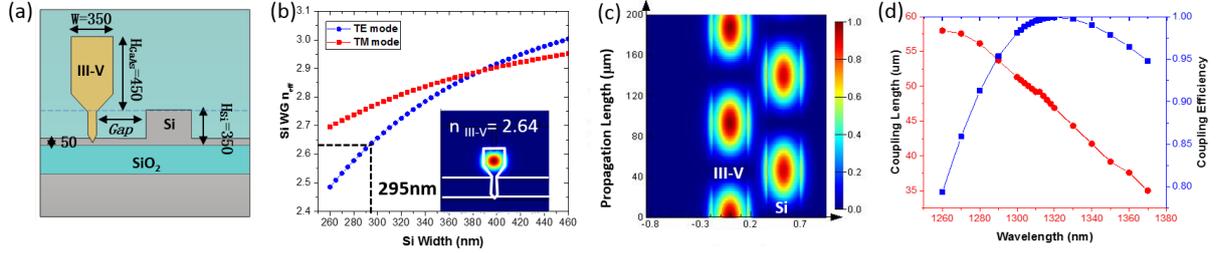


Figure 1. (a) Cross-section of the proposed directional coupler consisting of an active GaAs nano-ridge and a passive Si WG (unit: nm). (b) The calculated effective refractive index of the TE-like and TM-like ground modes of a 350nm high Si WG as a function of its width. The insert shows the TE-like ground mode of the III-V nano-ridge WG. (c) The 2-D top view of the optical power propagating in the coupler. (d) The coupling length and coupling efficiency as a function of wavelength. The coupler was optimised for 1310nm.

### 3 ADIABATIC COUPLER

Given that the directional coupler is narrow-band and exhibits a low tolerance to fabrication and temperature variations, a more robust adiabatic coupler is proposed. The tapered Si WG remains in the same layer as in the directional coupler discussed above but its width is varied (Figure 2 (a)). The left edge of the coupler is kept parallel with the GaAs nano-ridge while the right edge is linearly varying along the coupler. Figure 2(b) shows the top view of the adiabatic coupler. The tapered Si WG starts with a width of  $W_1$ , ends with a width of  $W_2 (> W_1)$  after a length  $L$ , and then connects to a straight WG. The respective optical modes at different cross sections of the coupler are also shown:  $\Phi_{III-V}^{TE}$  is the TE-like ground mode in the standalone III-V nano-ridge;  $\Psi_{+1}^{TE}$  is the symmetric (denoted with '+') TE-like supermode at the position of  $W_1$ ;  $\Psi_{+2}^{TE}$  is the symmetric TE-like supermode at the position of  $W_2$ ;  $\Phi_{Si}^{TE}$  is the TE-like ground mode in the standalone Si WG. For easier recognition, the symbol  $\Phi$  is used to represent the standalone waveguide optical modes while  $\Psi$  is used for the supermodes in the coupling region.

The coupling from the III-V lasing mode  $\Phi_{III-V}^{TE}$  to the Si WG mode  $\Phi_{Si}^{TE}$  can be decomposed into three individual coupling processes. The initial optical mode  $\Phi_{III-V}^{TE}$  in the active III-V nano-ridge is converted to  $\Psi_{+1}^{TE}$  at the start of the Si WG. Figure 2(b) shows that the supermode  $\Psi_{+1}^{TE}$  mostly overlaps with the III-V nanoridge for a narrow width  $W_1$  (that is  $\Psi_{+1}^{TE}$ ), and with the Si WG for a wide width  $W_2$  (that is  $\Psi_{+2}^{TE}$ ). The transition from  $\Psi_{+1}^{TE}$  to  $\Psi_{+2}^{TE}$  happens in the taper region. The last step is the conversion from  $\Psi_{+2}^{TE}$  to  $\Phi_{Si}^{TE}$ , after which the optical field is guided further in the standalone Si WG towards following optical components. The total coupling efficiency is the product of each individual mode coupling process.

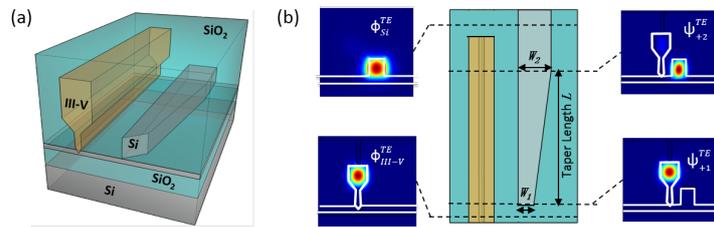


Figure 2. (a) 3-D sketch of the adiabatic coupler. (b) Top view of the coupler and the corresponding TE-like modes at different positions.

#### 3.1 Optimisation of Coupler Widths

To get a high coupling efficiency, the widths  $W_1$  and  $W_2$  are first optimised. Figure 3 (a) shows the overlap of mode  $\Psi_{+1}^{TE}$  with modes  $\Phi_{III-V}^{TE}$  (solid line) and  $\Phi_{Si}^{TE}$  (dashed line) as a function of  $W_{si}$  for  $W_{Gap} = 240\text{nm}$ . It is observed that  $W_1$  should be narrower than 275nm in order to get the overlap between  $\Phi_{III-V}^{TE}$  and  $\Psi_{+1}^{TE}$  higher than 99%, while  $W_2$  should be wider than 315nm for overlap between  $\Psi_{+2}^{TE}$  and  $\Phi_{Si}^{TE}$  higher than 99%. The intersection point is where  $W_{si} = W_{match} = 295\text{nm}$ . Apart from this, it has to be ensured that coupling only occurs among the four TE-like optical modes shown in Figure 2 (b), and all TM-like modes should be excluded. Figure 3 (b) shows the effective refractive index  $n_{eff}$  of the TE- and TM-like ground modes of the

separated III-V/Si WGs (solid lines) and the  $n_{eff}$  of the first four supermodes (dashed lines) of the coupler. The overlap of the dashed line with the solid line reveals whether the supermode is TE-like or TM-like, and if it is centered mostly in III-V or Si. Point *A* is again the phase-matched condition for  $\Phi_{III-V}^{TE}$  and  $\Phi_{Si}^{TE}$  where  $W_{si} = W_{match} = 295nm$ , while *B* is the phase-matched point for  $\Phi_{III-V}^{TE}$  and  $\Phi_{Si}^{TM}$  ( $W_{si} = 235nm$ ), *C* is the phase-matched point for  $\Phi_{III-V}^{TM}$  and  $\Phi_{Si}^{TM}$  ( $W_{si} = 325nm$ ), *D* is the phase-matched point for  $\Phi_{III-V}^{TM}$  and  $\Phi_{Si}^{TE}$  ( $W_{si} = 355nm$ ). To avoid the risk of coupling to TM-like modes, the tapered coupler should include point *A* but exclude *B* and *C*. From this we derive the conditions  $235nm < W_1 < 275nm$ ,  $315nm < W_2 < 325nm$ .

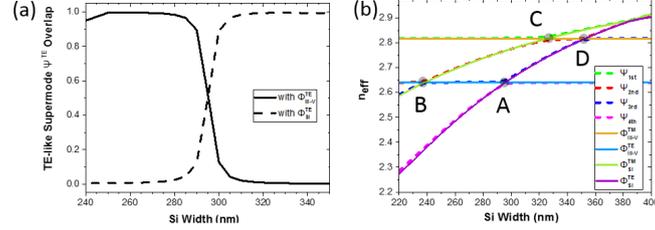


Figure 3. (a) The overlap of mode  $\Psi_+^{TE}$  with modes  $\Phi_{III-V}^{TE}$  (solid line) and  $\Phi_{Si}^{TE}$  (dashed line) as a function of  $W_{si}$  at  $W_{Gap} = 240nm$ . (b) The effective refractive index  $n_{eff}$  of the TE/TM-like ground modes of the separated III-V/Si WGs and of the first four supermodes.

### 3.2 Tapered Coupler Length

Figure 4(a) shows the coupling efficiency to the modes  $\Phi_{Si}^{TE}$ ,  $\Phi_{Si}^{TM}$ ,  $\Phi_{III-V}^{TE}$  and  $\Phi_{III-V}^{TM}$ , when the taper is excited by the mode  $\Phi_{III-V}^{TE}$ , as function of taper length  $L$ , whereby  $W_2$  and  $W_1$  are chosen to be their smallest possible values of  $W_1 = 275nm$  and  $W_2 = 315nm$  respectively. At  $W_{Gap} = 240nm$ ,  $L = 310\mu m$ , the coupling efficiency from  $\Phi_{III-V}^{TE}$  to  $\Phi_{Si}^{TE}$  reaches as high as 98%. Most of the remaining 2% of the power couples to the  $\Phi_{Si}^{TM}$  mode in Si. Figure 4(b) shows how the optical power is exchanged between the III-V nano-ridge and the Si WG and Figure 4(c) shows a 2D image of the optical power evolution along the coupler.

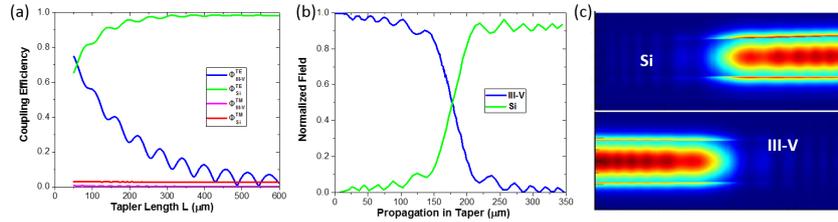


Figure 4. (a) Coupling efficiency as function of taper length  $L$ . (b) Power exchange between III-V nano-ridge and Si WG along propagation direction when  $L = 310\mu m$ . (c) The top-view 2-D image of optical power evolution along the coupler when  $L = 310\mu m$ .

## 4 CONCLUSION

This paper proposes a novel adiabatic coupler working in the O-band for the adiabatic mode conversion from a GaAs nano-ridge laser to a Si waveguide. The Si waveguide is compatible with our earlier presented process for the direct epitaxy of GaAs on silicon and requires no extra effort to fabricate. We show that a directional coupler design can reach a coupling efficiency of 100% but is sensitive to process and wavelength variations. To improve this, the design of a more robust tapered coupler is presented, which is more tolerant to process variations and can still achieve 98% coupling efficiency. The designed adiabatic coupler is expected to facilitate the interface between epitaxially grown active III-V devices and passive Si devices on the same substrate, opening the road towards the incorporation of III-V components in future Silicon Photonics platforms.

## ACKNOWLEDGMENT

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