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Transfer printing for heterogeneous silicon PICs

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Abstract

Photonic integrated circuits (PICs), implementing optical functions such as light generation, modulation, routing and detection on a single chip, are emerging as a powerful platform to realize miniaturized optical systems. These chips find applications in various fields, ranging from high-speed optical transceivers to disposable bio-sensors, LiDARs for detection and ranging, spectroscopic analytical sensors, etc.

Silicon photonics is the field that is using silicon fabrication technologies, developed over the last decades for advanced electronic integrated circuits, to realize PICs. Using this approach advanced PICs can be realized on 200mm or 300mm wafers in high volume and at low cost. On the silicon photonics platform many device structures are readily available: Si or SiN waveguides, micro-heaters for tuning/switching, Si or Ge based modulators and photodetectors. However, other optical functions such as light generation require the integration of III-V semiconductors on the silicon wafers. This can be realized using different approaches ranging from hybrid assembly over die-to-wafer bonding to monolithic integration. Every approach has its advantages and disadvantages. An interesting approach that we are developing is the use of micro-transfer-printing technology for the integration of III-V semiconductor devices on a silicon photonic wafer, which is a scalable and minimally-invasive approach. The technique is illustrated in Fig. 1 (for the specific case of III-V devices).

a) III-V Device Layer Release layer Substrate	b) Patterned device Petterned release layer Substrate	c) Fatterned device Patterned device Patterned release layer Substrate	source III-V wafer with fully processed III-V devices released from their substrate	target SiPh wafer
d) Patterned device Release Substrate	e) Manup Substrate	f) Stamp Sillicon		

Fig. 1 (left) process flow for the realization of III-V coupons on a III-V source wafer; (right) illustration of the parallel transfer-printing-based integration on a SiPh wafer.

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However, the approach is not limited to III-V semiconductors. It can be applied to any material system that can be released from its substrate. This includes for example Si/Ge diode structures, Si-based electronics (when fabricated on SOI), 2-dimensional materials such as graphene and films of quantum dots. All together these materials/devices enhance the silicon photonics platform by enabling new optical functions or improving the performance of existing functions. An overview of some device integration results are shown in Fig. 2

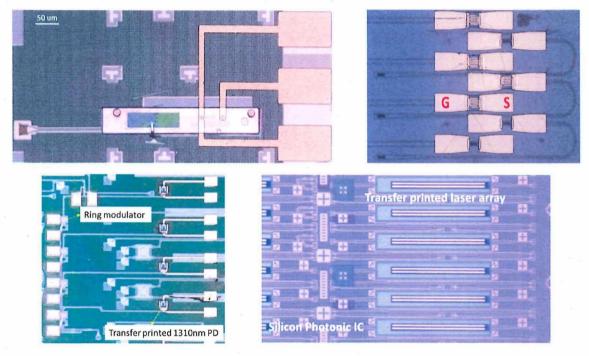


Fig. 2 (top) transfer-printed waveguide-coupled Ge PDs and GaAs metalsemiconductor-metal PDs integrated on a passive waveguide circuit; (bottom) InPbased p-i-n photodetectors and etched facet lasers integrated on a silicon PIC.

Conclusion

While still being a young technology we believe this integration approach has many advantages for the realization of heterogeneous silicon photonic integrated circuits, and will enable a further miniaturization of optical system with a wide range of applications, especially in the context of smart sensor solutions.

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