Scaling up Silicon Photonic Circuits: Where are the Challenges?

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***Abstract*—Silicon photonics fabrication technology allows large scaling of photonic circuits. But the scaling is limited by the design process for large interconnected circuits, and the operation of circuits with inherently imperfect and nonuniform building blocks.**

Keywords—silicon photonics, large-scale integration, design, photonic-electronic integration

I. Introduction

In the past decade, silicon photonics has rapidly grown into an accepted technology: there are multiple commercial fabs and publicly accessible research foundries, the first silicon photonics products have entered the market, and silicon photonics is generally considered as the technology that will enable scaling of photonic circuits for higher-bandwidth interconnects as well as a variety of applications in sensing, spectroscopy, medical diagnostics and optical information processing. The material system and the fabrication process can enable that scaling, up to 10000-10000 optical elements on a single chip [1].

II. Interconnectivity

However, when we look at silicon photonic circuits today, we see that the individual building blocks usually have a high performance, but the circuits are generally very simple: 'large scale integration' goes not much further than repeating an identical circuit many times over the chip. The chips can have a very high raw performance, but the functionality is generally quite limited. If we make the comparison with electronics, the functionality of the circuit has less to do with the performance of the individual transistors than with the interconnectedness of the many electronic gates. The level of interconnection in electronics is much higher than in today's electronics. True large-scale photonic integration will require this interconnectivity to fully realize the potential of silicon photonics.

Denser connectivity will also address a latent risk of today's silicon photonic circuits: reliability. As circuit complexity increases, the risk of a catastrophic failure of a single element goes up. Higher connectivity, together with configurability, can be used to implement redundancy and fault tolerant photonic circuits.

III. Design and Control

The fabrication technology to implement such larger circuits is here. While the adapted CMOS processes are still being improved continuously, it is not limiting the integration of these many components. The challenges lie in the design and the operation of such large circuits [2]. To integrate 10000s interconnected photonic elements in a circuit, fast circuit simulators with accurate circuit models are needed. These models need to capture sufficient richness of the optical behavior: in particular the effects of small parasitic reflections can propagate throughout a circuit and become increasingly problematic in larger circuits. It is an illusion that these will be completely eliminated in fabrication, so they should be anticipated during the design phase. Similarly, the fabrication technology will never be able to guarantee uniformity at a sub-nm level between subcircuits, dies, wafers and batches. The design tools need to capture those effects and estimate circuit yield. Design techniques to mitigate the effect of variability (e.g. linewidth-tolerant designs) can help there as well.

A silicon photonic circuit should not be regarded as a standalone chip. In practice, the optical circuit will be complemented by analog electronic drivers, digital control loops and software. These elements can no longer be considered fully decoupled: the operation of a silicon chip, with its control logic, should be incorporated into the design process. This requires design automation tools that span the gap between photonics and electronics design, going to reusable 'photonic' library elements or IP blocks that comprise a complete photonic, analog, digital and software stack.

IV. Conclusion

The scaling up of silicon photonics will rely on the ever-improving fabrication technology, but the key to scaling will be to unlock the interconnectivity. And the challenges there are situated more in the realm of design automation and control logic.

References

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