Design and fabrication of type-II InP-based lasers and photodetectors integrated on SOI waveguide

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We present the design and fabrication of 2 µm wavelength range type-II InP-based lasers and photodetectors integrated on a silicon photonic circuit. "W"-shaped type-II InGaAs/GaAsSb quantum wells are used as active region in the laser and photodetector structures. In order to achieve high efficient mode coupling, a taper structure in both the III-V waveguide and silicon waveguide is used. An anisotropic wet etching is used to fabricate a very narrow inverted taper tip. The integration of type-II lasers and photodetectors on a silicon photonic integrated circuit using the same III-V epitaxial stack for laser and detector enables the realization of a completely integrated spectroscopic sensor.

Introduction

In recent years, the 2 µm wavelength range is of enormous spectroscopic interest as a lot of gases and molecules have strong absorption signatures in this wavelength range [1]. Besides, this wavelength range has also shown potential for the next generation of communication systems [2]. Silicon photonics platform can be used to fabricate low cost passive photonic components (e.g., low-loss waveguide, grating coupler and multiplexer) since it can take advantage of standard complementary metal-oxidesemiconductor (CMOS) process technology. However, some drawbacks of using silicon for 2 µm wavelength range are that it is indirect band gap semiconductor materials and its band gap is around 1.1eV. So, how to realize the light sources and photodetectors integration on silicon become the most key problems for silicon photonics in 2 µm wavelength range. To overcome these drawbacks, epitaxial growth of strain-relaxed GeSn on silicon substrate can be used to achieve direct band gap group IV semiconductor materials and extend the light emission and detection wavelength to 2 µm wavelength range [3]. Another alternative method is heterogeneous integration of direct-bandgap III-V lasers on silicon [4]. For 2 µm wavelength range, type-I GaSbbased heterostructure and InP-based type-II heterostructure can be used to design lasers and photodetectors [5].

In this paper, firstly, we present the design of type-II InP-based lasers and photodetectors integrated on a silicon photonic circuit for 2 μ m wavelength range. An adiabatic taper in both the III–V and silicon waveguide is proposed to achieve an efficient coupling between the silicon waveguide and type-II quantum well. Afterwards, we shown the fabrication process flow of the integrated devices based on this design.

Devices Design

The schematic of the cross section of the integrated type-II lasers and photodetectors on silicon-on-insulator (SOI) can be seen in Figure 1. The III-V layer stack consists of a *p*-InGaAs contact layer, a *p*-InP cladding layer, an active region consists of six pairs of InGaAs/GaAsSb multiple quantum well (MQW) sandwiched between two separate confinement heterostructure (SCH) layers, and an n-InP contact layer. The silicon waveguide is a 400 nm thick rib waveguide with 180 nm deep etch. The III-V epitaxial stack is bonded on the silicon waveguide circuit by adhesive Benzocyclobutene (DVS-BCB) bonding.



Fig.1. Schematic of cross section view of the integrated type-II lasers and photodetectors on SOI.

The energy band diagram of the active region quantum well is shown in Figure 2. Each quantum well consists of one GaAsSb layer confining the holes, surrounded by two InGaAs electron confining layers. The "W"-shaped periods of quantum well are separated by tensile strained $GaAs_{0.58}Sb_{0.42}$ layers, which can be used to avoid wave functions coupling to a broad miniband. The "W"-shaped structure is designed here to increase the overlap between the wave functions of electron and hole states in the type-II quantum well, which can improve the gain of laser and MQW absorption coefficient. The spatially indirect transition makes that type-II quantum well photodetectors can detect longer wavelengths than devices based on a type-I heterostructure.



Fig.2. Energy band diagram of a "W"- shaped type-II quantum well.

For the hybrid III-V laser and photodetector on SOI, a high optical gain in the III-V active region and efficient coupling between the III-V active region and the silicon waveguide are the main targets in our optical design. The laser wavelength can be selected by distributed feedback gratings in the silicon waveguide, which is not discussed in this paper. The design of the gain and coupling section in the hybrid laser and photodetector is schematically illustrated in Figure 3. The laser structure can be divided into three sections. The center of the device provides the optical gain, where the

optical mode is completely confining in the 5-6 μ m wide III-V mesa and 9.8% confining in the quantum well. This optical coupling is realized using two sections of III-V/silicon spot-size converter structures defined by tapering both III-V and silicon waveguide. In the first III-V taper section, the width of III-V waveguide linearly quickly reduces to 1 μ m, where the optical mode is still completely confined in the III-V waveguide as shown in Figure 3(b). The optical mode gradually couple to silicon waveguide in the second taper section by slowly tapering III-V waveguide from 1 μ m to 0.5 μ m while the silicon waveguide tapering from 0.3 μ m to 1.5 μ m, as shown in Figure 3(c). The coupling efficiency is higher than 90% for the adiabatic taper 0.5 μ m taper tip. In the 0.5 μ m wide III-V taper tip, the optical mode is completely coupled down to silicon waveguide as shown in Figure 3(d). For the hybrid photodetector, the light couples from silicon waveguide to III-V active region by tapering III-V waveguide and then absorbed and converts to current in the type-II quantum well. More than 95% of the light is absorbed in the 150 μ m long III-V waveguide using a 0.5 μ m taper tip and an absorption coefficient of 1000 cm⁻¹ as shown in Figure 3(e).



Fig. 3. Top view of the integrated InP-based type-II laser and photodetector on SOI.

Devices Fabrication

The SOI waveguide fabrication is carried out in imec's CMOS pilot line on a 200 mm SOI wafers. Rib waveguides are etched 180 nm deep in 400 nm thick silicon device layer. The III-V epitaxial stack is bonded onto the silicon waveguide circuit by adhesive bonding using a 100 nm thick DVS-BCB bonding layer. After bonding, the InP substrate is removed by pure HCl solution. Then the III-V waveguide and taper is defined on a SiNx hard mask, followed by ICP etching to etch through the InGaAs contact layer and 1:1 HCl: H₂0 solution to etch *p*-InP cladding layer. The anisotropic HCl wet etching of InP creates "V"-shaped sidewall when the waveguide is oriented along the [01-1] direction. Afterward, SiN_x is deposited on the sample to cover the *p*-InP cladding layer sidewall to protect the III-V taper in the following wet etching and passivate the thick cladding layer. The SCH and MQW layers are etched by a H₃PO₄: H₂O₂: Citric Acid: H₂O 1:1:20:70 solution, which has a high etching selectivity (~250:1) of GaAsSb to n-InP. Then, different devices are isolated by 1:1 HCl: H₂0 solution etching of *n*-InP layer. After III-V wet etching processes, Ni/Ge/Au is deposited as n-contact. Afterwards, DVS-BCB is spin coated on the sample and curing at 250 °C for 1.5h to passivate the devices. Then, reactive ion etching (RIE) is used to etch DVS-

BCB to open windows for the *p*-contact and n-contact. In the end, Ti/Au is deposited on the n-contact and *p*-contact as probe pad. Figure 4(a)-(h) schematically illustrated the hybrid lasers and photodetectors processes flow. A scanning electron microscope (SEM) image of the device taper tip cross section is shown in Figure 4(k).



Fig.4. (a)-(h) Process flow, (k) SEM image of the cross section of the III-V taper tip.

Conclusion

A general overview of the design and fabrication of InP-based type-II hybrid lasers and photodetectors on SOI is presented in this contribution. The integration of type-II lasers and photodetectors using the same III-V epitaxial stack enable completely integrated absorption spectroscopy systems on a chip.

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