IIIV/Si Hybrid Integrated Devices for Optical Interconnect

Kaixuan Chen[a], Yuntao Zhu[a], Jianxin Chen[a], Qiangsheng Huang[b], Xin Fu[b,c], Jianhao Zhang[b], Yaocheng shi[b], Jin Liu[a], Günther Roelkens[c] and Liu Liu[a,*]

[a]SCNU-ZJU Joint Research Center of Photonics, Centre for Optical and Electromagnetic Research, South China Academy of Advanced Optoelectronics, Science Building No. 5, South China Normal University, Higher-Education Mega-Center, Guangzhou 510006, China;

[b]Centre for Optical and Electromagnetic Research, JORCEP [Sino-Sweden Joint Research Center of Photonics], Zhejiang Provincial Key Laboratory for Sensing Technologies, East Building No. 5, Zijingang Campus, Zhejiang University, Hangzhou 310058, China;

[c]Photonics Research Group, Department of Information Technology, Ghent University-IMEC, Ghent 9000, Belgium

ABSTRACT

We discuss our view of the on-chip optical interconnect infrastructure for future multi-core processers based on wavelength-division-multiplexing (WDM) and our recent results on some key devices for such structures. Cascading performance of various wavelength multiplexers and de-multiplexers including arrayed waveguide gratings (AWGs) and echelle gratings based on the silicon-on-insulator platform are discussed and compared. IIIV based electro-absorption (EA) modulators on silicon realized through benzocyclobutene (BCB) adhesive bonding are analyzed. Ultra short adiabatic taper based mode converters between passive and active structures are designed. The integration of multi-channel modulators, detectors and wavelength de-multiplexers is realized.

Keywords: optical interconnect, wavelength division multiplexer, hybrid integration, electro-absorption modulator

1. INTRODUCTION

Given the increasing demands on interconnects, traditional electrical interconnects has encountered a bottleneck on speed and power consumption [1], which forms a barrier for further improving high-performance multi-core processors in next generation supercomputers. Optical interconnects can offer better performance considering the above aspects [2]. Due to the compatible fabrication processes with Complementary Metal Oxide Semiconductor technology, silicon photonics has drawn much attention towards large scale integration of photonic devices [3]. Multifunctional, high-speed, and highly-integrated photonic circuits built on silicon have been demonstrated recently, which shows a great potential for next generation on-chip optical interconnect [4, 5].

The on-chip optical interconnect infrastructure we propose to implement is shown in Fig.1, where a photonic layer is built on a multi-core processor. Each core is connected through optical interface modules (including modulators, detectors, and wavelength multiplexers/de-multiplexers) and a central switching fabric. In this paper, we will focus on the optical transceiver module. To increase the total transmission rate, a wavelength division multiplexer (WDM) scheme is adopted with 6 different wavelength channels. A modulator or a detector is implemented on each wavelength channel in the transmitter part and the receiver part, respectively. The data rate of each wavelength channel is designed to be 30Gb/s, and thus a one-way aggregated interconnect rate of 180Gb/s in one physical waveguide channel can be realized between processer cores. Due to fabrication errors and temperature variations, the center wavelengths of a multiplexer are inclined to vary from the designed values. Poor cascading performances of the multiplexer at the transmitter part and the de-multiplexer at the receiver part, such as high insertion loss and large cross talk, can be the result. In this paper, various cascading multiplexers and de-multiplexers including AWGs and echelle gratings on the silicon-on-insulator (SOI) platform are designed, fabricated, and compared, in order to obtain the optimized component structure which would give the best performance to the WDM system in the proposed on-chip optical interconnect. The

*liu.liu@coer-scnu.org; phone +86-20-34725186 ext. 8306; fax +86-20-34728410

shallowly etched reflection-type AWGs has shown the best cascading performance yielding a 10dB insertion loss with ±1dB non-uniformity, as compared to the cascaded echelle gratings and the deeply etched transmission-type AWGs, which show an 11dB insertion loss with ±2dB non-uniformity and a 13dB insertion loss with ±3dB non-uniformity, respectively.

IIIV based EA modulators utilizing the quantum-confined Stark effect of a multiple quantum well (MQW) structure on silicon have been developed for applications beyond 50 Gb/s [6], which is also adopted in this paper for realizing both modulators and detectors. Hybrid integration technology through BCB adhesive bonding is employed to integrate the IIIV structures on the SOI circuits. Ultra short adiabatic tapers for mode conversion between the SOI waveguide and the hybrid active structure are designed. Over 95% coupling efficiency with a tapered coupler of less than 10μm length can be realized.

An interconnect link consisting of two 6-channel AWGs with 1.6nm channel spacing and 12 EA-based modulators and detectors is fabricated on an SOI chip. A data rate of 30Gb/s in both modulation and detection channels is measured with a clear eye open.

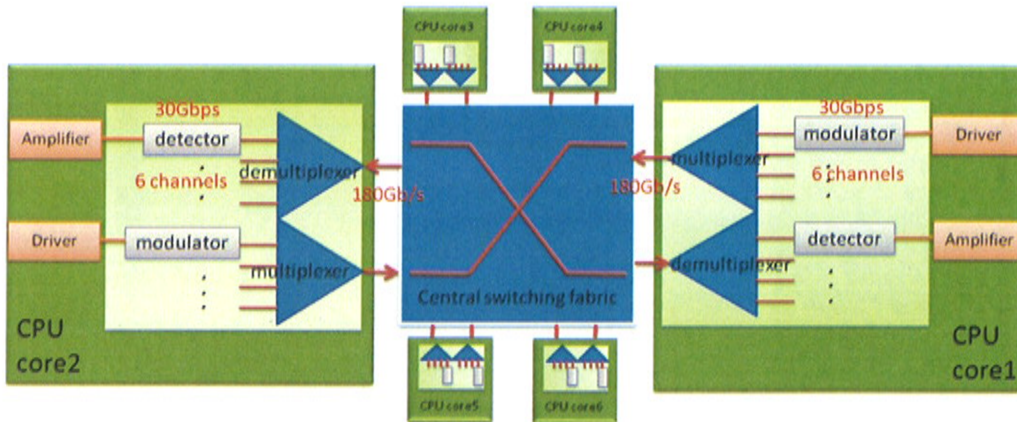

Figure 1. Sketch of the proposed WDM based on-chip optical interconnect system.

2. COMPARISON OF CASCADING PERFORMANCE OF (DE)MULTIPLEXERS ON SILICON

Using WDM is an effective way to expand the bandwidth of a single waveguide channel in an on-chip optical interconnect. Integrated silicon photonic devices to realize a high bandwidth multiplexing/de-multiplexing function mainly include AWGs, echelle gratings, micro ring resonators (MRR). Due to the high insertion loss of MRR [7], we focus on AWGs and echelle gratings as the WDM component of the proposed on-chip interconnect system. The alignment of center wavelengths between the multiplexer and the de-multiplexer, as well as the channel uniformity, within one interconnect is very important. The misalignment of center wavelengths can lead to high insertion loss in the cascaded multiplexer/de-multiplexer. Meanwhile, the channel non-uniformity of a single (de)multiplexer would further increase the insertion loss, as well as large channel non-uniformity, when cascaded. Here, three types of WDM devices based on deeply-etched transmission-type AWGs (T-AWGs), echelle gratings, and shallowly-etched reflection-type AWGs (R-AWGs) on SOI with 400GHz channel spacing are fabricated with electron-beam lithography and dry etching. Their cascading performances are studied.

We have achieved ultra-small 15×15 deeply-etched T-AWGs recently [8], but there is no report about the cascading performance of such AWGs so far. We designed and fabricated standalone T-AWGs and pairs of cascaded ones where the two T-AWGs, used as a multiplexer and a de-multiplexer, respectively, are connected by SOI waveguides. All the T-AWGs are on the same silicon chip and have 8 channels at 400GHz channel spacing. From Fig.2 (a), one can find that the misalignment of center wavelengths of two standalone T-AWGs can be as large as 0.4nm. An insertion loss of about 5dB and a channel non-uniformity of larger than 6dB can also be observed. This large wavelength misalignment causes a

high insertion loss of 13dB and a channel non-uniformity of ±3dB when cascading this type of T-AWGs for wavelength multiplexing and de-multiplexing as shown in Fig. 2(b).

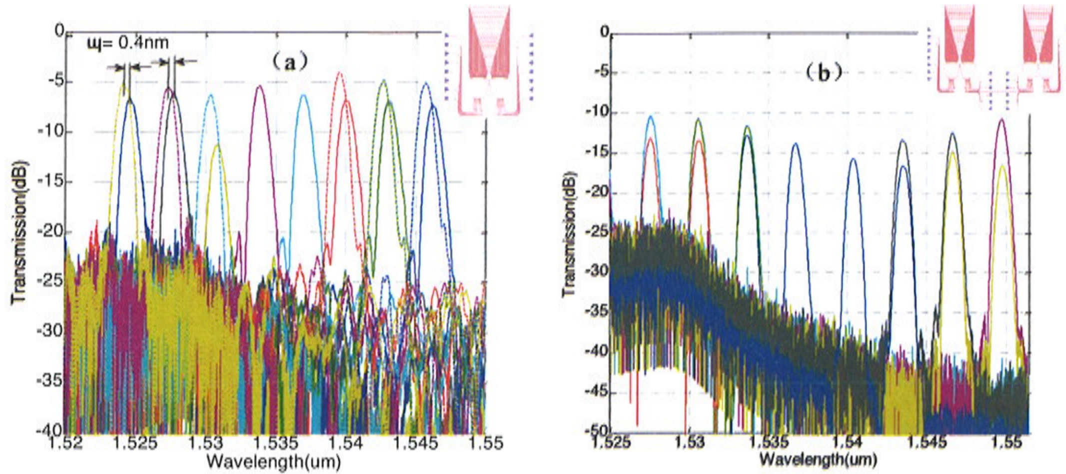

Figure 2. (a) Measured spectra of two single deeply-etched T-AWGs of 8 channels. The solid curve is for a standalone T-AWG, and the dotted curve is for one T-AWG in the cascading case, where only 6 channel outputs are present since the other two channels are used for cascading. (b) Measured spectra of cascading T-AWGs. Insets show the corresponding mask layouts.

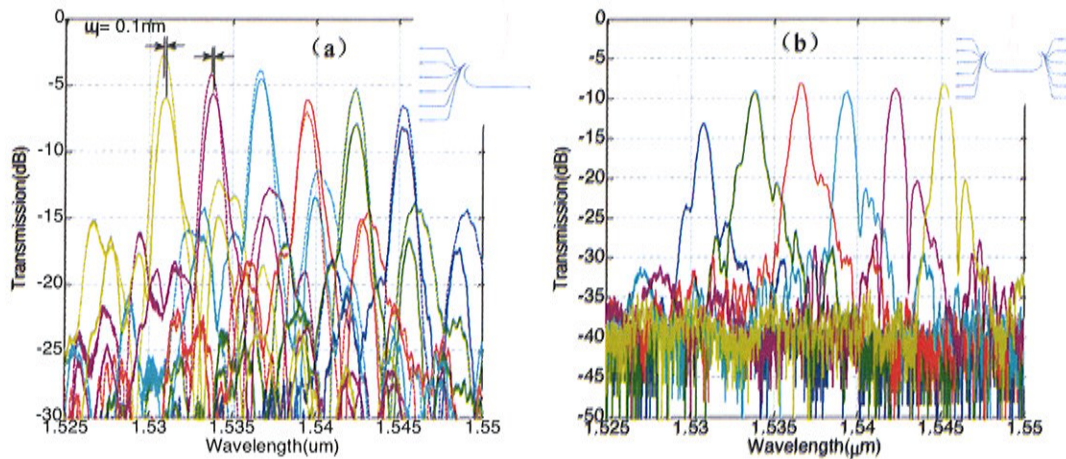

Figure 3. Measured spectra of (a) two standalone echelle gratings of 6 channels and (b) cascading echelle gratings. Insets show the corresponding mask layouts.

Echelle gratings are also a candidate for integrated multiplexer/de-multiplexers in WDM applications. As compared to AWGs, echelle gratings can offer potentially smaller device footprints and a higher integration density for devices with large channel counts [9]. 6-channel standalone and cascading echelle gratings with shallowly etched access waveguides and deeply etched grating reflection facet are also fabricated in the same chip. A shown in Fig. 3(a), the misalignment of the center wavelengths of two standalone echelle gratings is only about 0.1nm and the insertion loss is about 6dB with a non-uniformity of 4dB. As a result, in the cascaded case an insertion loss of 11dB and a channel non-uniformity of ±2dB can be achieved (see Fig.3 (b)), which is better than those in the cascaded deeply etched T-AWGs shown previously.

To further improve the cascading performance, all shallowly etched R-AWGs with straight arrayed waveguides (see Fig.4) were designed [10]. The straight arrayed waveguides in the R-AWGs are formed by etching 70nm on the 200nm

thick top silicon layer, which is the same etch depth as the reflection DBR at the end of each waveguide. The all shallow etching process, the shortening of the arrayed waveguides, and the one free-propagation-region (FPR) structure effectively reduce the accumulation of phase errors [11], and thus stabilizes the center wavelengths. The side lobes and crosstalk are also suppressed. Figure 4 shows the cascading performance of the shallowly etched R-AWGs. An insertion loss of 10dB and a channel non-uniformity of ±1dB are measured. A cascade crosstalk of about -25dB can also be achieved.

Comparing the three structures, the R-AWG structure shows the best performance in cascading. Due to the two FPR and deeply-etched waveguide structure, the T-AWGs need a high process consistency, which induces a low reproducibility. On the other hand, there is only one FPR in the echelle grating and R-AWG cases. The shallow etching process of shorter and straight arrayed waveguides makes the R-AWGs more tolerant on fabrication errors. This reduces the accumulation of phase errors, and thus lowers the insertion loss and provides good channel uniformity.

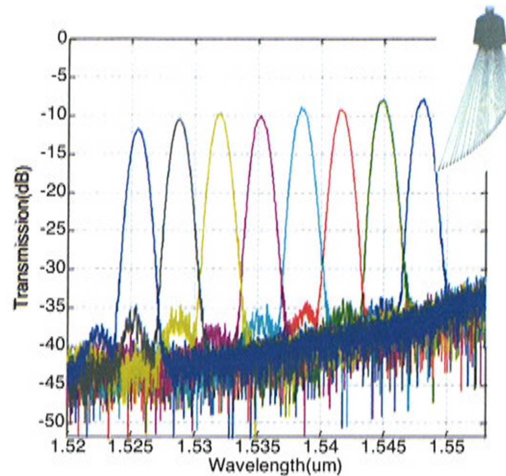

Figure 4. Transmission spectra of cascading shallowly etched R-AWGs. Inset shows the mask layout.

3. ULTRA SHORT ADIABATIC TAPERS FOR MODE CONVERSION BETWEEN PASSIVE AND ACTIVE STRUCTURES

Among various Si/IIIV hybrid integrated devices, a common critical issue is to design a compact mode coupler structure to efficiently route light between the hybrid active section (normally thick to feature vertical electrical injection) and the silicon waveguide (normally thin for single-mode operation). An adiabatic taper has been considered an optimal structure for a mode converter, given its low insertion loss, low reflection losses, and good fabrication tolerance [12].

We propose an ultracompact bi-sectional adiabatic tapered coupler consisting of two linear tapered sections only in the IIIV structure, and the underneath SOI waveguide is kept straight with a common dimension of 600nm×220nm. The bi-sectional tapered coupler mimics a semi-3D taper, which avoids exciting high-order modes in the thick p-cladding layer. Figure 5(a) shows the cross-sectional view of the Si/IIIV hybrid section. Here, the silicon waveguide is kept untapered throughout the whole structure, and the BCB layer thickness h_{BCB} is chosen to be 50nm, which is a common value in the BCB adhesive bonding technology. The IIIV epi-layer structure in Ref. [6] is also adopted here for realizing modulators and detectors. Figure 5(b&c) show a sketch of the proposed bi-sectional tapered coupler, as well as the definition of various parameters. Those parameters are optimized numerically, and the results are listed in Tab. 1. The total length of the tapered section is 9.5μm. The light propagation in this 9.5μm-long tapered coupler is shown in Fig. 6(b). The fundamental mode coupling efficiency reaches 95% over a wide wavelength range. As a comparison, in Fig. 6(a), a conventional single-section taper design with the same taper parameters is also simulated. The only difference is that the thick p-cladding layer covers the whole taper. The coupling efficiency in this case is only 83%. One can see obviously that high-order modes are exited in the thick p-InP cladding layer along the taper.

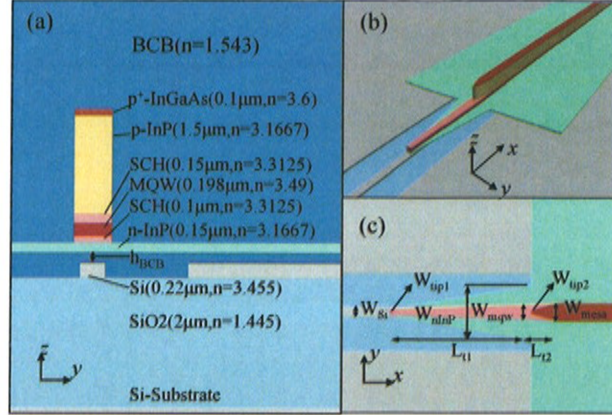

Figure 5. (a) Cross-sectional view of the hybrid Si/III-V waveguide. (b) 3D and (c) top view of the bi-sectional adiabatic tapered coupler, respectively.

Table 1. Optimized parameters of the tapered coupler.

Parameter	L_{t1}	L_{t2}	W_{mqw}	W_{Si}	W_{tip1}/W_{tip2}	W_{nInP}	W_{mesa}
(μm)	7.5	2	0.8	0.6	0.2	3	1

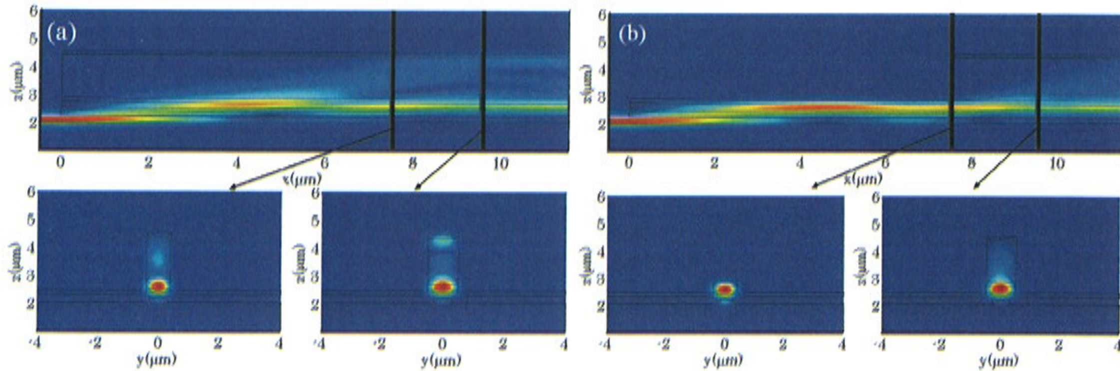

Figure 6. Light propagation in (a) the conventional taper with the p-cladding all over the taper and (b) the proposed bi-sectional tapered coupler. Field profiles at the end of the first tapered coupler and the second tapered coupler are also shown.

4. THE INTEGRATION OF MULTI-CHANNEL MODULATORS, DETECTORS, AND WAVELENGTH (DE)MULTIPLEXERS

Based on the scheme shown in Fig.1, we have fabricated 4 groups of such WDM based on-chip optical interconnect systems integrated with 6 EA modulators and 6 detectors in each wavelength channel. The mask layout is shown in Fig. 7, together with some pictures of the fabricated chip. The channel spacing of the wavelength multiplexer is 1.6nm. An external tunable laser is used as the light source, which is input to the chip through grating couplers. An Anritsu pattern generator and a radio frequency amplifier are used to drive the modulator with a V_{pp} of ~1.5V. After multiplexing and de-multiplexing, the optical signal is launched to the detector which has the same structure as EA modulator, and is then analyzed by an Agilent digital sampling oscilloscope. In between the multiplexer and de-multiplexer, a small portion

(5%) of the multiplexed signal is drawn out from the bus waveguide and routed directly off chip for monitoring, as well as for analyzing the EA modulators and detectors separately.

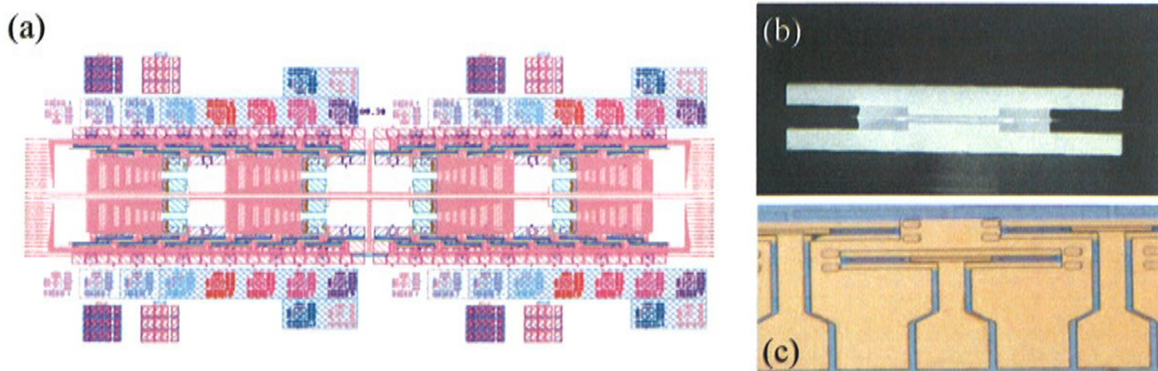

Figure 7. (a) Mask layout of the optical interconnect chip. (b) Fabricated hybrid active section just before the over-cladding deposition. (c) Finished modulator/detector.

Figure 8(a) shows the measured eye pattern of one EA modulator through the aforementioned monitoring channel. An erbium doped fiber amplifier is used to amplify the output signal. The EA modulator is driven at 30Gb/s with nonreturn to zero code of 2^7-1 pseudo random bit sequence. A clear eye open can be observed. The on-chip detector performance was also measured through the monitoring channel by using an external commercial modulator. The result is shown in Fig. 8(b), which shows a similar behavior as that of the EA modulator.

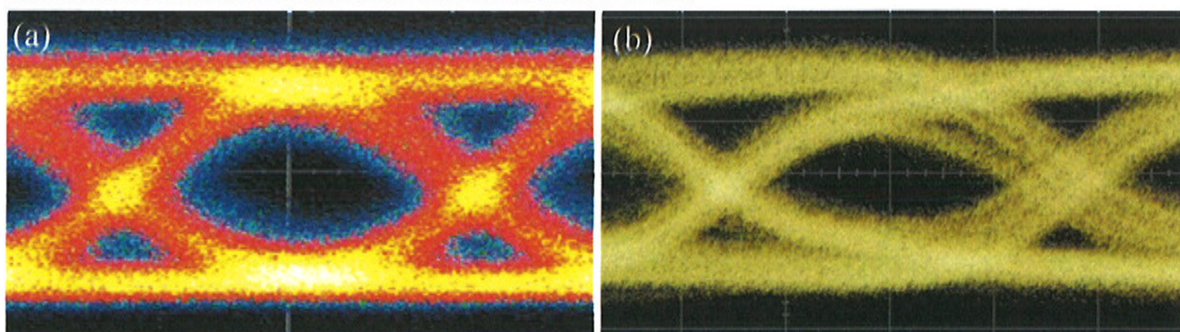

Figure 8. Measured eye patterns for (a) the EA modulator and (b) the detector. Data rate is at 30Gb/s.

5. CONCLUSIONS

In this paper, the cascading performance of various wavelength multiplexers and de-multiplexers including AWGs and echelle gratings realized on SOI are discussed and compared. The shallowly etched R-AWGs show the best cascading performance with 10dB insertion loss with ±1dB non-uniformity. An ultracompact bi-sectional adiabatic tapered coupler is proposed, which can give a 95% coupling efficiency between the SOI waveguide and the hybrid active section with a taper length of 9.5μm. A WDM based on-chip optical interconnect system integrated with 6 EA modulators and 6 detectors in each wavelength channel is fabricated. The modulators and the detectors share the same structure. A data rate of 30Gb/s for both modulation and detection is measured with a clear eye open.

ACKNOWLEDGEMENT

This research is partially supported by 863 project (Ministry of Science and Technology of China, #2012AA011001), National Nature Science Foundation of China (#61107020), and the Guangdong Innovative Research Team Program (#201001D0104799318).

REFERENCES

[1] Gaburro, Z., Optical interconnect, [Silicon Photonics], edited by L. Pavesi and D. J. Lockwood, Springer-Verlag, Berlin, 121-171 (2004).

[2] Goodman, J. W., Leonberger, F. J., Kung, S.-Y., and Athale, R. A., "Optical interconnections for VLSI systems." Proc. IEEE 72, 850-866 (1984).

[3] Bogaerts, W., Baets, R., Dumon, P., Wiaux, V., Beckx, S., Taillaert, D., Luysseart, B., Van Campenhout, J., Bienstman, P., and Van Thourhout, D., "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," J. Lightwave Technol. 23(1), 401-412 (2005).

[4] Alduino, A., Liao, L., Jones, R., Morse, M., Kim, B., Lo, W., Basak, J., Koch, B., Liu, H., Rong, H., Sysak, M., Krause, C., Saba, R., Lazar, D., Horwitz, L., Bar, R., Litski, S., Liu, A., Sullivan, K., Dosunmu, O., Na, N., Yin, T., Haubensack, F., Hsieh, I., Heck, J., Beatty, R., Park, H., Bovington, J., Lee, S., Nguyen, H., Au, H., Nguyen, K., Merani, P., Hakami, M., and Paniccia, M. J., "Demonstration of a High Speed 4-Channel Integrated Silicon Photonics WDM Link with Hybrid Silicon Lasers," Integrated Photonics Research, Silicon and Nanophotonics (IPRSN), PDIWI5, (2010).

[5] Urino, Y., Shimizu, T., Okano, M., Hatori, N., Ishizaka, M., Yamamoto, T., Baba, T., Akagawa, T., Akiyama, S., Usuki, T., Okamoto, D., Miura, M., Noguchi, M., Fujikata, J., Shimura, D., Okayama, H., Tsuchizawa, T., Watanabe, T., Yamada, K., Itabashi, S., Saito, E., Nakamura, T., and Arakawa, Y., "First demonstration of high density optical interconnects integrated with lasers, optical modulators and photodetectors on single silicon substrate," Opt. Express 19(26), B159-B165 (2011).

[6] Tang, Y., Chen, H.-W., Jain, S., Peters, J. D., Westergren, U., and Bowers, J. E., "50 Gb/s hybrid silicon traveling-wave electroabsorption modulator," Opt. Express 19(7), 5811–5816 (2011).

[7] An, J., Zhang, J., Wang, Y., Wang, L., Pan, P., and Qi, Y., "Study on Wavelength Division Multiplexer for Silicon Photonics," Laser & Optoelectronics Progress, 11, 59-64 (2014).

[8] Fu, X., and Dai D., "Ultra-small Si-nanowire-based 400 GHz-spacing 15×15 arrayed-waveguide grating router with microbends," Electronics letters 47(4), 266-268 (2011).

[9] Bogaerts, W., Selvaraja, S. K., Dumon, P., Brouckaert, J., Vos, K. D., Van Thourhout, D., Baets, R., "Silicon-on-insulator spectral filters fabricated with CMOS technology," IEEE journal of selected topics in quantum electronics 16(1), 33-44 (2010)

[10] Ma, K., Huang, Q., Zhang, J., Chen, S., Fu, X., Dai, D., Shi, Y., Chen, K., Chen, J., Liu, L., and He, S., "Fabrication of all shallowly etched silicon reflection-type arrayed-waveguide gratings with one stigmatic point," ACPC, AF3B.5 (2014).

[11] Okamoto, K., and Kenzo, I., "Fabrication of silicon reflection-type arrayed-waveguide gratings with distributed Bragg reflectors," Optics letters 38(18), 3530-3533 (2013).

[12] Wang, Q., Ng, D. K. T., Wang, Y., Wei, Y., Pu, J., Rabiei, P., and Ho, S. T., "Heterogeneous Si/III-V integration and the optical vertical interconnect access," Opt. Express 20(15), 16745-16756 (2012).

CREATE AN ACCOUNT | SIGN IN

ABOUT SPIE | CONTACT US | HELP | SHOPPING CART

SPIE.
CONNECTING MINDS.
ADVANCING LIGHT.

SPIE is the international society for optics and photonics.

SEARCH

HOME CONFERENCES + EXHIBITIONS PUBLICATIONS EDUCATION MEMBERSHIP INDUSTRY RESOURCES CAREER CENTER NEWS + VIDEOS

Your Selections

Query Term

IIIV/Si Hybrid Integrated Devices for Optical Interconnect

Clear All Refinements

Refine this search

Category

Profiles (4)
Publications (1)

Product Type

All Products (1)
Technical Articles (1)

Product Format

Hard Copy (1)

Content Type

All Content (1)
People (4)

Technologies & Applications

Demultiplexers (1)
Equipment and services (1)
Multiplexers (1)
Sensors (1)
Wavelength division multiplexing (1)

5 search results for:

IIIV/Si Hybrid Integrated Devices for Optical Interconnect

Display: 20 per page Sort By: Relevance

PROCEEDINGS PAPER • NEW

IIIV/Si hybrid integrated devices for optical interconnect

Kaixuan Chen, Yuntao Zhu, Jianxin Cheng, ZJU-SCNU Joint Research Ctr., South China Normal Univ. (China); Qiangsheng Huang, Sino-Swedish Joint Research Ctr. of Photonics, Zhejiang Univ. (China); Xin Fu, Sino-Swedish Joint Research Ctr. of Photonics, Zhejiang Univ. (China)Univ. Gent (Belgium); Jianhao Zhang, Yaocheng Shi, Sino-Swedish Joint Research Ctr. of Photonics, Zhejiang Univ. (China); Jin Liu, ZJU-SCNU Joint Research Ctr., South China Normal Univ. (China); Günther Roelkens, Univ. Gent (Belgium); Liu Liu, ZJU-SCNU Joint Research Ctr., South China Normal Univ. (China)

Published in Proceedings Volume 9366: Smart Photonic and Optoelectronic Integrated Circuits XVII
February 2015 • Hide Abstract

We discuss our view of the on-chip optical interconnect infrastructure for future multi-core processers based on wavelength-division-multiplexing (WDM) and our recent results on some key devices for such structures. Cascading performance of various wavelength multiplexers and de-multiplexers including arrayed waveguide gratings (AWGs) and echelle gratings based on the silicon-on-insulator platform are discussed and compared. IIIV based electro-absorption (EA) modulators on silicon realized through benzocyclobutene (BCB) adhesive bonding are analyzed. Ultra short adiabatic taper based mode converters between passive and active structures are designed. The integration of multichannel modulators, detectors and wavelength de-multiplexers is realized.

Available on the SPIE Digital Library

PROFILE
Mr. Qiangsheng Huang
Zhejiang Univ.

PROFILE
Miss Xin Fu
Zhejiang Univ.

PROFILE
Mr. Kaixuan Chen
South China Normal Univ.

PROFILE
Prof. Gunther Roelkens
Univ. Gent

Copyright © 2015 SPIE

About SPIE | Author Information | Privacy Policy | Sitemap | SPIEDigitalLibrary.org