High-Q Photonic Crystal Nanocavities on 300 mm SOI Substrate Fabricated With 193 nm Immersion Lithography

Weiqiang Xie, Martin Fiers, Shankar Selvaraja, *Member, IEEE*, Peter Bienstman, *Member, IEEE*,
Joris Van Campenhout, *Member, IEEE, Member, OSA*, Philippe Absil, and Dries Van Thourhout, *Member, IEEE*

Abstract—On-chip 1-D photonic crystal nanocavities were designed and fabricated in a 300 mm silicon-on-insulator wafer using a CMOS-compatible process with 193 nm immersion lithography and silicon oxide planarization. High quality factors up to 10^5 were achieved. By changing geometrical parameters of the cavities, we also demonstrated a wide range of wavelength tunability for the cavity mode, a low insertion loss and excellent agreement with simulation results. These on-chip nanocavities with high quality factors and low modal volume, fabricated through a high-resolution and high-volume CMOS compatible platform open up new opportunities for the photonic integration community.

Index Terms—CMOS, nanocavities, photonic crystal (PhC), silicon-on-insulator (SOI).

I. INTRODUCTION

PHOTONIC CRYSTAL (PhC) cavities have been investigated intensively during recent years. Compared with conventional optical resonators, owing to the existence of a band gap, these PhC cavities can strongly confine light both on a temporal and on a spatial scale, thus enabling both ultra-high quality factors (Q) and ultra-small cavity modal volumes (V). This unique property of PhC cavities allows effectively controlling the lifetime and the density of photons and strongly boosting light-matter interaction inside cavities, which is essential to manipulate light at extremely low power levels or at ultra-fast speed. Therefore, the use of PhC cavities has been proposed in the context of several innovative photonic applications such as ultra-low threshold lasers [1]–[3], ultra-fast optical switching and modulation [4], dynamic control of light [5], [6], and the study of cavity quantum electrodynamics [7]. Among currently investigated PhC cavities, one-dimensional (1-D) PhC

nanocavities, since their first emergence [8], have a simpler structure and are more compact compared to higher dimensional PhC cavities, and therefore, have drawn a lot of interest recently [9]–[14]. High Q and extremely low V have been demonstrated in these 1-D PhC nanocavities both numerically and experimentally [9]–[12]. In spite of their structural simplicity, the fabrication of 1-D PhC nanocavities still remains a challenge because of their minimal feature size and rigorous requirements with respect to fabrication imperfections. Most successful demonstrations [9]–[14] thus far relied on high-resolution electron beam lithography but because of its slow throughput this approach is likely to be limited to research or small volume applications. Today's well-developed complementary metal-oxide-semiconductor (CMOS) platform on the other hand is compatible with high-volume fabrication and also may offer the possibility for ultra-compact, chip-scale integration of PhC-based optical components with existing optical devices and even electronics. Indeed, over the past decade, we have witnessed successful fabrication of many optical building blocks for photonic circuitry based on a silicon-on-insulator (SOI) platform, using standard CMOS fabrication technologies. Consequently, there is a need to develop PhC-based building blocks, for instance PhC cavities, employing a CMOS compatible process. Thus far, the performance of such qualities was limited, mostly by the patterning resolution provided by the lithography tools used, based on 193 or 248 nm DUV [15], [16]. In this study, we show the successful realization of on-chip 1-D PhC nanocavities integrated with out-of-plane grating couplers, fabricated on a 300 mm SOI wafer in a CMOS pilot line using 193 nm immersion lithography. We experimentally demonstrate high-Q factors in these on-chip 1-D nanocavities and good correspondence with simulations. Furthermore, by changing geometrical parameters of the cavities, we have achieved a wide tuning of resonance wavelength and a low insertion loss. The reliability of the fabrication of SOI PhC nanocavities using a CMOS platform is also discussed.

II. DESIGN SOI NANOCAVITIES

The design of our 1-D SOI PhC nanocavity is based on the mode-gap modulation approach [9], [12], in which the mode gap of the quasi-1-D PhC waveguide is modulated by structural parameters such as the lattice constant, the hole size or the width of the PhC waveguide. Through this mode gap modulation, a cavity mode can arise from the lower-lying dielectric band of
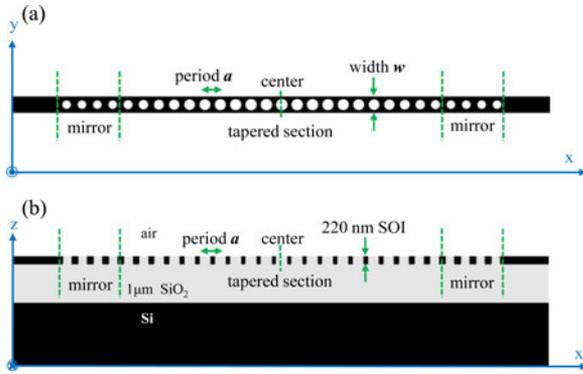
Fig. 1.   Schematics of 1-D SOI PhC nanocavity with circular holes embedded in silicon oxide matrix, consisting of the tapered and mirror sections. The whole structure is symmetric with respect to the cavity center. (a) Top and (b) x–z plane views of the cavity.

Fig. 2.   Band diagram for the SOI PhC waveguides (inset for the schematic) consisting of a period-a ($a = 400$ nm) sequence of circular holes with radius of $r = 0.22a$ and $r = 0.30a$, respectively. The width of waveguide is $w = 440$ nm. Only fundamental TE-like bands are plotted in the irreducible Brillouin zone. (The light cone is shaded light blue, bounded by the black-colored light line of air cladding.) The straight dot line denotes the frequency position of the resonant mode for the cavity in which the hole of $r = 0.30a$ serves as the cavity center and the holes of $r = 0.22a$ as the mirror.

a PhC waveguide in the modulated region (defect region), and subsequently, it is localized within the band gap provided by a periodic PhC mirror. Since the band gap of a 1-D PhC waveguide is incomplete, for a certain localized mode within the gap there always exists intrinsic radiative loss, which is detrimental to accomplishing a high-Q cavity. In 1-D nanocavities, typically most of the radiative loss is caused by the mismatch [9] between the guided mode of the defect section (wire waveguide mode or PhC Bloch mode, depending on the type of defect) and the mode of the PhC mirror section. This mode mismatch can be minimized by replacing the abrupt interface from the defect to the mirror by a gradual transition of the geometric configuration. In this way, the radiative losses can be dramatically reduced, resulting in a high-Q cavity.

In our design, we start with a quasi-1-D PhC strip waveguide structure with periodic circular holes, and then, gradually decrease the radius of the holes from the center symmetrically to the two mirror arms for which the holes have a terminating radius value. The radius is parabolically tapered from its maximum to minimum value, in the same manner as was implemented in [12]. Fig. 1(a) and (b) shows the detailed structure of the 1-D SOI cavity, which is composed of a 1-D PhC waveguide with circular holes etched in a 220 nm-thick silicon layer lying on top of a 1 μm buried silicon oxide layer. The holes are back-filled with silicon oxide through a combination of SiO_2 deposition and chemical mechanical polishing (CMP), resulting in a planar surface. Note that this structure might be quite advantageous in some applications, for example, to integrate active materials with the cavity. The period of the PhC lattice, defined as the center-to-center distance between two holes, is fixed at $a = 400$ nm. The radius of the holes is parabolically tapered by reducing the radius from $0.30a$ for the center hole to $0.22a$ for the mirror holes, leaving four holes as cavity mirror with constant radius of $0.22a$ at each side of the cavity. The total number of holes is fixed to 29 in our design to allow easy coupling between the cavity and access waveguides during measurement. On the mask, we varied the width of the cavity w, from 460 to 580 nm and also scaled the radius of the holes with various scaling factors (SF) from 0.8 to 1.2, in order to study
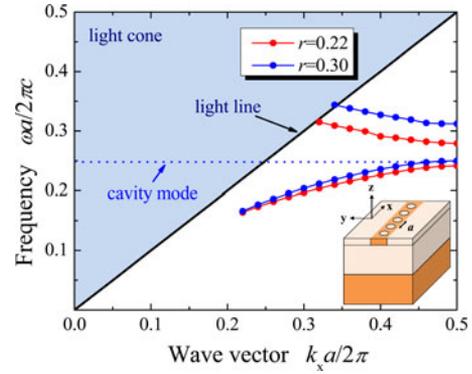
the dependence of the resonant mode wavelength and Q on the width of the cavity and the size of the holes.

To analyze the SOI cavity numerically, we computed both the band diagram for the associated PhC periodic waveguide and the resonant mode of the cavity with the t3-D finite-difference time-domain (FDTD) method, using a freely available software package [17]. In Fig. 2, we present the band diagram for the circular-hole PhC waveguides with two different radii $r = 0.22a$ and $r = 0.30a$, respectively. The width of the waveguide is fixed at $w = 440$ nm. It is clear that this PhC waveguide exhibits a large mode gap between the fundamental TE-like bands and that the gap remains well below the light cone, potentially providing strong confinement for a cavity mode lying within this gap. The dotted line in Fig. 2 denotes the fundamental transverse-electric (TE) like cavity mode calculated for the cavity design of Fig. 1, taking into account a width of 440 nm and a radius scaling factor SF of 1.0. We observe that the frequency of this cavity mode almost overlaps with the edge of the lower band of the PhC waveguide with $r = 0.30a$, as shown in the corresponding band diagram in Fig. 2. It is also clear that the cavity mode is well localized within the band gap of the PhC waveguide with $r = 0.22a$ that is used as the mirror section of the cavity. According to the aforementioned numerical analysis, one can easily understand that in the cavity design based on the mode-gap modulation approach the cavity mode is originally formed from the Bloch mode of the lowest TE-like band of the center PhC waveguide, and then, is confined within the mode gap of the PhC mirror. By changing the radius of the holes or the width of the cavity, we can further tune the frequency of the resonant mode as well as the position of the band gap of the mirror section.

Next, we performed comprehensive FDTD simulations for PhC cavities with width w varying from 400 to 580 nm and with the radius SF varying from 0.8 to 1.3 for each width. Employing a 29-hole design, we found that these SOI cavities can support a fundamental mode with resonance wavelength varying from
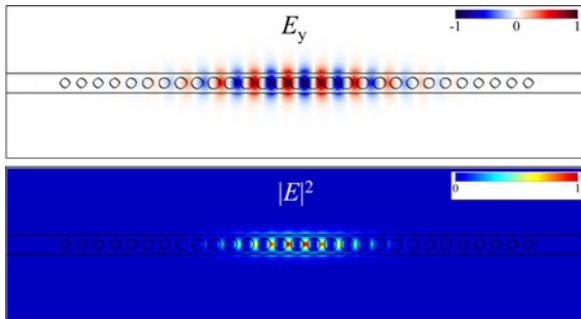
Fig. 3. Normalized electric field (E_y) and field intensity ($|E|^2$) of the fundamental cavity mode.

Fig. 4. SEM images of fabricated SOI nanocavity: (a) top view of the whole cavity, (b) enlarged view of holes, and (c) FIB cross-sectional image of a circular hole.

1450 to 1650 nm and a Q-factor as high as 1.0×10^5 and V as small as $0.6(\lambda/n)^3$ can be readily realized with appropriate geometrical parameters of the cavity. Note that the total number of holes in our cavities is only 29 (including four mirror holes at both sides), and that they are embedded in an oxide matrix on an SOI substrate with only a 1 μm buried oxide layer. This leads to a slight leakage of the cavity mode into the bottom silicon substrate. When adding more mirror holes to reduce the waveguide loss and suspending the cavity in air, one can easily obtain simulated quality factors Q of up to 10^7. In Fig. 3, we present the electric field profiles (E_y component and $|\boldsymbol{E}|^2$) of the fundamental mode for the cavity with parameters of $w = 500$ nm and SF $= 1.2$. It is obvious that the fundamental cavity mode is a TE-like mode, where E_y is dominant and that the light field is highly localized around the center of the cavity with a modal volume of $0.6(\lambda/n)^3$.

III. CHARACTERIZATIONS AND DISCUSSIONS

The complete fabrication process was carried out on a 300 mm SOI wafer in a CMOS pilot line. The devices were patterned with 193 nm deep ultraviolet immersion lithography and a dry etch process using a Si_3N_4 hard mask. Next the devices were planarized through silicon oxide deposition (using a high-aspect ratio filling process) and a CMP process. In the future, this planarization step might allow for straightforward integration with optically active materials. Fig. 4 shows the scanning electron microscope (SEM) and focused ion beam (FIB) cross-sectional images of the fabricated SOI nanocavity with silicon oxide lateral cladding. Note that the cavity is embedded in an oxide matrix and that the FIB cross section in Fig. 4(c) was taken along the dashed line indicated in Fig. 4(b) under the protection of two layers of platinum (Pt) deposited *in situ* by electron beam an ion beam, respectively. It can be seen that the cavity is well-defined in the silicon layer. The etched holes have nearly vertical sidewalls, an important requirement for PhC-based devices. Thanks to the high-aspect ratio filling process all holes are completely filled and the wafer exhibits a smooth top surface.

Due to a lithography-to-dry etch process bias, the holes experienced a dimensional gain compared to the design, while the waveguides shrunk in width. To allow a quantitative comparison of fabricated and designed devices, we determined the actual dimensions of cavities with various width and radius SF
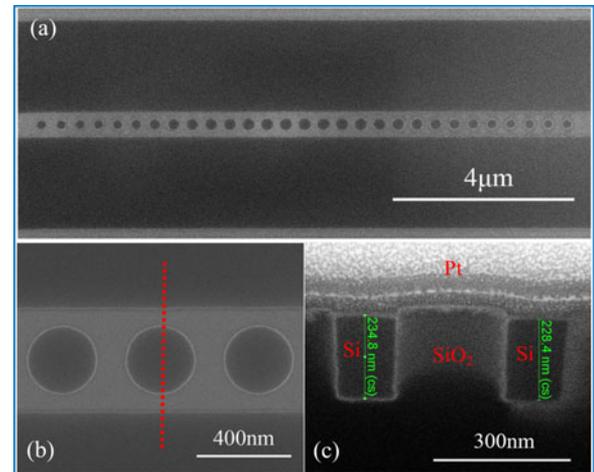
using top–down SEM. Statistically, an average 60 nm reduction in width and 0.2 offset in SF is observed after fabrication. This means, for the designs of width from 460 to 580 nm and SF from 0.8 to 1.1, the real width and SF of the fabricated cavities range from 400 to 520 nm and from 1.0 to 1.3, respectively. Accordingly, for both the simulated and measured results mentioned later, actual values for width and SF as measured from the fabricated devices will be used.

To allow direct optical characterization, the 1-D PhC nanocavities are integrated with out-of-plane grating couplers optimized for TE polarization. We measured the transmitted spectra of the cavities with a resolution of 1 pm by using tunable lasers covering a wavelength range from 1470 to 1640 nm, and the transmittance is obtained by normalizing these spectra to a reference waveguide. The experimental Q-values of these nanocavities were extracted by fitting the resonance peak with a Lorentzian line shape, namely, $Q = \lambda_c/\Gamma$, where λ_c and Γ are the associated resonance wavelength and linewidth of the cavity mode, respectively. The input power was attenuated to ~ 0.1 μW, to suppress thermo-optic effects.

First, in order to study the dependence of cavity mode and Q on the size of the PhC holes, we measured a group of cavities with the same width $w = 440$ nm but various radius scaling factors SF of 1.0, 1.1, 1.2, and 1.3, and plot their transmittance spectra and the associated fits for the fundamental modes in Fig. 5(a). The changes of the resonance wavelength λ_c and quality factor Q with the different SF are plotted in Fig. 5(b). It is obvious that the resonance peak and Q of the cavities are very sensitive to the SF and that the peaks shift to shorter wavelength when increasing the SF. This can be explained from the inset band diagram of the PhC waveguide in Fig. 5(a). As analyzed previously in Fig. 2, the resonance frequency of the fundamental mode in our 1-D cavity is principally determined by the position of the lowest TE-like band of the central PhC waveguide. When increasing the radius of the hole in the center, for instance from $r = 0.30$ to $0.36a$ (i.e., SF from 1.0 to 1.2) the lowest TE-like band of the PhC waveguide is simultaneously pushed up toward
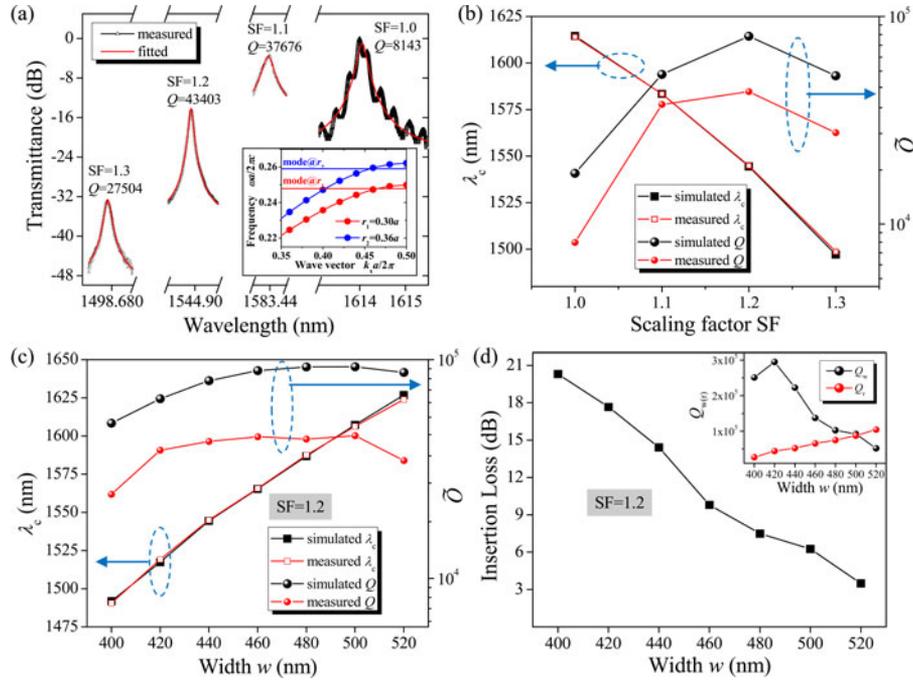
Fig. 5.   (a) Measured and fitted transmittance spectra for the fundamental modes of the cavities with $w = 440$ nm and various SF. (The inset shows the calculated lowest TE-like bands of the PhC waveguides with $r = 0.30a$ and $r = 0.36a$, respectively.) (b) Simulated and measured resonance wavelength (λ_c) and Q factor from (a) as a function of SF. (c) Simulated and measured λ_c and Q as a function of the width w of the cavities with a fixed SF = 1.2, and (d) measured insertion loss for different w. (The inset shows the extracted waveguide Q_w and radiation Q_r versus the width w.)

higher frequency, as distinctly shown in the inset band diagram in Fig. 5(a). As a consequence, the mode position blue-shifts for the corresponding cavity as denoted by the straight lines in the inset. As seen in Fig. 5(b), with the SF increasing from 1.0 to 1.3, the resonance wavelength decreases almost linearly with the SF, exhibiting a wavelength shift of ∼3.2 nm/nm change in hole radius. Fig. 5(b) also shows that a maximum Q is obtained for a SF of 1.2, which also can be explained in terms of the band gap of the 1-D PhC. When increasing the SF of the cavity, one can push the cavity mode closer to the middle of the band gap supplied by the PhC mirror, where the mode is expected to be confined more strongly. Further increasing the SF to 1.3, however, reduces the confinement again and increases the radiative loss in the cavity thereby reducing the Q. Thus, at an optimal SF of 1.2, we obtained a maximum Q in the cavity. In Fig. 5(b), we also present the FDTD simulated results for the resonance wavelength λ_c and Q for different SF and find an excellent agreement between the measured and simulated results. The remaining discrepancy between the measured and simulated Q can be attributed to structural imperfections in the sidewalls of the waveguide and holes, and loss mechanisms including scattering.

Next, we investigated the influence of the width of the cavities on the resonance wavelength λ_c and Q factor of the cavity modes, as presented in Fig. 5(c). Obviously, with increasing the cavity width at a fixed SF, λ_c exhibits a linear redshift at a rate of 1.1 nm-redshift per nanometer of increasing width. The measured Q, however, remains as high as 4.0×10^4 for a broad range of widths, a behavior also seen for the simulated Q. This property is very important for practical applications where the ability to tune the resonance wavelength while preserving a

high Q is essential. Again, we compare the results of the measured and simulated λ_c versus the width w in Fig. 5(c) and find that the shift of the measured λ_c agrees well with the simulated result. This, together with the results shown in Fig. 5(b) for tuning of the SF, demonstrates the excellent correspondence between the measured and simulated operating wavelength, taking into account a reduction of 60 nm in width and 0.2 bias in SF as explained before. This in turn demonstrates the accuracy and reliability of CMOS technology for the fabrication of PhC nanocavities.

For practical applications, both high Q and low insertion loss are needed. Therefore, we measured the insertion loss, determined from measuring the transmission normalized with respect to a reference waveguide, for cavities with various widths. As shown in Fig. 5(d), the insertion loss decreases when increasing the cavity width. For cavities with a width $w > 420$ nm, the insertion loss is below 10 dB, while the Q for these cavities still remains as high as 4.0×10^4. To understand this, one can separate the total cavity loss (corresponding to the total Q) into the radiation loss and the waveguide loss, both corresponding to the quality factors of the radiation Q_r and waveguide Q_w, respectively. In our symmetrical 1-D cavity, the total Q can be expressed as $1/Q = 1/Q_r + 1/Q_w$, and the maximum transmission at the cavity resonance λ_c is given by $T(\lambda_c) = (Q/Q_w)^2$ [18]. From the two equations aforementioned, we can extract Q_r and Q_w separately, which are plotted in the inset of Fig. 5(d). In the expression of $T(\lambda_c)$, the value of peak transmission is determined by the proportion of the Q_w in the total Q. When the total quality factor Q is limited by the waveguide losses (namely when $Q_r > Q_w$), then more energy

of the cavity mode is coupled to the access waveguide than is being coupled to radiation loss, resulting in a higher peak transmission (for $Q_r \gg Q_w$, T approaches 100%), and thus, a low insertion loss. From the inset of Fig. 5(d), we can indeed see how the competition between Q_r and Q_w influences the insertion loss when increasing the width. When $Q_r > Q_w$, the measured insertion loss decreases below 4 dB in our cavities. It should be noted that the Q and the insertion loss can be readily engineered by adjusting the geometrical parameters of the cavity. For instance, by reducing the radius of the holes or by removing some mirror holes, a moderate Q ($\sim$10000) and an even higher transmission ($\sim$100%) can be accomplished, which could be desired for certain applications. Finally, it is important to note again that the on-chip 1-D SOI cavities discussed earlier all are embedded in an oxide matrix. As mentioned already, from simulations, we expect a considerably higher Q-factor for a suspended cavity in air. We verified this by removing the oxide matrix (including the oxide filling the holes) as well as the bottom oxide using an HF-dip. In that case, a Q of 1.1×10^5 is easily attained, and thereby, actually reaches the same level as the values reported for 1-D nanocavities fabricated by electron beam lithography [12]. Furthermore, it is worth noting that the cavity designs were repeated over the whole 300 mm SOI wafer. The results discussed above were from a randomly selected die on the wafer. We also measured the Q and resonance wavelength of cavities from different other regions of the wafer and found that the uniformity in Q and resonance wavelength was excellent with a maximum $\sim$16% variation of measured Q and about $\pm$6 nm resonance wavelength shift over the wafer, which means that both the throughput and the quality of the fabrication of nanocavities can be guaranteed in this fabrication process.

IV. CONCLUSION

We designed and fabricated on-chip 1-D PhC nanocavities on a 300 mm SOI wafer using advanced CMOS-compatible processes, including 193 nm immersion lithography. SEM and optical transmission characterization of these compact PhC nanocavities revealed a high quality in terms of fabrication accuracy and a high Q factor of 4.5×10^4 (1.1×10^5 without oxide) together with a low insertion loss. Study of the dependence of the resonance wavelength on the actually fabricated cavity width and hole radius showed an excellent agreement between the measured and simulated results. This also means the small deviation in fabricated and originally designed dimensions can be easily compensated for in future runs through introducing a small design bias. The high performance of the cavities demonstrated here reveals the suitability of advanced high-volume CMOS processes for fabricating compact high-Q nanocavities. These nanocavities potentially form a promising building block for realizing densely integrated photonic circuitry on the SOI platform.

ACKNOWLEDGMENT

REFERENCES

[1] S. Matsuo, A. Shinya, T. Kakitsuka, K. Nozaki, T. Segawa, T. Sato, Y. Kawaguchi, and M. Notomi, "High-speed ultracompact buried heterostructure photonic-crystal laser with 13 fJ of energy consumed per bit transmitted," *Nature Photon.*, vol. 4, no. 9, pp. 648–654, 2010.

[2] B. Ellis, M. A. Mayer, G. Shambat, T. Sarmiento, J. Harris, E. E. Haller, and J. Vuckovic, "Ultralow-threshold electrically pumped quantum-dot photonic-crystal nanocavity laser," *Nature Photon.*, vol. 5, no. 5, pp. 297–300, 2011.

[3] Y. Takahashi, Y. Inui, M. Chihara, T. Asano, R. Terawaki, and S. Noda, "A micrometre-scale Raman silicon laser with a microwatt threshold," *Nature*, vol. 498, no. 7455, pp. 470–474, 2013.

[4] K. Nozaki, A. Shinya, S. Matsuo, Y. Suzaki, T. Segawa, T. Sato, Y. Kawaguchi, R. Takahashi, and M. Notomi, "Ultralow-power all-optical RAM based on nanocavities," *Nature Photon.*, vol. 6, no. 4, pp. 248–252, 2012.

[5] T. Tanabe, M. Notomi, E. Kuramochi, A. Shinya, and H. Taniyama, "Trapping and delaying photons for one nanosecond in an ultrasmall high-Q photonic-crystal nanocavity," *Nature Photon.*, vol. 1, no. 1, pp. 49–52, 2007.

[6] M. Notomi, E. Kuramochi, and T. Tanabe, "Large-scale arrays of ultrahigh-Q coupled nanocavities," *Nature Photon.*, vol. 2, no. 12, pp. 741–747, 2008.

[7] M. Nomura, N. Kumagai, S. Iwamoto, Y. Ota, and Y. Arakawa, "Laser oscillation in a strongly coupled single-quantum-dot-nanocavity system," *Nature Phys.*, vol. 6, no. 4, pp. 279–283, 2010.

[8] J. S. Foresi, P. R. Villeneuve, J. Ferrera, E. R. Thoen, G. Steinmeyer, S. Fan, J. D. Joannopoulos, L. C. Kimerling, H. I. Smith, and E. P. Ippen, "Photonic-bandgap microcavities in optical waveguides," *Nature*, vol. 390, no. 6656, pp. 143–145, 1997.

[9] P. Lalanne, C. Sauvan, and J. P. Hugonin, "Photon confinement in photonic crystal nanocavities," *Laser Photon. Rev.*, vol. 2, no. 6, pp. 514–526, 2008.

[10] P. B. Deotare, M. W. McCutcheon, I. W. Frank, M. Khan, and M. Loncar, "High quality factor photonic crystal nanobeam cavities," *Appl. Phys. Lett.*, vol. 94, no. 12, p. 121106, 2009.

[11] L. D. Haret, T. Tanabe, E. Kuramochi, and M. Notomi, "Extremely low power optical bistability in silicon demonstrated using 1D photonic crystal nanocavity," *Opt. Exp.*, vol. 17, no. 23, pp. 21108–21117, 2009.

[12] E. Kuramochi, H. Taniyama, T. Tanabe, K. Kawasaki, Y. G. Roh, and M. Notomi, "Ultrahigh-Q one-dimensional photonic crystal nanocavities with modulated mode-gap barriers on SiO$_2$ claddings and on air claddings," *Opt. Exp.*, vol. 18, no. 15, pp. 15859–15869, 2010.

[13] W. S. Fegadolli, J. E. B. Oliveira, V. R. Almeida, and A. Scherer, "Compact and low power consumption tunable photonic crystal nanobeam cavity," *Opt. Exp.*, vol. 21, no. 3, pp. 3861–3871, 2013.

[14] P. B. Deotare, L. C. Kogos, I. Bulu, and M. Loncar, "Photonic crystal nanobeam cavities for tunable filter and router applications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 2, Mar./Apr. 2013.

[15] M. Settle, M. Salib, A. Michaeli, and T. F. Krauss, "Low loss silicon on insulator photonic crystal waveguides made by 193 nm optical lithography," *Opt. Exp.*, vol. 14, no. 6, pp. 2440–2445, 2006.

[16] S. K. Selvaraja, P. Jaenen, W. Bogaerts, D. Van Thourhout, P. Dumon, and R. Baets, "Fabrication of photonic wire and crystal circuits in silicon-on-insulator using 193-nm optical lithography," *J. Lightw. Technol.*, vol. 27, no. 18, pp. 4076–4083, Sep. 2009.

[17] A. F. Oskooi, D. Roundy, M. Ibanescu, P. Bermel, J. D. Joannopoulos, and S. G. Johnson, "MEEP: A flexible free-software package for electromagnetic simulations by the FDTD method," *Comput. Phys. Commun.*, vol. 181, no. 3, pp. 687–702, 2010.

[18] J. D. Joannopoulos, S. G. Johnson, J. N. Winn, and R. D. Meade, "Designing photonic crystals for applications," in *Photonic Crystals: Molding the Flow of Light*, 2th ed. Princeton, NJ, USA: Princeton Univ. Press, 2008, p. 210.

Weiqiang Xie received the B.S. degree in applied physics from Xi'an Jiaotong University, Xi'an, China in 2008, and the M.S. degree in condensed matter physics from Shanghai Jiaotong University, Shanghai, China in 2011. He joined the Photonics Research Group in Ghent University, Ghent, Belgium, and IMEC as a Ph.D. candidate in 2011. His research interests include the integration of colloidal quantum dots with silicon and silicon nitride photonics for on-chip visible and infrared light sources.

Martin Fiers completed his studies in electrical engineering at Ghent University, Ghent, Belgium in 2008 and joined the Department of Information Technology (INTEC) at the same university for the Ph.D. degree in photonic reservoir computing. After his graduation in 2013, Martin is working to improve the integrated photonic design cycle by writing software for optical design and modeling. His main interests include the modeling of nanophotonic components and reservoir computing.

Shankar Selvaraja received the M.E. degree in optical communication from the College of engineering, Anna University, Chennai, India, in 2004, the M.Sc. degree in microsystems and microelectronics from the University of Twente, Enschede, The Netherlands, in 2005, and the Ph.D. degree for his work on Wafer-Scale Fabrication Technology for Silicon Photonic Integrated Circuits in 2011. Since then, he has been a Postdoctoral Researcher and now as silicon photonics integration engineer at IMEC, Ghent, Belgium. His research interests include CMOS compatible device, process development, and integration for on-chip optical interconnects. He has authored or coauthored more than 90 journals and peer-reviewed conference articles.

Peter Bienstman was born in Ghent, Belgium, 1974. He received the M.Sc. degree in electrical engineering and the Ph.D. degree from Ghent University, Ghent, in 1997 and 2001, respectively. Currently he is an Associate Professor with the Department of Information Technology, Ghent University. During 2001–2002, he spent a year in the Joannopoulos research group at MIT. His research interests include several applications of nanophotonics (biosensors and photonic information processing) as well as nanophotonics modeling. He has published more than 50 papers and holds several patents. He is a member of the IEEE Photonics Society. He has been awarded the European Research Council starting grant for the Naresco-project: Novel paradigms for massively parallel nanophotonic information processing.

Joris Van Campenhout received the Ph.D. degree in electrical engineering from Ghent University, Gent, Belgium, in2007, for his work on hybrid-integrated III–V microdisk lasers on silicon. He is a Program Manager of IMEC's industry-affiliation program on Optical I/O, which explores silicon-based optical interconnects enabling low-power, high-bandwidth chip I/O in future CMOS nodes. Prior to joining IMEC, he was at IBM T.J. Watson Research Center, New York, NY, USA, where he worked on CMOS-integrated silicon optical switches. He is a member of the IEEE and OSA, and serves as a technical program committee member in OFC/NFOEC, CLEO and IEEE-IPC.

Philippe Absil received the Ph.D. degree in 2000 from the Department of Electrical Engineering, University of Maryland, College Park, MD, USA. His doctoral work contributed to the early demonstrations of semiconductor micro-ring resonators. He is the optical IO program director at IMEC and is responsible for the silicon photonics technology platform development since 2010. Before that, he spent seven years managing the advanced CMOS scaling program at IMEC. In the early 2000s, he developed the passive photonics platform technology for Little Optics Inc., Annapolis, MD.

Dries Van Thourhout received the degree in physical engineering and the Ph.D. degree from Ghent University, Ghent, Belgium in 1995 and 2000, respectively. From 2000 to 2002, he was with Lucent Technologies, Bell Laboratories, Crawford Hill, working on InPInGaAsP monolithically integrated devices. In 2002, he joined the Department of Information Technology (INTEC), Ghent University, continuing his work on integrated optoelectronic devices. His research interests include heterogeneous integration by wafer bonding, intrachip optical interconnect, and WDM-devices.