Effect of Mask Discretization on Performance of Silicon Arrayed Waveguide Gratings

Shibnath Pathak, Michael Vanslembrouck, Pieter Dumon, Dries Van Thourhout, Peter Verheyen, Guy Lepage, Philippe Absil, and Wim Bogaerts

***Abstract*— We studied the impact of the lithography mask discretization on silicon arrayed waveguide grating (AWG) performance. When we decreased the mask grid from 5 to 1 nm, we observed an experimental improvement in crosstalk of 2.7–6 dB and cumulative crosstalk improvement of 1.2–5 dB, depending on the wavelength channel spacing and the number of output channels. We demonstrate the effect for the AWGs with 200- and 400-GHz channel spacing, with 4, 8, and 16 output wavelength channels. With 1-nm mask grid, the average crosstalk is −26 and −23 dB for 400- and 200-GHz devices, respectively. This is the lowest crosstalk for silicon AWGs reported to the best of our knowledge. A simulation study is performed by looking specifically at phase errors due to mask grid snapping (ignoring other phase error sources), which shows an expected improvement in crosstalk of 12 dB.**

***Index Terms*— Nanophotonics, wavelength division multiplexing, optical filters, silicon-on-insulator, silicon devices.**

I. Introduction

ARRAYED waveguide gratings (AWGs) are one of the commonly used photonics integrated components for wavelength de/multiplexing [1]. For WDM communication applications it is desirable to have an AWG with low loss and low crosstalk. This drives research interest to improve the performance of AWGs in various material systems for different wavelength ranges. Any material system imposes design restrictions and/or opportunities for AWGs, largely depending on the refractive index contrast of the waveguides. For instance, in silicon-on-insulator the high contrast waveguides allow sharp bends to reduce the device footprint but they are also extremely sensitive to phase errors, which reduces the margin of error of both the design and fabrication. On the other hand, lower contrast material platforms such as silica [2] and InP [3] are much more relaxed in terms of design and fabrication, but the devices become much larger which reduces the integration density. Other than phase errors, high contrast waveguides typically suffer from higher propagation losses. Despite the higher propagation losses in silicon waveguides, the overall insertion loss of an AWG can be kept reasonably low because of the compact device size. Still, the high phase error sensitivity will increase the overall crosstalk of the silicon AWG, being one of the key factors that limit AWG performance in this material system.

In general, the phase errors of a fabricated AWG are not determined by the design but by fabrication imperfections [4]. The effects of fabrication imperfections on the performance of a silicon AWG can be partly reduced by engineering the design of the AWG [5]–[8]. Still, this works only to a certain extent, as fabrication imperfections are difficult to reduce or remove completely. For instance, mask discretization will inevitably introduce phase errors, as grid snapping will change the length of the waveguides. This mask discretization is entirely dependent on the available mask making technology. In 2001 Chauhan D. Lee pointed out this effect on low contrast AWGs [9]. As low contrast waveguides are less phase error sensitive a larger improvement in the mask technology is needed to significantly improve the crosstalk. In this letter we demonstrate the effect of mask discretization on the performance of silicon AWGs, and experimentally show that a smaller mask grid can result in a dramatic improvement of the crosstalk.

II. Phase Errors

The crosstalk in a silicon AWG is the combined effect of many mechanisms: the phase errors that are accumulated along the delay lines, reflections, defocusing in the free propagation regions (FPR), and cross-coupling in the array. It is not straightforward to separate the contributions of each of these mechanisms, although past experiments have already significantly reduced the contribution of some of these effects. E.g. the effect of reflection were reduced by using double-etched apertures [5].

The key contributor to crosstalk in recent silicon AWGs remain the phase errors [5]–[8], [10], [11]. When the distributed light in the waveguides recombines in the free propagation region (FPR), phase errors will translate in ripples in the optical phase front as shown in Fig. 1. These ripples will induce sidelobes in the image at the output waveguides, resulting in optical power coupled to the wrong outputs. We can separate these phase errors into two categories: deterministic and stochastic errors. In the latter category we find sidewall roughness and linewidth/thickness variations as key causes. Using wider waveguides in the delay sections can alleviate the impact of theses effects [5]–[8]. Mask discretization on the other hand result in deterministic errors.

As the common design of our AWGs uses rectangular 'Manhattan' waveguide paths [5]–[8] where the bend sections

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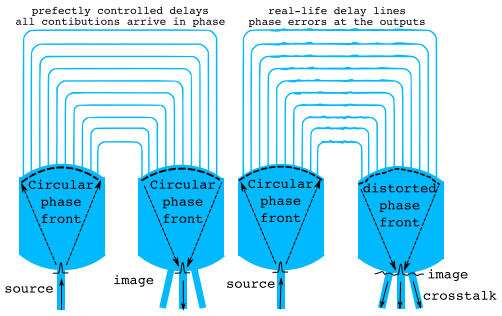

Fig. 1. Schematic diagram of the AWG with ideal delay lines and with phase error affected delay lines.

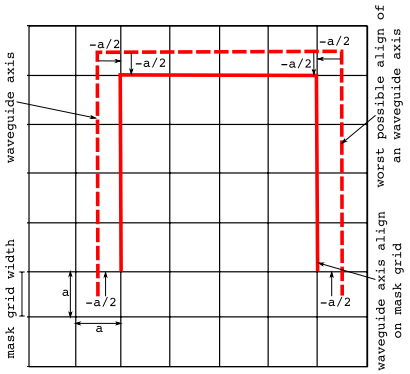

Fig. 2. The length deviation of a waveguides due to the grid snapping.

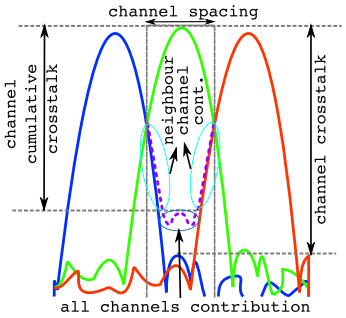

Fig. 3. Definition of different crosstalk of an AWG spectrum.

are identical for all delay lines, we first looked at the effect of the mask grid on the straight delay sections of the AWG. The effect is illustrated in Fig. 2. The path for the delay line is calculated along 3 sides of a rectangle (taking into account the length of the bends). During that calculation, the coordinates of the sides are calculated to high precision. However, during subsequent export to a GDSII mask file, the process is snapped to a fixed grid. In practice, we used a 5 nm grid, which means the length deviation in each waveguide could be up to ± 15 nm, which translates in phase errors of $\pm\pi/19$. By going to a 1 nm grid, these variations drop to ± 3 nm, or phase errors of $\pm\pi/96$. While the grid snapping in our mask design is fairly random (a rounding error depending on the calculated delay length), it is a deterministic process: two identically designed AWGs will experience the same phase error contributions from grid snapping. As an example in Fig. 4 we show the length deviations due to the 1 nm and 5 nm grid over the 72 waveguides of a 16 $\times$ 400 GHz AWG. The maximum and minimum phase errors over the 72 waveguides introduced by the 5 nm grid discretization are

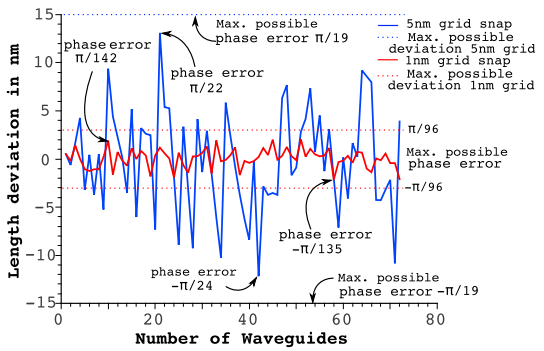

Fig. 4. The length deviation over the waveguides of 16 $\times$ 400 GHz AWG due to 1 nm and 5 nm grid snapping.

$\pi/22$ and $-\pi/24$ respectively, which are reduced to $\pi/142$ and $-\pi/135$ respectively for the 1 nm grid. As the length deviation is not constant over the array quasi-random phase errors will be introduced, which will increase the crosstalk of the device. But the mask discretization will not effect the waveguide width as the waveguide width (800 nm and 450 nm) is an integer multiply of the mask grid width (5 nm and 1 nm) and the waveguide axis is parallel to the mask grid. If the waveguide is at an angle with the grid this can also introduce line width variations depending on the discretization algorithm as well as the mask preparation and writing procedure. To reduce the impact of angled discretization algorithms, we prefer to use Manhattan layouts, which are also very suitable for the silicon waveguides with micrometer-scale bends. We studied the effect of the phase errors through simulation and experimentally, by designing and simulating a set of identical AWGs on both a 1 nm and a 5 nm grid, and fabricating them side-by-side.

Usually the crosstalk of an AWG is characterized by the single channel crosstalk floor which is the crosstalk floor measured with one active input channel. Under operational conditions when all the input channels are active, the crosstalk of all channels (which is further referred to as the cumulative crosstalk) will be added linearly, which results in a much higher effective crosstalk. In Fig. 3 the conventional crosstalk and the cumulative crosstalk of the center channel are indicated: the conventional crosstalk is defined by the difference between the crosstalk floor and the peak power of the channel. We define the cumulative crosstalk as the difference between the peak power in the channel and the cumulative power coupled to the other channels, added up over the wavelength band of the channel. The cumulative crosstalk has two major contributions: at the edges of the wavelength band it is dominated by the slope of the nearest neighbor channel (further referred to as neighboring channel contributed crosstalk) and the center part which is mainly caused by phase errors (further referred to as phase error contributed cumulative crosstalk). The neighboring channel contributed crosstalk depends on the channel bandwidth, which can be decreased by increasing the number of waveguides used in the array [7].

III. Design

To elaborate the effect of mask discretization on the performance of a SOI AWG we designed a set of AWGs with

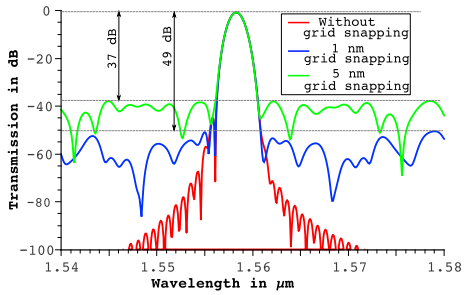

Fig. 5. Simulated transmission spectrum of 16 × 400 GHz AWG (8th channel) for 1 nm, 5 nm and without grid snapping.

4, 8 and 16 wavelength channels AWGs for both 200 GHz and 400 GHz channel spacings. The AWGs were designed for IMEC's passive silicon photonics platform, using a 220 nm thick silicon guiding layer on top of a 2 μm oxide layer using a double etch process: a 220 nm deep etch to define high contrast photonics wires and a 70 nm etch to define grating couplers and low contrast waveguides (also referred as shallow etch). Patterns were defined using 193 nm UV lithography. See [7], [8] for further design details of the SOI AWGs. We used the same design to generate two set of AWGs on the same mask with 1 nm and 5 nm grid snapping. Independent of channel spacing, for the same number of wavelength channels we used the same number of waveguides: 24, 40 and 72 waveguides for 4, 8 and 16 channels AWGs respectively. For an equal number of wavelength channels and an equal number of waveguides the delay length of the 200 GHz device will be twice the delay length of the 400 GHz device. This will increase the influence of phase errors due to the sidewall roughness.

IV. Simulation

The AWGs were simulated using a semi-analytical model [7] integrated in our design software (IPKISS) [12], [13]. As we want to illustrate the effect on the crosstalk due to the phase errors introduced by the grid snapping we didn't include any stochastic phase error due to sidewall roughness in the simulation. Fig. 5 shows the simulated spectral response of the 8th channel of the 16×400 GHz AWG without grid snapping, and for 1 nm and 5 nm snapping. The simulation indicates, as expected, that the insertion loss will not be affected significantly while the crosstalk floor will increase due to the coarser mask grid. In the simulation we can see that the crosstalk is improved by 12 dB as we change the grid from 5 nm to 1 nm. In this simulation, we did not take into account discretization of the waveguide bends. The additional phase errors contributed due to bend discretization will vary depending on the discretization algorithm, as well as the grid.

V. Experiment

We fabricated those devices on a 200mm SOI wafer. They were discretized on a 1 nm and 5 nm grid, and positioned side by side on the same photomask and fabricated together in the same process. To characterize the AWGs the input and output channels are connected to 1D grating couplers and we normalize the transmission spectrum of the AWGs to that of a

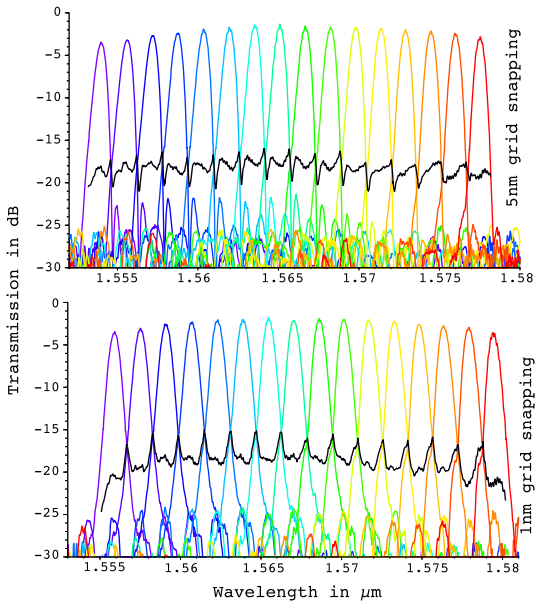

Fig. 6. Experimental transmission spectrum of 16 × 200 GHz AWG using 5 nm and 1 nm grid snapping. Black line indicate the cumulative power of the device.

straight waveguide with the same type of grating couplers. The optical fibers are aligned to the grating couplers with an automated alignment setup, which uses a reproducible and wavelength-corrected algorithm to align with an accuracy of 0.01 μm in X, Y, Z directions.

Figs. 6 and 7 show the measured spectral responses of 16×200 GHz and 16×400 GHz AWGs using 5 nm and 1 nm grid snapping. For the 16×400 GHz AWGs the crosstalk floor drops from −21 dB (for the 5 nm grid) to −26 dB (for the 1 nm grid) [14]. For the 16×200 GHz AWGs the crosstalk floor drops from −19.8 dB (for the 5 nm grid) to −22.5 dB (for the 1 nm grid). We see that the crosstalk is substantially higher than the simulated AWGs, because other crosstalk mechanisms are still present, mainly the phase error contribution of the sidewall roughness, which is also the reason behind the smaller improvement for the 200 GHz device as the delay length is double that of the 400 GHz AWGs: 21.86 μm for 16 × 200 GHz and 10.93 μm for 16 × 400 GHz AWGs. The cumulative crosstalk is −17 dB and −22 dB for 400 GHz AWGs using the 5 nm and 1 nm grid, respectively. For 200 GHz AWGs the cumulative crosstalk improves from −15 dB for 5 nm grid to −17 dB for the 1 nm grid. Figs. 6 and 7 show that for 5 nm grid devices the neighboring channel contributed cumulative crosstalk is almost equal to the phase error contributed cumulative crosstalk as the channel overlap is minimal. For the 1 nm grid the neighboring channel contributed cumulative crosstalk is dominating due to the reduction of the discretization induced phase errors. This neighboring channel contributed cumulative crosstalk can be improved further by increasing the number of waveguides used in the array.

Other AWGs, with different channel counts, show similar improvements as listed in Table I. From Table I we can see that with a fixed number of output channels when we decrease the channel spacing the improvement of the crosstalk reduces because of longer delay length. The situation is much more

TABLE I

COMPARISON OF AWG INSERTION LOSS [(IL), HIGHEST POWER CHANNEL → LOWEST POWER CHANNEL] AND CROSSTALK LEVEL BETWEEN 1 nm AND 5 nm MASK GRID DISCRETIZATION

Channels	Spacing GHz	Area [μm^2]	IL 5 nm [dB]	IL 1 nm [dB]	XT 5 nm [dB]	XT 1 nm [dB]	ΔXT [dB]	CXT 5 nm [dB]	CXT 1 nm [dB]	ΔCXT [dB]	FSR [nm]
4	200	845×243	-1.9→-2.3	-1.7→-2.6	-18.3	-23	4.7	-16.3	-20.5	4.2	9.5
4	400	468×237	-2.2→-2.5	-1.8→-2.2	-21.6	-27	5.4	-20.3	-24.7	4.4	19
8	200	873×308	-1.5→-2.7	-1.9→-3.1	-20.5	-23.6	3.1	-17.8	-19.0	1.2	15.8
8	400	490×307	-2.3→-3.7	-1.3→-2.7	-20	-26	6.0	-17	-21.5	4.5	32
16	200	920×446	-1.6→-3.6	-2.0→-3.7	-19.8	-22.5	2.7	-15	-17	2.0	29
16	400	530×435	-1.5→-3.5	-1.5→-3.5	-21	-26	5.0	-17	-22	5.0	54

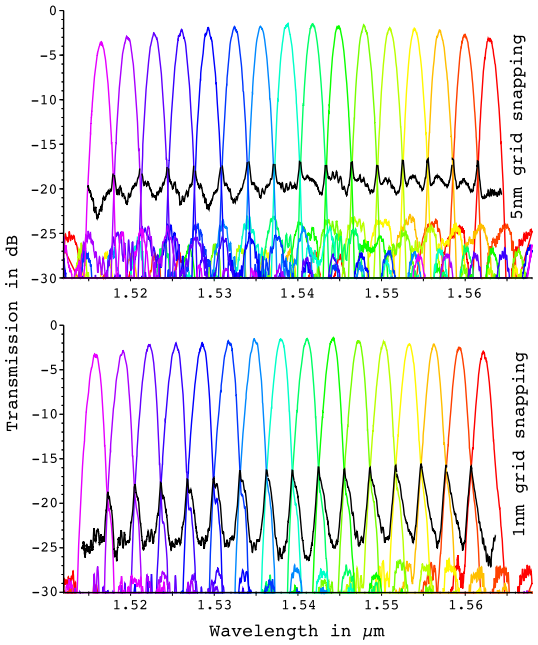

Fig. 7. Experimental transmission spectrum of 16×400 GHz AWG using 5 nm and 1 nm grid snapping. Black line indicates the cumulative power of the device.

complex when the channel spacing is fixed and the number of output channels is increasing: the delay length will be shorter but the number of waveguides needs to increase, which will increase the size of the AWG. Therefore depending on the number of waveguides used in the array the improvement of the crosstalk varies with the number of output channels. Ideally the insertion loss of an AWG should be independent of the grid discretization but in Table I we can see some variation in the insertion loss. This can be explained by the normalization with sightly different fabricated grating couplers or thickness and width variation of the waveguides over the wafer, which also leads to a wavelength shift of the full spectrum as we can see from Figs. 6 and 7.

VI. CONCLUSION

We demonstrate a significant improvement in silicon AWGs by going from a 5 nm mask discretization to a 1 nm mask grid. We see an experimental improvement of 2.7 to 6 dB in crosstalk and 1.2 to 5.0 dB in cumulative crosstalk due to snapping-related phase errors depending the channel spacing and number of output channel. In future AWG designs, it is possible to minimize the impact of the grid snapping by either optimizing the layout of the entire AWG, or by slightly repositioning the horizontal and vertical sections of the individual delay lines.

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