Building a sustainable future for silicon photonics

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Silicon photonics presents immense opportunity for innovation in telecom, datacom and sensing. But how do we build the food chain from research to high volume manufacturing? How do we address the issues associated with design tools, industrial fab capability, test and packaging capability?

Since about 2000 research in the field of silicon photonics has geared up at a rapid pace resulting in a stunning series of achievements reported by academic and industrial organizations worldwide. Furthermore the first commercial products are on the market. The reasons for the immense interest that this field has aroused and for the rapid progress are simple. For the first time a photonic integration technology could fall back on an immense technology and knowledge base with stable and high-yield processing and with patterning capability with nanometer-level accuracy. This came at a time where computing systems started to need a new interconnect technology with high throughput, high areal density at chip entry and low energy per bit. This need led to substantial resources for research both in a public funding and a private investment context. Another factor helped to advance the field. The nanoelectronics community is aware that CMOS scaling will stop at some point and is actively exploring new avenues that build on the same technology base. Silicon photonics is perfectly "phase matched" with this "More than Moore" evolution.

Where will the field be in another ten years from now? The dream of many is that silicon photonics will develop into a generic technology that can address many different markets and will be based on stable technology platforms, preferably in an industrial foundry-like approach. This would allow fabless companies to develop innovative products and evolve seamlessly from prototyping to small-volume manufacturing and possibly all the way to high volume manufacturing. The roadmap towards such a model is long and only some first steps have been taken.

On the positive side it is noteworthy that several companies and institutes are developing stable technology platforms for silicon photonics. Moreover several initiatives have emerged in recent years for the organization of shared multi-project-wafer shuttles for silicon photonics on state-of-the-art CMOS-lines. This MPW-approach lowers the entry barriers dramatically both for academic research groups and for fabless companies. It is also interesting to see that silicon photonics is no longer considered exclusively as a technology for transceivers but also as an important technology for sensing markets and for biomedical markets. Actually the products for these latter markets may be simpler and their introduction may be easier than is the case for transceivers.

In spite of all the promise there remain a number of important issues and challenges – open questions even - on the road to widespread application. Three such challenges are discussed hereafter.

1. Standardization and compatibility with CMOS process technology

New process development in a CMOS-fab environment is very expensive, but once a process is developed the "rewards" in terms of cost per chip are enormous. This is not only the case when the manufacturing volume is large but also for modest volumes, at least if the fab does not depend exclusively on those modest volumes. All of this suggests that it is imperative to develop a generic and standardized silicon photonics technology that is as much as possible compatible with CMOS process technology and that allows for a broad variety of applications. The risk is that technology development for performance optimization in one application may lead to poor performance in another application or in worst case rule out the other application altogether. The choice of the silicon layer thickness in SOI-wafers is one example of this. Ideally the whole silicon photonics industry and research community works with one type of SOI-wafer and with processes optimized for this wafer. But that may not serve all markets equally well. One should hope that some sort of basic generic silicon photonics technology is becoming the de-facto standard and that minor variations to that standard can serve many markets.

2. Back-end processing and packaging

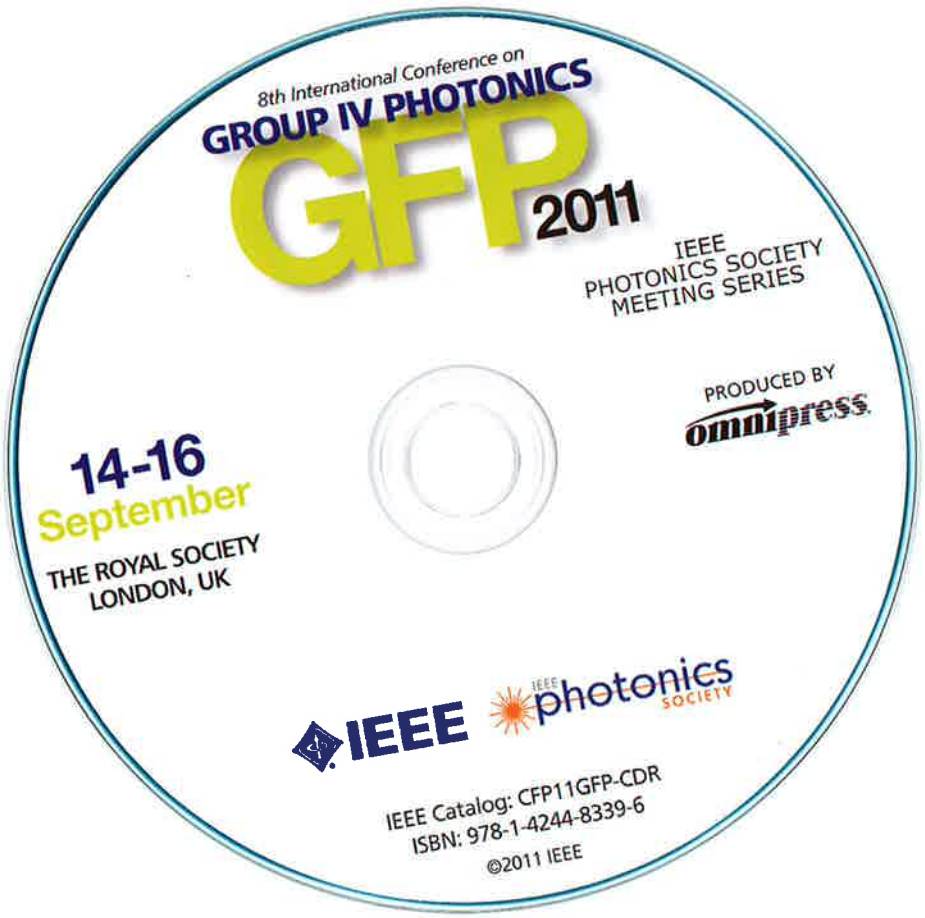
There is no point in having a technology capable of manufacturing complex chips at low cost if the subsequent back-end or packaging technology is very expensive. The field of silicon photonics requires some unconventional back-end processing and packaging. In terms of back-end processing one often uses overlay materials such as III-V semiconductors or organic materials to add functionality to the photonic components. Some of these back-end processing steps cannot easily be done in a 200 or 300 mm fab or they bring in materials that are undesired in a CMOS-fab. This means that there is a need for dedicated fabs to do this processing and possibly also of specific new tools.

A similar situation exists with respect to packaging and in particular with respect to the attachment of single or multiple optical fibers. Given the requirements with respect to alignment existing packaging methods are mostly expensive. It will take new creative approaches to address these challenges and to develop tools for it.

In a number of applications a pure silicon photonics solution may not be the best approach for a photonic system and one may want to combine silicon photonics chips with III-V chips, with silica chips or with organic chips. This "mix-and-match" approach will only be viable if suitable photonic multi-chip packaging approaches are developed that allow for cost-effective microsystem integration.

3. Design tools

A third challenge is presented by the design methodologies for silicon photonics. Photonic integrated circuits can have a high degree of complexity at various levels and this calls for a hierarchical approach involving physical device modeling, technological process modeling, circuit simulation and design, layout generation, design rule checking etc. When the functionality is not only optical but also electrical, often with high bandwidth signals, the resulting design problem is very tough. In many cases one also needs to take into account thermal design problems. Considering the relatively high cost of fabrication as well as its duration, the economic value of first-time-right design is very large. In spite of efforts in recent years, the landscape of design tools for silicon photonics remains rather scattered and incomplete today. There is a clear need for advanced tools that can link three-dimensional geometry data to detailed device models as well as to circuit models and that can accurately predict overall system performance including the sensitivity to changes in the "details". Also, data exchange between design tools from different vendors should be made possible. This is not purely a software development problem. There are also more fundamental questions with respect to the underlying methodology.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