Post-bonding fabrication of photonic devices in an Indium phosphide membrane bonded on glass

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We demonstrate the successful fabrication of passive photonic devices in a 300-nm thick Indium phosphide (InP) membrane bonded on glass, using a post-bonding fabrication scheme. Our results show that post-bonding processing can be used to allow double-side processing of InP membrane devices. Furthermore, the yield in InP membrane fabrication can be increased by bonding the membrane prior to patterning. Characterization results show good performance in power splitters and ring resonators (Q ~ 15,000). However, waveguide losses were found to be very high (25 dB/cm) and need to be reduced by e.g. optimizing the lithography steps.

Introduction

The integration of small photonic circuits on top of different substrates is very interesting for a number of applications. High on the list, on-chip photonic interconnect networks have been proposed to improve the speed, density and energy consumption of computer chips, by replacing some of the metallic wires they contain with photonic waveguides [1]. Conversely, highly integrated optical sensors could be fabricated by combining on a single substrate the photonic sensing devices and the electronic circuit driving them. The most promising way to realize all these applications is to develop reliable and scalable photonic membrane technologies.

Recently, we have shown that one of these technologies, IMOS (Indium phosphide Membrane on Silicon), promises the integration of ultra-small active and passive photonic devices in a single layer [2]. The devices realized previously in this platform were processed before bonding. This process scheme was well suited for passive devices requiring only single-sided processing. However, for more complicated devices it may be useful, if not necessary, to apply processing steps both before and after bonding.

Finally, the BCB bonding process was found to be more reliable (both in terms of uniformity and success rate) for un-patterned dies/wafers than for patterned ones. Therefore, even for single-sided processing, the technology could be made more reliable by bonding the un-patterned membrane right after the growth, and printing the devices after bonding and substrate removal. In this paper, we report the successful fabrication of photonic devices in the IMOS platform (with glass as the holder substrate) using post-bonding processing.

In the following sections of this paper, a detailed description of the post-bonding fabrication scheme recently developed for IMOS will be given, followed by the presentation of some measurements carried out on real devices fabricated according to this scheme.

Fabrication Scheme

The first step in the fabrication consists in the epitaxial growth of the future membrane. A 300-nm thick etch-stop InGaAs layer is grown on top of an InP substrate, followed by the 300-nm thick InP membrane layer (cf. diagram on the left in Fig. 1). The InGaAs etch-stop layer will be used in a subsequent step to protect the InP membrane layer during the InP substrate removal.

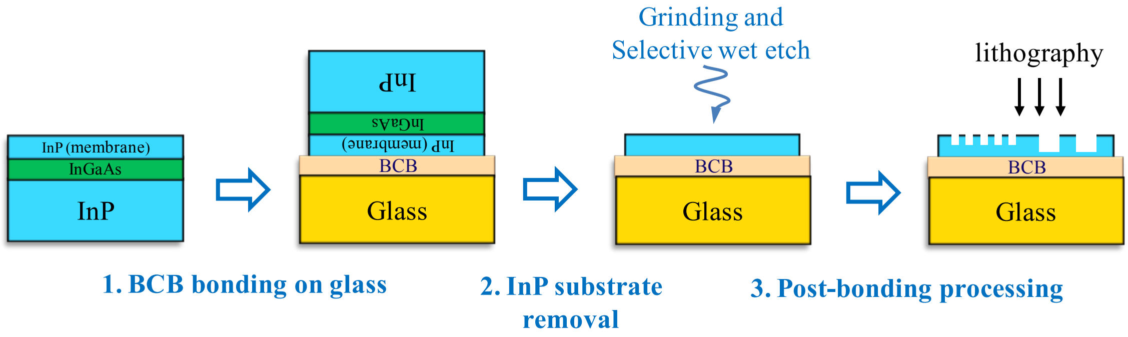

Fig. 1 IMOS post-bonding fabrication scheme (not to scale)

After the growth, the InP wafer (or a die from it) is bonded upside-down on glass. A diluted BCB solution (in mesitylene) is spin-coated on the glass carrier wafer. The liquid BCB solution can planarize the wafer topography and sufficiently small particles can be incorporated in the adhesive film. After spin-coating, the BCB is baked at 150°C to evaporate the solvent and settle the applied film. Finally, the InP wafer is attached on the glass carrier wafer and the whole stack is placed in an oven where the BCB is cured in a nitrogen atmosphere at 250 °C for 1h. Usually, a pressure of 200-300 kPa is applied during the curing.

In order to create the high vertical index-contrast of the membrane, the InP substrate is then removed from the bonded sample by grinding and wet etching (see step 2 in Fig. 1). Grinding being a fast but coarse process, it is used to thin down the InP wafer from 300 µm to about 50 µm. The sample is then successively put for around 1.5h in a wet etching solution of 4 H_3PO_4: 1 HCl (which etches InP selectively to InGaAs), and for 30 seconds in a solution of 10 H_2O: 1H_2SO_4: 1H_2O_2 (which etches InGaAs selectively to InP). In this way, a bonded InP membrane is left which is very smooth, clean and has the exact thickness produced in the epitaxial growth.

Once the membrane has been created, it is patterned using a combination of high-resolution e-beam lithography and optical lithography. A 50-nm layer of Si_3N_4 is first deposited on the membrane by plasma-enhanced chemical vapour deposition (PECVD). A positive e-beam resist, ZEP-520, is then spun on the sample and exposed to define the photonic circuit pattern. After development, the sample is baked for 2 minutes at 155 °C to reduce the roughness in the developed ZEP-520 features, and the pattern is subsequently transferred to the Si_3N_4 layer using a CHF_3-based reactive ion etching (RIE) process.

In the pattern thus defined, some parts need to be etched “deep” in the InP membrane (the trenches of the waveguides and other devices), while others need to be etched “shallow” (the grooves of the gratings used to couple light into and out of the membrane

[3]). In order to achieve this, another lithography step is necessary. However, since the resolution needed here is not very high, we use optical lithography instead of e-beam lithography. A positive optical resist, AZ-4533, is deposited on the sample and exposed using an optical mask to open the area with the waveguides and other devices while keeping the area of the gratings covered. After a hard-bake of the patterned AZ-4533 at 200 °C for 20 minutes, the InP membrane is etched using an inductively coupled plasma (ICP) CH_4-H_2 process, at 60 °C. Once an etching depth of 160 nm has been reached, the AZ-4533 mask pattern is removed in a high-power O_2 plasma stripper. The ICP etching is then resumed with the same recipe until depths of 120 nm and 280 nm have been etched in the grating grooves and in the waveguide trenches, respectively.

Finally, the Si_3N_4 mask is removed using buffered HF, and the sample is ready for characterization.

Measurement Results

In order to test the post-bonding processing scheme presented in this paper, simple passive devices were fabricated (see Fig. 2). These include straight waveguides, 1×2 multi-mode interference (MMI) power splitters and ring/racetrack resonators for estimating the propagation losses.

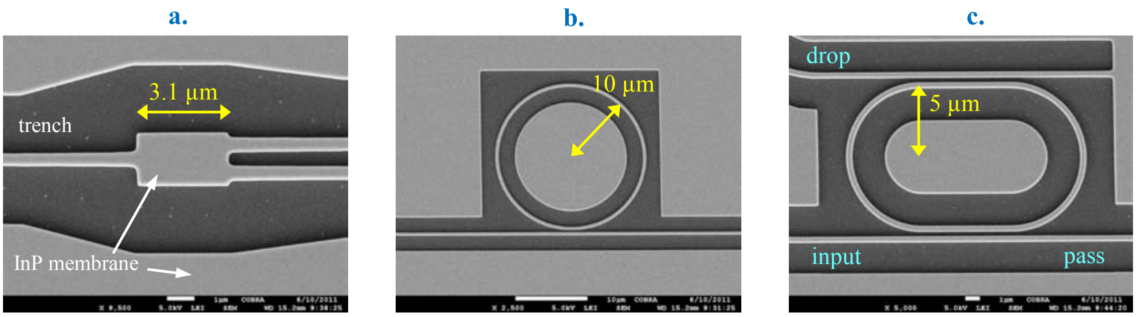

Fig. 2 An MMI power splitter (a.), a ring resonator (b.) and a racetrack (c.) fabricated using IMOS post-bonding processing

The MMI splitters showed very good performance. For the best splitters, each arm was found to transmit exactly half of the power transmitted by straight waveguides of the same length as the full device. The excess losses of the MMI splitters are thus shown to be below the standard deviation of the transmission measurements (~1 dB), a value compatible with previous results obtained by pre-bonding processing [2].

Ring resonators and racetracks are another family of device with very simple layouts, yet numerous applications (ranging from sensing to wavelength division multiplexing). In our chip, we use them to assess the quality of the waveguides (through the value of the propagation losses). Ref. [4] offers a clear description of a ring resonator model that can be used to fit the measured transmission (or $|S_{21}|^2$ coefficient, when normalized), and extract useful parameters from it, such as the propagation losses in the ring and the coupling coefficient between the ring and the straight waveguide.

In Fig. 3a, the measured transmission of a 10-µm ring is shown, together with the fitted curve obtained with the ring model of [4]. The propagation losses in this ring were found to be 23.2 dB/cm, and the coupling coefficient 2.5×10^{-3}. The quality factor of this ring resonance is around 14,800. The transmission through the pass and drop ports of a racetrack are shown in Fig. 3b. For this device, the quality factor is around 3,100 and the suppression ratio in the pass port is more than 16 dB.

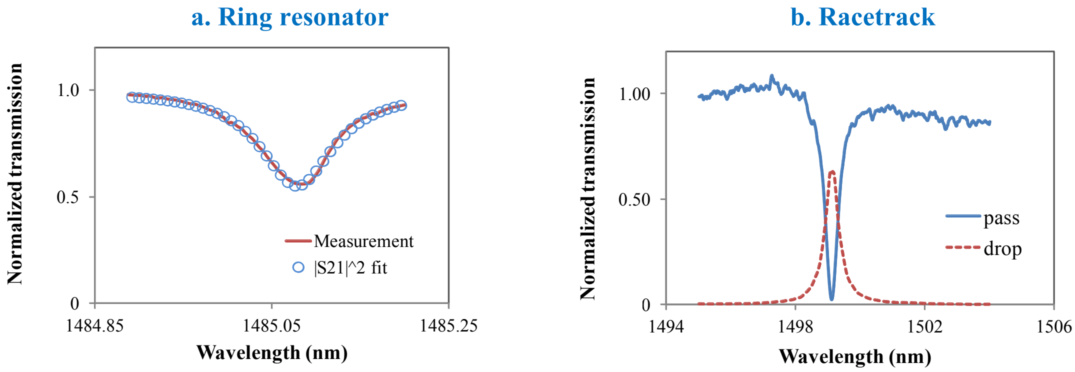

Fig. 3 Measured transmission of the ring resonator (a.) and racetrack (b.) pictured in Fig. 2

The rather high value found for the propagation losses in the ring may be explained by residual roughness in the waveguide sidewalls. Furthermore, growth defects have been observed in the InP membrane, which can certainly cause extra scattering of light. Currently, we are working on optimizing the fabrication process to further reduce the sidewall roughness, by using a combination of O_2 plasma oxidation and diluted H_3PO_4 wet etching.

Conclusion

In this paper, we present the first demonstration of successfully integrated IMOS passive devices processed after bonding. These passive devices show reasonably good performances (MMI splitters with excess losses below 1dB, ring resonators with Q-factors of nearly 15,000), which can be further improved. Besides, These results are comparable (or better) than those of devices made with pre-bonding processing [2], indicating that post-processing is a very promising approach for passive IMOS devices fabrication. Finally, it is interesting to note that this work represents an important step towards the future double-sided processing of active devices in IMOS.

References

[1] D.A.B. Miller, “Optical interconnects to electronic chips,” Applied Optics, vol. 49, issue 25, pp. F59-F70, 2010.

[2] J.J.G.M. van der Tol *et al.*, “Photonic integration in indium-phosphide membranes on silicon,” IET Optoelectronics, vol. 5, issue 5, pp.218-225, 2011.

[3] G. Roelkens *et al.*, “Bridging the Gap Between Nanophotonic Waveguide Circuits and Single Mode Optical Fibers Using Diffractive Grating Structures,” Journal of Nanoscience and Nanotechnology, vol. 10, pp.1551-1562, 2010

[4] A. Vörckel *et al.*, “Asymmetrically Coupled Silicon-On-Insulator Microring Resonators for Compact Add–Drop Multiplexers,” IEEE Photonics Technology Letters, vol. 15, no. 7, 2003