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Loss reduction in silicon nanophotonic waveguide micro-bends through etch profile improvement

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ABSTRACT

Single mode silicon photonic wire waveguides allow low-loss sharp micro-bends, which enables compact photonic devices and circuits. The circuit compactness is achieved at the cost of loss induced by micro-bends, which can seriously affect the device performance. The bend loss strongly depends on the bend radius, polarization, waveguide dimension and profile. In this paper, we present the effect of waveguide profile on the bend loss. We present waveguide profile improvement with optimized etch chemistry and the role of etch chemistry in adapting the etch profile of silicon is investigated. We experimentally demonstrate that by making the waveguide sidewalls vertical, the bend loss can be reduced up to 25% without affecting the propagation loss of the photonic wires. The bend loss of a 2 μm bend has been reduced from 0.039dB/90° bend to 0.028dB/90° bend by changing the sidewall angle from 81° to 90°, respectively. The propagation loss of 2.7 ± 0.1dB/cm and 3 ± 0.09dB/cm was observed for sloped and vertical photonic wires respectively was obtained.

1. Introduction

Scaling down of devices and circuits is the key for advancement in technology and functionality; microelectronics is an excellent example. In microelectronics, scaling is mainly driven by fabrication technology, in contrast, material technology dictated the size of the devices in integrated photonics. For example, the size of a device can be reduced by six orders of magnitude by increasing the refractive index contrast ($\Delta = (n_{core}^2 - n_{clad}^2)/2n_{core}^2$) from 0.007 to 0.412. High index contrast material technology, in particular, silicon-on-insulator (SOI) enables sub-micron waveguide cross-section and micrometer scale waveguide bends. The micro-bends forms an essential component in compact circuits and device design [1]. In addition, manufacturing photonic circuits with the existing microelectronics fabrication technology is an added advantage in making silicon (Si) photonics competitive in the market. Using such fabrication process, various active and passive photonics devices have been demonstrated. In particular, exploiting micro-bends are arrayed waveguide gratings (AWG), Mach–Zehnder interferometers, and ring resonators for various applications [2,3].

Recently, there has been considerable interest to estimate losses in the micro-bends using numerical and analytical methods [4,5]. Various loss mechanisms, such as transition loss and polarization conversion loss were numerically calculated assuming a symmetrical waveguide geometry. However, in practice the fabricated waveguides are asymmetric (or with sloped sidewalls). Modelling such an asymmetric waveguides is not straightforward, this requires a fine grid definition in the computation window, which often results in a computationally challenging task. Despite this challenge, Sakai et al. have found that the waveguide sidewall angle is crucial for low loss micro-bends [5]. Deviation from perfectly vertical sidewalls results in polarization cross talks between TE and TM like modes in the micro-bends. This loss gives rise to undesirable bend loss for polarization sensitive waveguide circuit and for general power budget in a photonic circuit.

In this paper, we investigate the etch profile improvement of Si photonic wires and its effect on the bend loss in the micro-bends. The waveguide profile is tuned by varying the etch chemistry of the dry etch process. We demonstrate that by increasing the verticality of the photonic wire sidewalls the bend loss in the micro-bends can be reduced as much as 25%.

2. Experiment design

The etch experiments were carried out in a 200 mm pilot-line facility at IMEC, Belgium. To reduce the process development costs, 200 mm dummy SOI wafers were fabricated by depositing 220 nm of amorphous Si on top of 2000 nm high density plasma silicon dioxide instead of crystalline SOI wafers. After layer deposition, the circuit pattern is first transferred into the photoresist using 193 nm optical lithography and followed by dry etching [6]. During lithography, the wafers are coated with 77 nm of organic bottom anti-reflective coating layer (BARC) and 330 nm of photoresist. The wafer is then exposed and developed (Fig. 1). After optical lithography, the wafers

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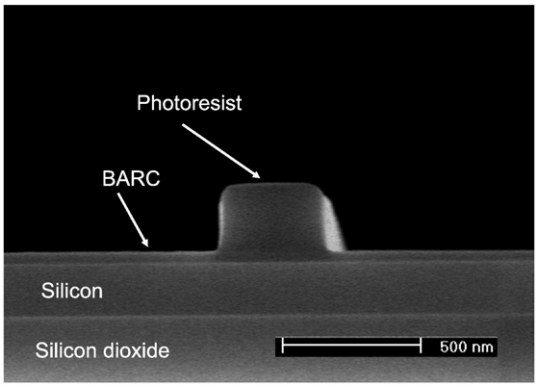


Fig. 1. Cross-section electron micrography layer stack after photolithography.

are dry etched using an inductively coupled plasma-reactive ion etching (ICP-RIE) process.

2.1. Etching system and sequence

The etch experiments were carried out in a 200 mm industrial tool, which consists of a high density inductively coupled plasma chamber and a load-lock. The source power was inductively coupled to the plasma through the quartz top plate in the chamber, while the wafer temperature was kept at 60 °C. The etch gases used in our study are Cl_2, HBr, CF_4 and SF_6. Table 1 summarizes the sequence of the etching processes inside the chamber and the gas mixtures. In addition to the etch steps, the chamber is cleaned after etching each wafer using a *F* based plasma to create a stable chamber condition for the subsequent etch process.

After chamber cleaning, the wafer is loaded into the chamber for etching. The BARC layer is opened first (step 1) to access the underlying Si, followed by photoresist hardening using HBr to improve etch selectivity between the photoresist andSi [7]. Before the actual Si etch, the native oxide is removed (step 3). The Si etch is carried out in 3 steps, firstly, a *F* containing plasma (step 4, main etch 1) is used to etch ≈44 nm of Si followed by a highly selective HBr/O_2 plasma (step 5, main etch 2) to etch the major part of Si. Finally, over etch (step 6, over etch) is applied to remove any footing in Si. After completing the Si etch, the remaining photoresist and the BARC layer are stripped in-situ using O_2/SF_6 plasma (step 7). The wafers are further cleaned, first, by using a dry plasma clean to remove any remaining polymers and then by wet chemical clean. The wet clean is performed using an ammonium peroxide mixture and a sulphuric acid peroxide mixture.

It is well known that the dry etching process can be anisotropic. In order to achieve anisotropic Si etching we use sidewall protection also referred to as sidewall passivation layer. It has been shown that the thickness of the passivation layer (PL) formed on the sidewalls of Si during etching determines the etch profile [8]. The constituents in the PL come from both the etch plasma and the etch by-products. By controlling the constituents, the thickness of the PL can be modified.

Table 1
Etch process sequence and gases.

Step no.	Process step	Etch gas	Gas ratio (%)
1	BARC Open	HBr/O_2	75/25
2	Photoresist hardening (PRH)	HBr	100
3	Oxide break through (BT)	CF_4/CH_2F_2	89/11
4	Main etch 1 (ME1)	$Cl_2/HBr/CF_4/O_2$	17/34/48/1
5	Main etch 2 (ME2)	HBr/O_2	100-97.5/0-2.5
6	Over etch (OE)	HBr/O_2/He	32/1/67
7	Resist strip	O_2/SF_6	95/5

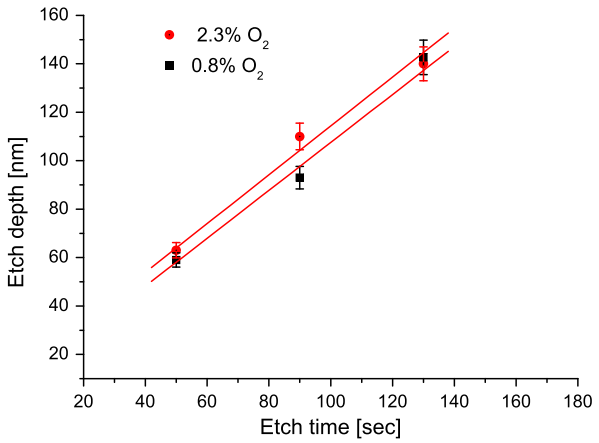


Fig. 2. Silicon etch rate with 0.8% and 2.3% of O_2 in main etch 2(ME2).

Since main etch 2(ME2) is the major contributor to the Si etch and the etch profile, we exploit the etch chemistry in ME2 to tune the etch profile. In our experiment, we study the effect of O_2 on the etch profile of Si by varying the percentage of O_2 in the feed gas between 0-2.5% in ME2, while other etch steps were kept unchanged.

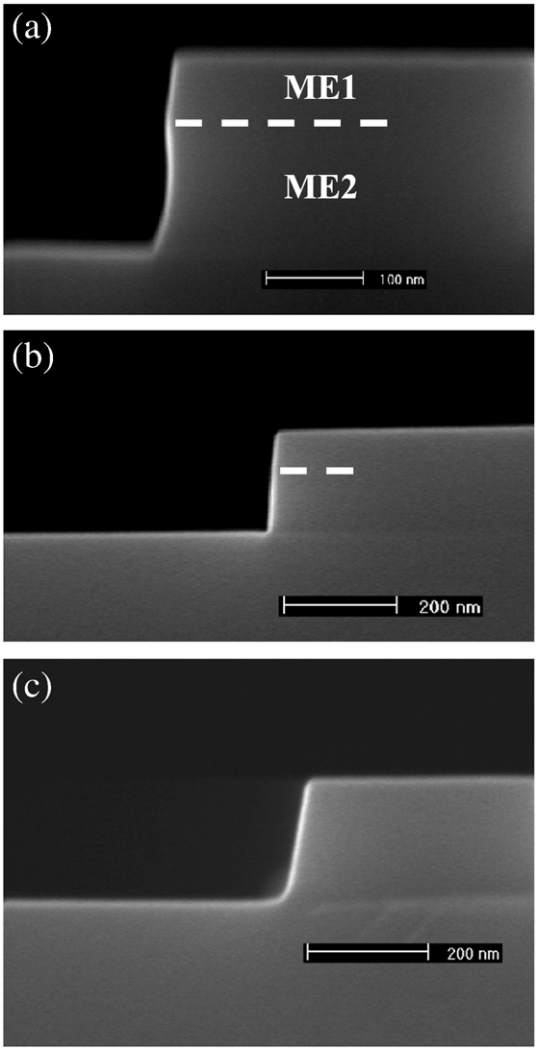


Fig. 3. Si etch profile as a function of O_2 concentration a) 0% , b) 0.8% and c) 2.3%. The dotted lines shows the pattern defined by ME1 and ME2.

2.2. Etch rate and profile analysis

The Si etch rate is deduced from the etch depth of a 2000 nm wide Si trench. A cross-section scanning electron microscope (XSEM) is used to measure the etch depth and profile for different chemistries. The image from XSEM is further processed using image processing algorithms in order to remove SEM-image artefacts and accurately extract the waveguide sidewall angles.

2.3. Photonic test structure

Single-mode photonic wire waveguides (450×220nm) were used as test structures to study the effect of waveguide profile on the propagation loss and bend loss. In order to extract these two losses effectively, photonic wires with various lengths (5–50 mm) were spiralled with different bending radius (2, 3, and 5 μm) and number of bends (50–550) [6]. Grating couplers were used to couple TE polarized light from a single mode optical fiber into the waveguides. The single mode waveguides were adiabatically tapered to a broad waveguide of 10 μm in order to increase the coupling efficiency to a single mode optical fiber [9]. Apart from efficient light coupling, the grating couplers are highly polarization sensitive any polarization conversion in the micro-bends can be measured as transmission loss from the waveguides.

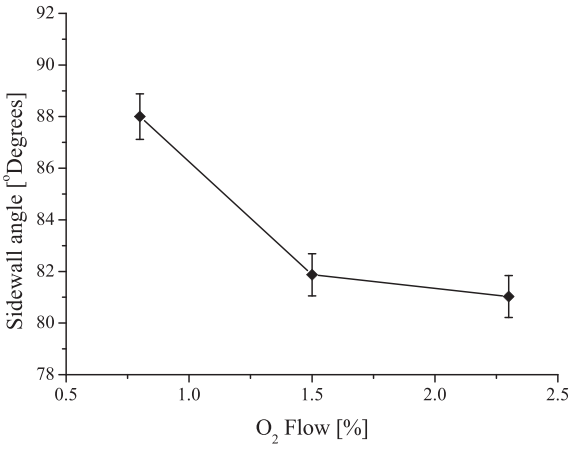


Fig. 5. Sidewall angle as a function of O_2 concentration in HBr/O_2.

3. Results and discussions

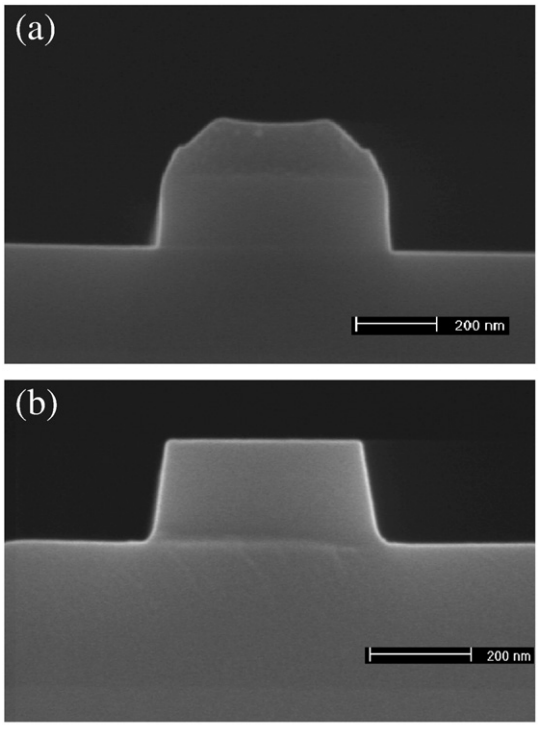
3.1. Si etch rate

We observe a slight increase in the Si etch rate with an increase in O_2 concentration (Fig. 2). An etch rate of ≈60 nm/min and ≈72 nm/min was obtained for 0.8 and 2.3% respectively of O_2 the in ME2 feed gas. The increase in the etch rate can be attributed to unsaturation of polymeric volatile etch byproducts by *O* atoms. This unsaturation results in release of reactive Br atoms from etch byproducts, which increases the etch rate. However, at a higher concentration, O atom chemisorbs on to the Si surface and reduces the etch rate. Thus by using an optimum amount of O_2 the Si etch rate can be kept high enough for good wafer throughput.

3.2. Sidewall angle analysis

Following etching 220 nm of Si with different concentrations of O_2 in HBr/O_2, the waveguide profile was characterized using a XSEM. Fig. 3 shows the sidewall profile of a photonic wire etched with three different concentrations of O_2. As mentioned before ME1 was kept constant for all the three cases. This allows us to confirm that the profile change is due to ME2 and not due to other effects, such as photoresist erosion.

When exposed to a pure HBr plasma, we observe isotropic Si etching (Fig. 3a) due to the absence of PL on the sidewalls, which exposes Si to aggressive Br radicals. Anisotropy can be achieved by



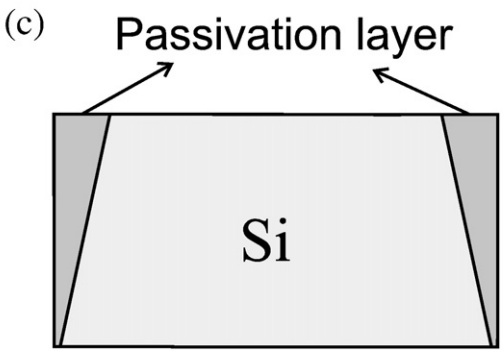


Fig. 4. Silicon etch profile a) before, b) after resist strip and clean and c) schematic of passivation layer thickness on the sidewalls.

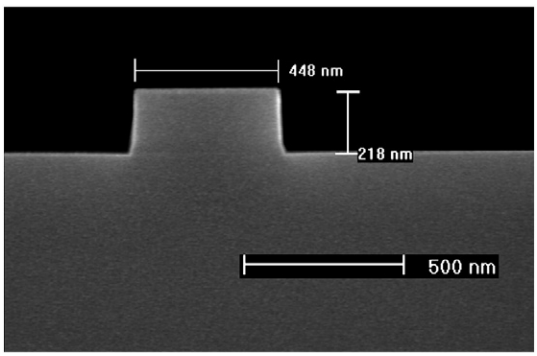


Fig. 6. Silicon photonic wire with vertical profile etched with optimal (0.75%) O_2 concentration.

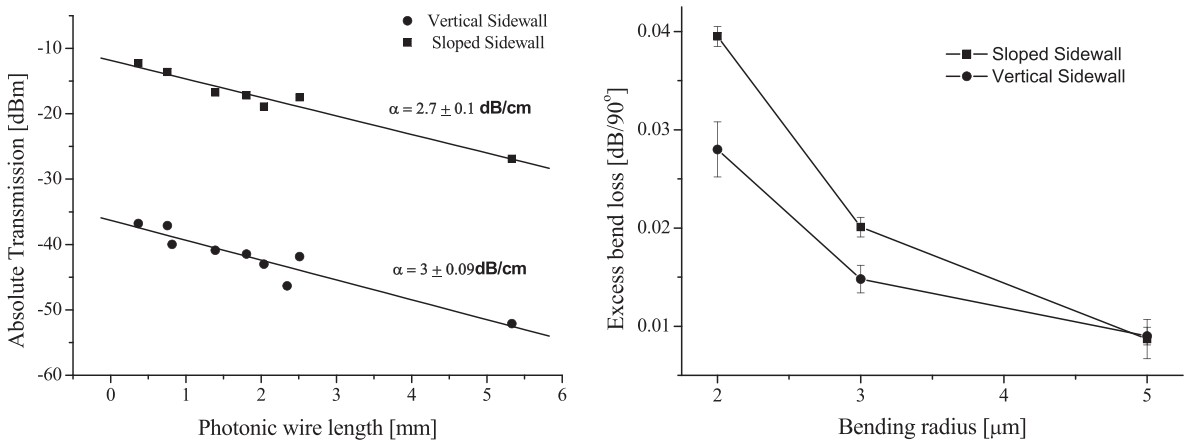


Fig. 7. (Left) Propagation loss of a photonic wire with sloped (81°) and vertical (90°) sidewall profile and (right) comparison of bend loss of sloped (81°) and vertical (90°) photonic wire.

protecting the sidewalls with a PL containing Si/O/Br/C, which is chemically resistant to Br radicals. In particular, SiO_xBr_y like compounds are good sidewall inhibitors to achieve anisotropic Si etching [8]. The thickness of the PL depends on the amount of Si, O, Br and C in it. By increasing the concentration of any of the constituents, the thickness can be increased. In our case, when a small amount of O_2 is added in the feed gas, the etch process is made anisotropic (Fig. 3b and c) as a result of sufficient PL deposition on the sidewalls.

Even though a PL facilitates anisotropic etching, it modifies the etch profile. The top of the wire is exposed longer than the bottom resulting in a thicker PL at the top than at the bottom (Fig. 4c). Fig. 4a shows a photonic wire before photoresist removal and cleaning, where a vertical sidewall can be clearly observed. However, after cleaning the photoresist and the PL layer the actual etch profile is revealed (Fig. 4b). This clearly shows the gradient in the PL thickness along the height of a photonic wire sidewall. By controlling the PL thickness the sidewall angle can be tuned (Fig. 5). Fig. 6 shows a photonic wire fabricated with the optimum O_2 concentration (0.75%) in ME2 and reducing ME1 etch duration.

3.3. Photonic wire propagation and bend loss

The photonic wire and micro-bends were optically characterized by coupling TE polarized light in and out of the waveguides using identical grating fiber couplers. The light from a broad band light source (superluminescent-LED) or a tunable laser is launched into the waveguides through polarization controlling wheels. The output is measured using an optical spectrum analyzer or a power-meter. The transmitted power is measured and projected against photonic wire length and number of micro-bends in a three dimensional space. By fitting a plane, we could extract the propagation loss and bend loss at the same time.

From the propagation loss characterization, we observed a propagation loss of 3 ± 0.1dB/cm and 2.7 ± 0.09dB/cm for vertical (90°) and sloped (81°) sidewall wires respectively (Fig. 7). The difference of 0.3*dB/cm* in propagation loss can be attributed to slight increase in the sidewall roughness due to thinner PL thickness on the photonic wire with vertical sidewalls.

We do observe a decrease in micro-bend loss of photonic wires with vertical sidewalls. Fig. 7 shows the bend loss of micro-bends with different bend radius and sidewall angle. There is a clear indication that the bend loss of a vertical sidewall bend decreases by $\approx 25\%$ from a sloped sidewall bend. The bend loss shows a typical loss trend when the bend radius is decreased as a consequence of an increase in perturbation. We observe bend loss as low as 0.015 and 0.028 dB/90° bend for bend radius of 3 and 2 μm respectively for vertical photonic wire bends, while for sloped wires the bend loss stood at 0.029 and 0.039 dB/90° bend for 3 and 2 μm bend radius respectively. The improvement in the bend loss of narrow bends can be attributed mainly to a reduction in the polarization conversion loss in the bends due to the symmetric waveguide profile. However, no significant change was observed for large bends (5 μm), where the perturbation is less significant. The results obtained from our experiments agree well with the trend obtained from 3-D FDTD simulations by Sakai et al. [5]. Since the sidewall roughness of both waveguide profiles are similar, the micro-bend loss reduction can be clearly attributed to photonic wire sidewall angle. The tradeoff between the micro-bend loss and propagation loss of the vertical sidewall photonic wires can be compensated by using post-fabrication treatements [10]. Various processes, such as wet chemical etching and oxidation has been proposed to reduce the sidewall roughness generated during the patterning process [11].

4. Conclusions

We have shown that by modifying the dry etch chemistry the sidewall angle of a silicon photonic wire can be tuned. The contribution of O_2 to the sidewall passivation layer thickness and controlling the sidewall angle has been studied. The bend loss, which includes polarization conversion and transition losses is reduced from $0.039 \pm$ dB/90° bend to 0.028dB/90° bend by changing the sidewall angle from 81° to 90° respectively. For <5 μm bends the bend loss reduces as much as 25%, while for >5 μm bends the improvement was very minimal. The change in the propagation loss of a sloped (2.7dB/cm) and vertical (3dB/cm) sidewall photonics wires was keptas low as at + 0.3dB/cm.

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