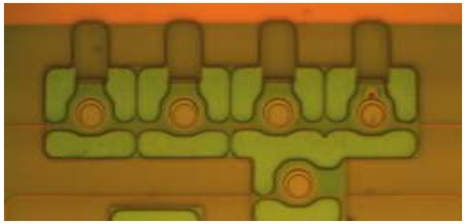
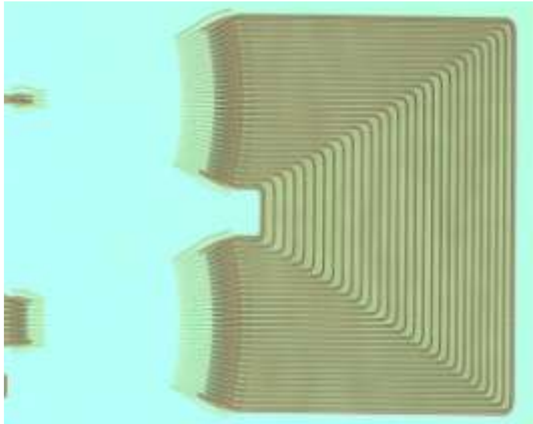
Silicon Photonics

Dries Van Thourhout

ACP 2010 - Tutorial



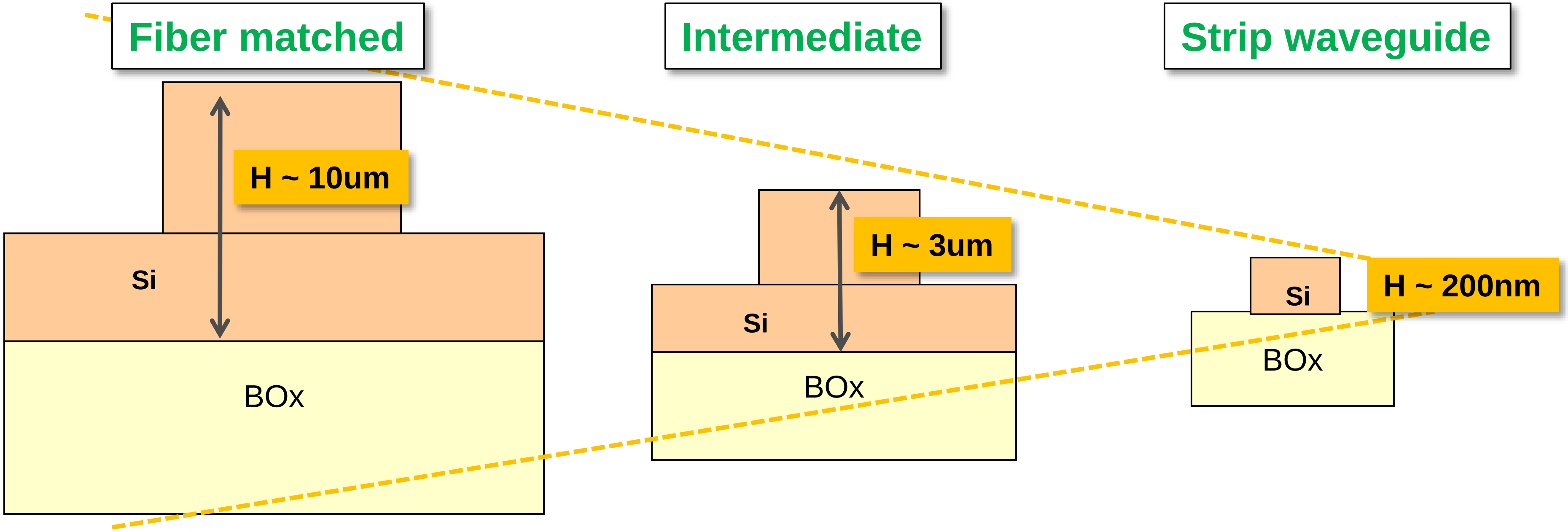


Presentation will be available from http://photonics.intec.ugent.be/download

Silicon Photonics

Dries Van Thourhout

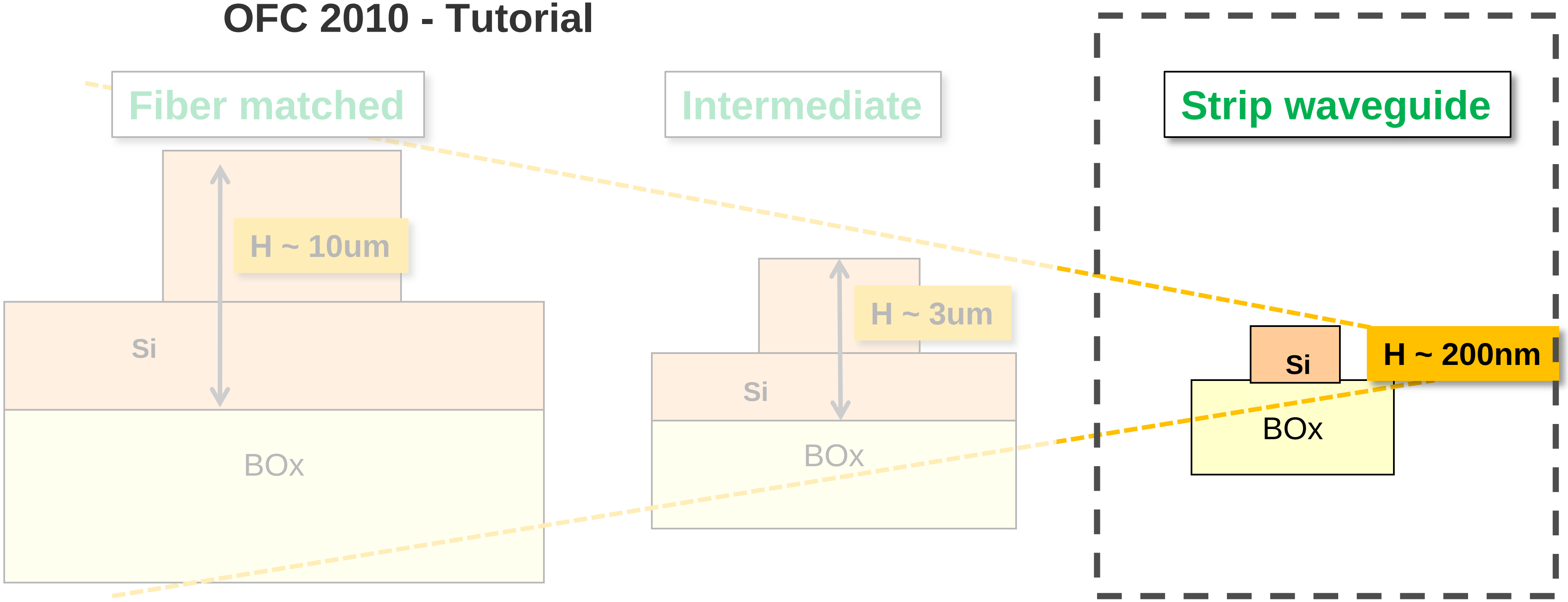
OFC 2010 - Tutorial



Silicon Photonics

Dries Van Thourhout

OFC 2010 - Tutorial



Disclaimer

This is a tutorial

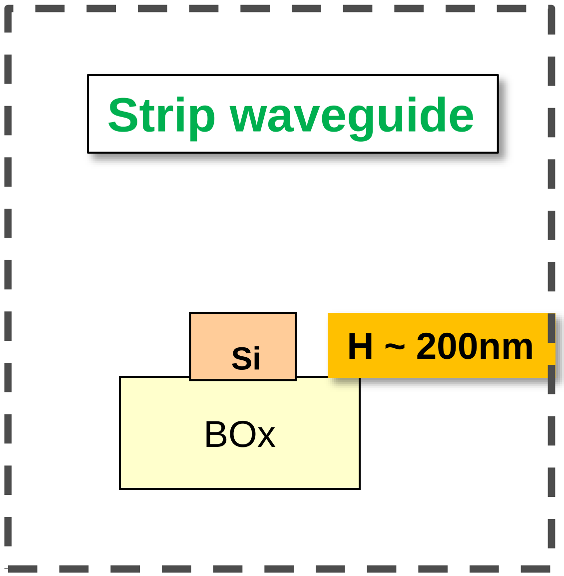
- Experts in the field are welcome but not intended public ☺
- Not covering advanced topics
  - Photonic crystals
  - Plasmonics
  - …

Material available:

- References in green: available from www.photonics.intec.ugent.be
- References in blue: available from literature
- Complete presentation: will be available from http://photonics.intec.ugent.be/download

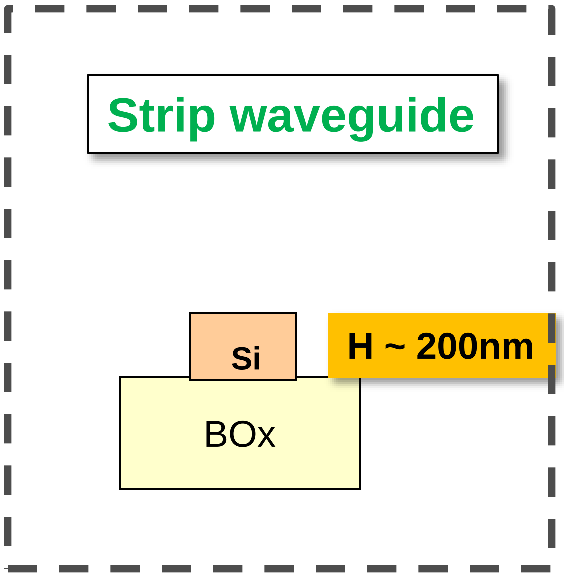
Bogaerts e.a. , JSTQE 16, 33-44 (2010)

Gnan e.a., Electronic Lett. 44, p115 (2008)



Why Silicon ?

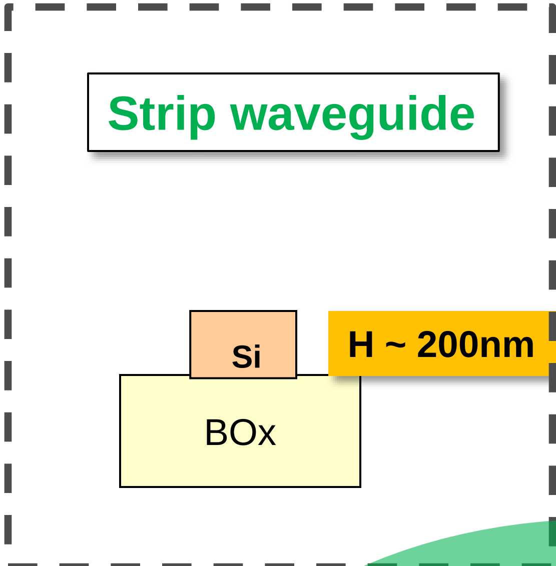
- Silicon is transparent in telecom range
- Processing using very large existing equipment base !!!
- High index contrast → compact circuits
  - But others also have sufficient contrast (e.g. SiN, HfO …)
- Active functionality possible
  - High thermo-optic effect
  - Carrier plasma effect
  - Integration with Germanium, III-V …

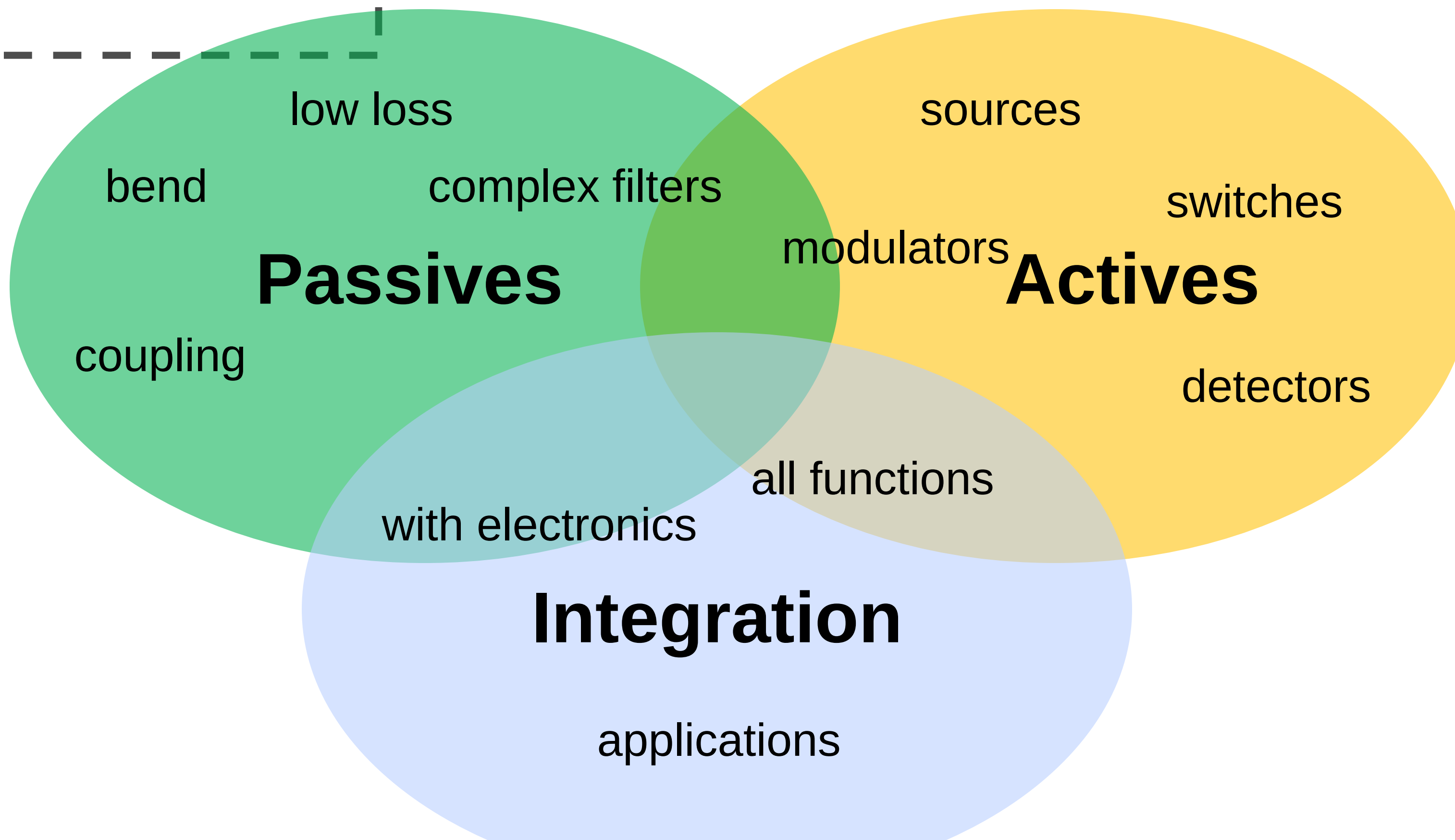


Why strip waveguide ?

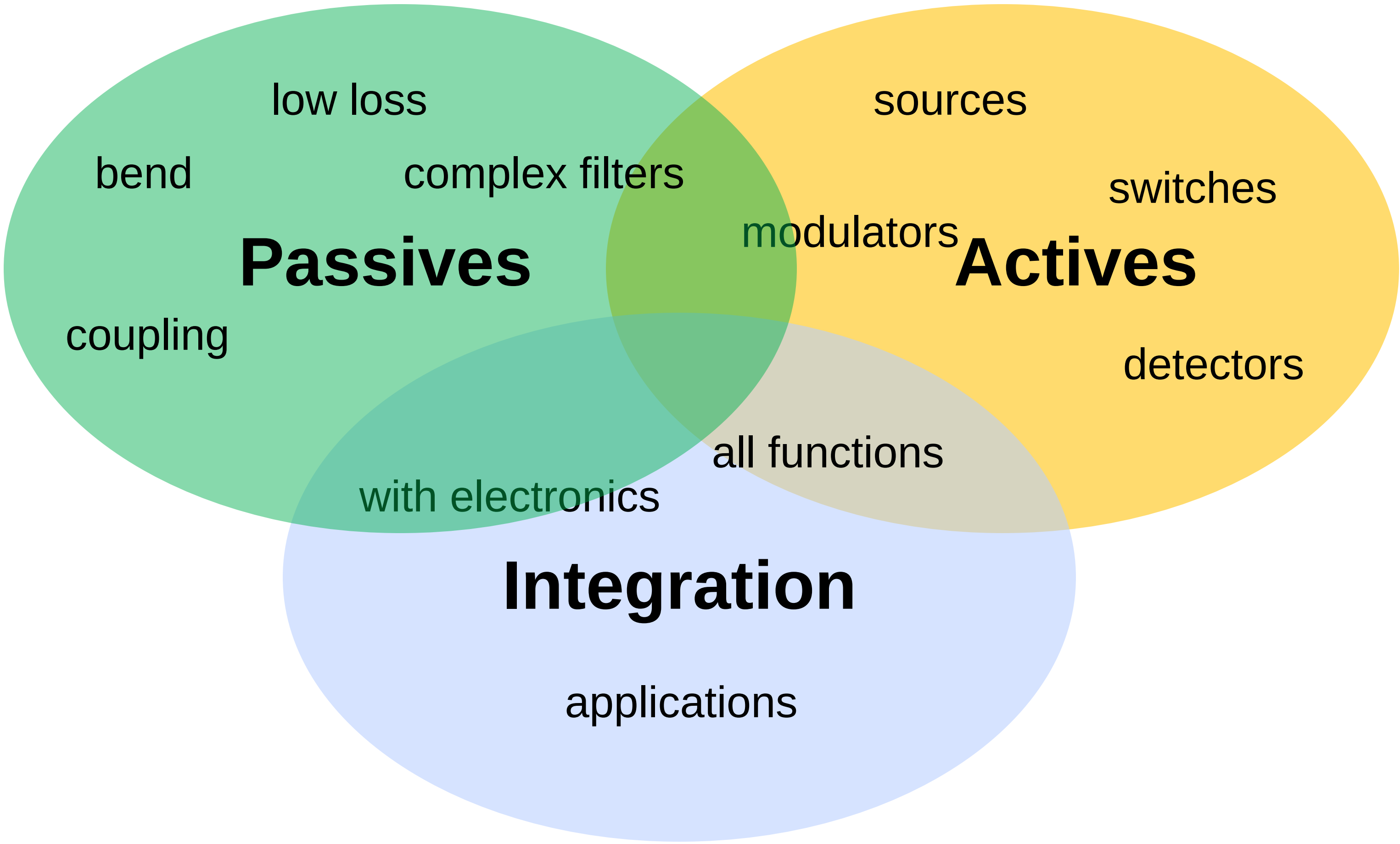
- **Very compact circuits**
- **Processing more compatible with electronics processing**
- **Active functionality enhanced**
  - **Increased light-material interaction**
  - **Faster devices**
  - **Lower power consumption**
  - **Higher non-linear effects**

What do we need?

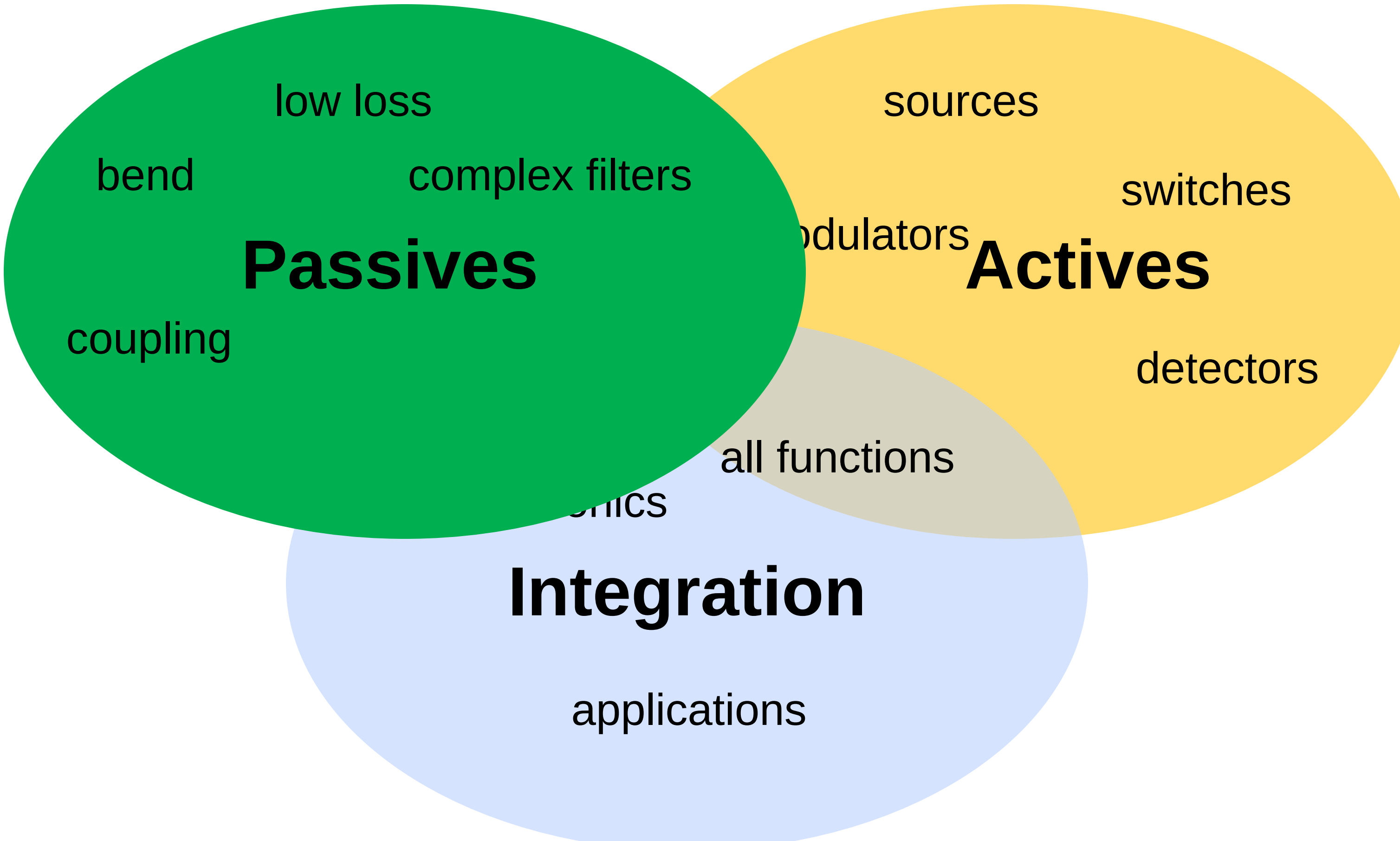




Outline


low loss
sources
bend
complex filters
switches
modulators
Passives
Actives
coupling
detectors
all functions
with electronics
Integration
applications

Outline

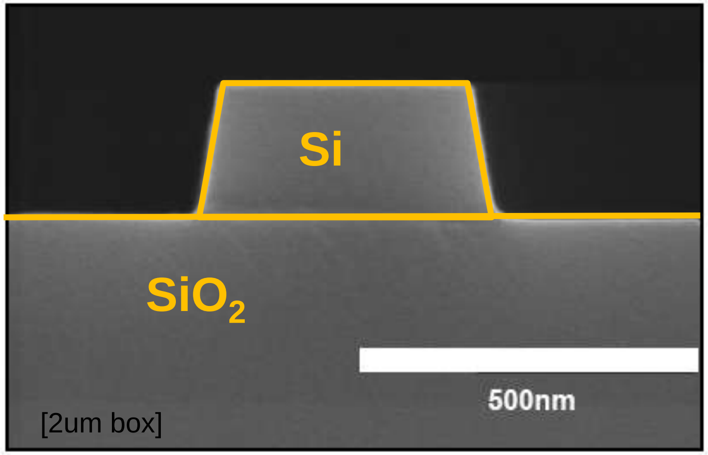


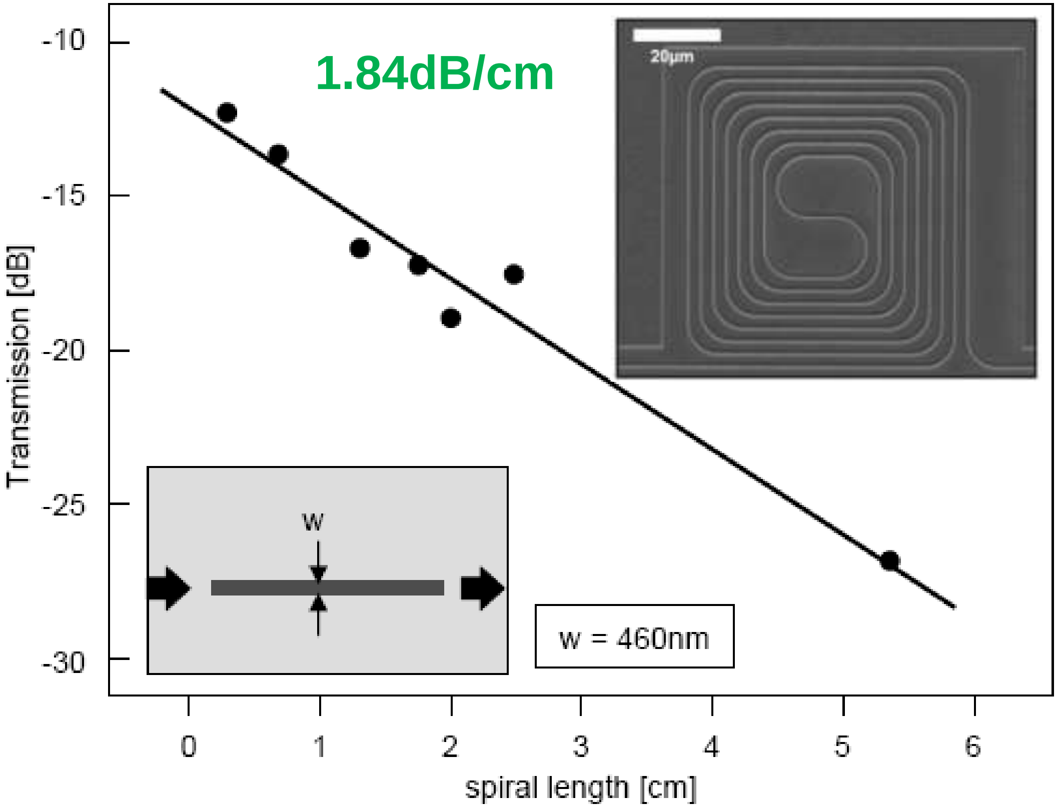
low loss
bend
complex filters
Passives
coupling
sources
switches
odulators
Actives
detectors
all functions
onics
Integration
applications

Straight waveguide

Our standard waveguide: 450nm x 220nm Si

- Fabricated using 193nm DUV lithography
- In standard pilot line, on 200mm wafer
- Starting from SOI or amorphous silicon





Bogaerts e.a. , JSTQE 16, 33-44 (2010)

Straight waveguide

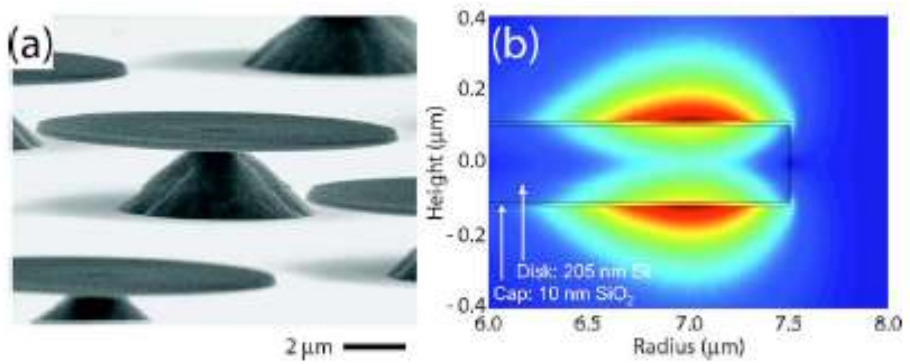
Origin of losses ?

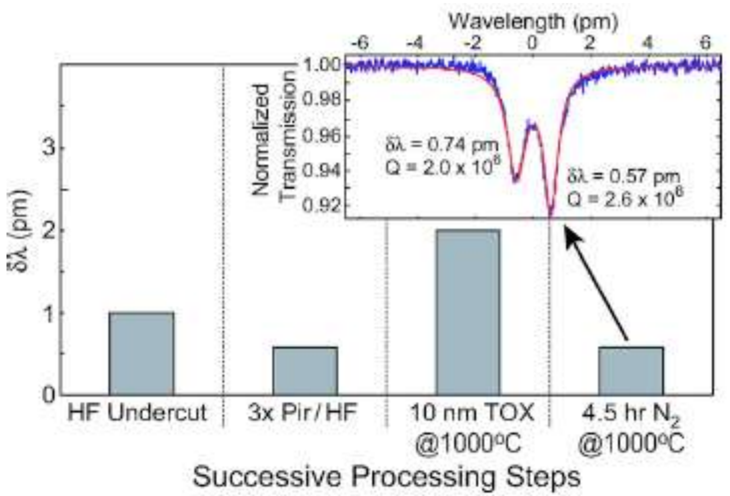
- Surface roughness
- Surface absorption

How to decrease losses further ?

- eBEAM lithography + HSQ resist **0.9dB/cm**
- Surface treatment
  - Wet or dry oxidation
  - Hydrogen or other treatment
  - Encapsulation

Gnan e.a., Electronic Lett. 44, p115 (2008)





Borselli, Painter, e.a., APL 91, 131117 (2007)

Straight waveguide

Origin of losses

- Surface roughness
- Surface absorption

How to decrease losses further ?

- eBEAM lithography + HSQ resist 0.9dB/cm
- Surface treatment
  - Wet or dry oxidation
  - Hydrogen or other treatment
  - Encapsulation
- Use wider waveguide
  - Locally multimode waveguide 0.3dB/cm
  - Include single mode filters
    - (narrow sections or bends)
- Change waveguide shape
  - Optimize confinement at interface

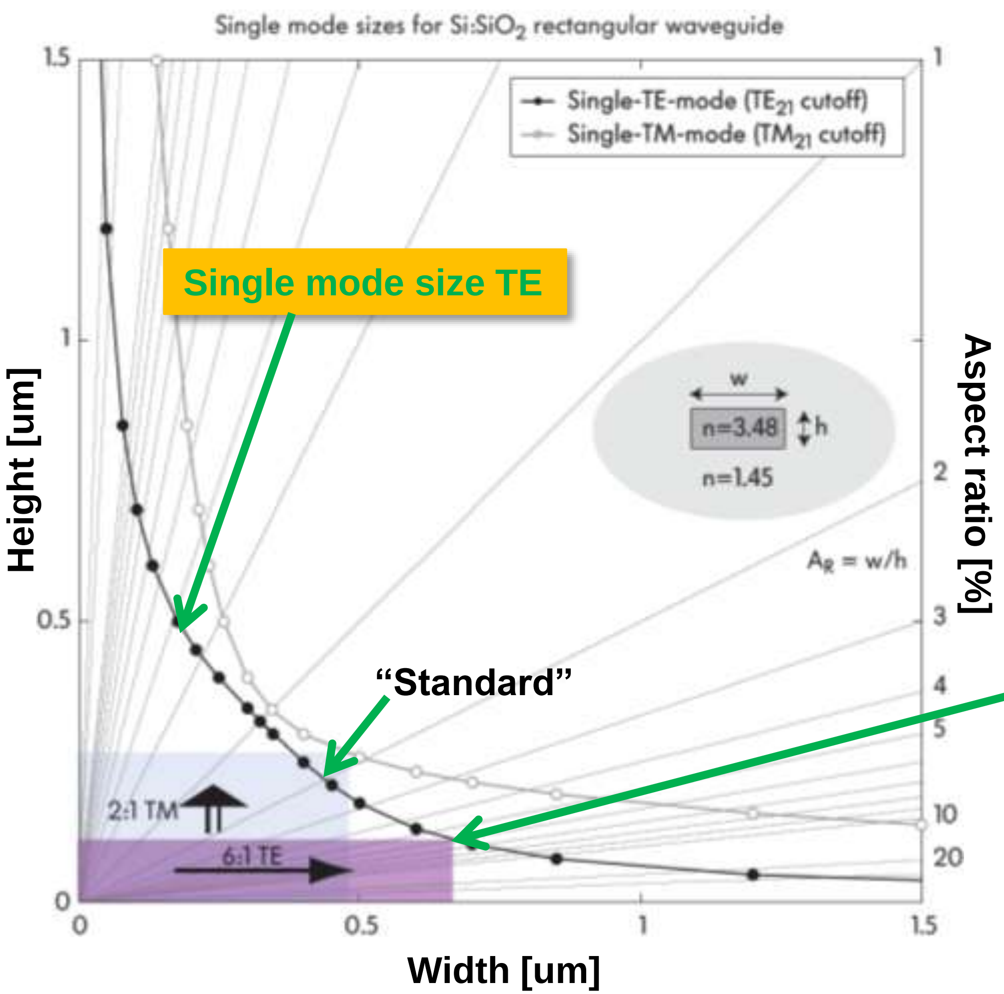
Gnan e.a., Electronic Lett. 44, p115 (2008)

Borselli, Painter, e.a., APL 91, 131117 (2007)

Spector e.a., IPRNA IThE5 (2004)
Toliver e.a. , OFC OWJ4 (2010)
Bogaerts e.a , GPF (2010)

Popovic, PhD Thesis, MIT (2008)

Straight waveguide



Popovic, PhD Thesis, MIT (2008) (http://dspace.mit.edu)

Question:

- Given certain optimization criteria
- What is optimal **aspect ratio** for waveguide ?

Popovic e.a. :

- Optimisation for:
  - Low loss,
  - Low sensitivity to dimensional variations
  - High thermal optic effect
- Choose AR = 6:1 !!!

Alternative optimisation criteria:

- High non-linear effects

  Vaillitis, Leuthold, e.a. OE 17 pp. 17357 (2009)

- Optimized sensing (overlap with outside world)

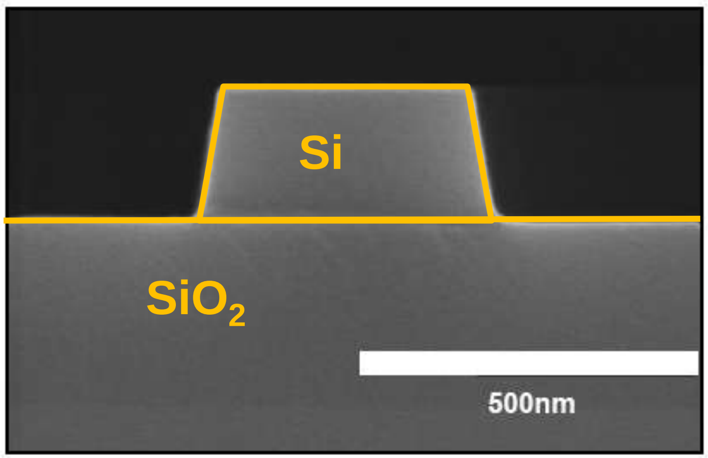
  Debackere, PhD thesis UGent (2010)

- Dispersion

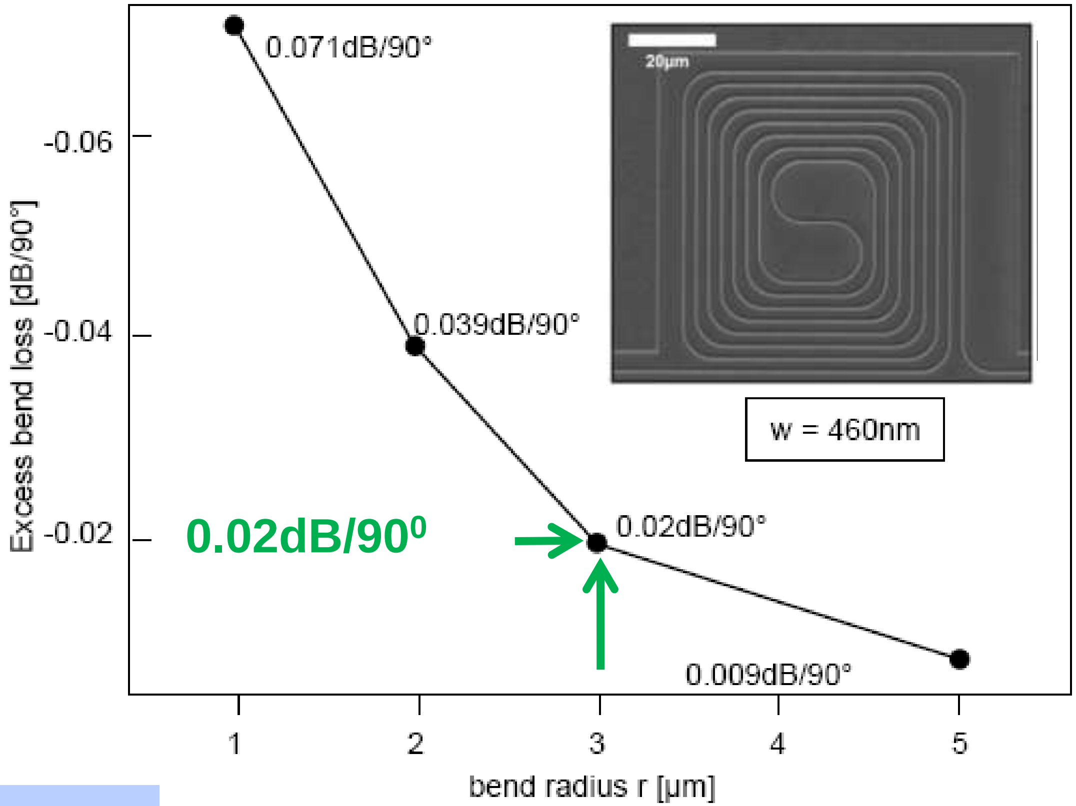
Bend waveguide

Our standard waveguide: 450nm x 220nm Si

- Fabricated using 193nm DUV lithography
- In standard pilot line, on 200mm wafer
- Starting from SOI or amorphous silicon



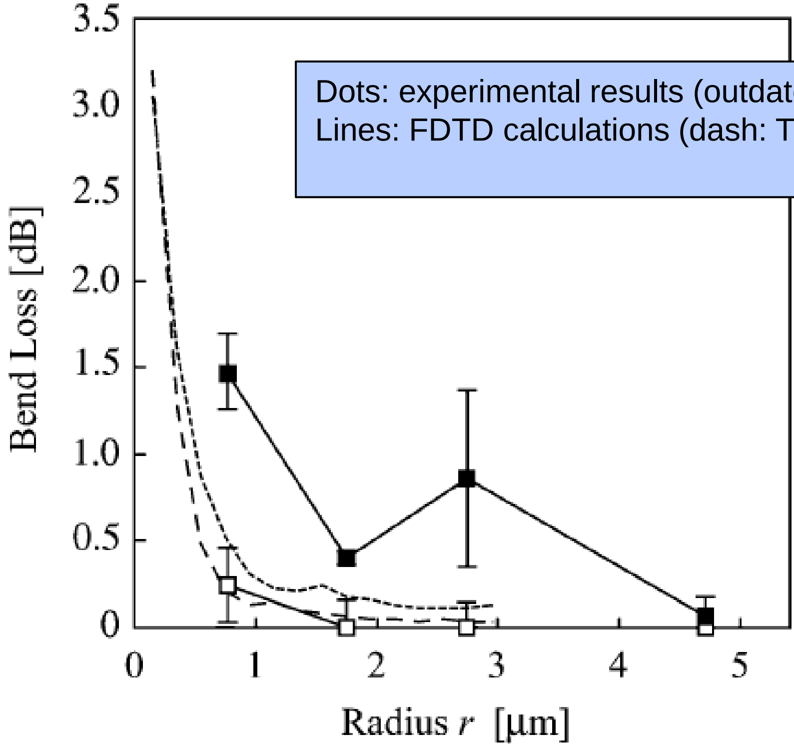
- In agreement with FDTD calculations
- Offset straigth-bend might improve (?)



S.K. Selvaraja, JLT 27, p.4070 (2009)
Y. A. Vlasov and S. J. McNab, Optics Express, p. 1622 (2004)

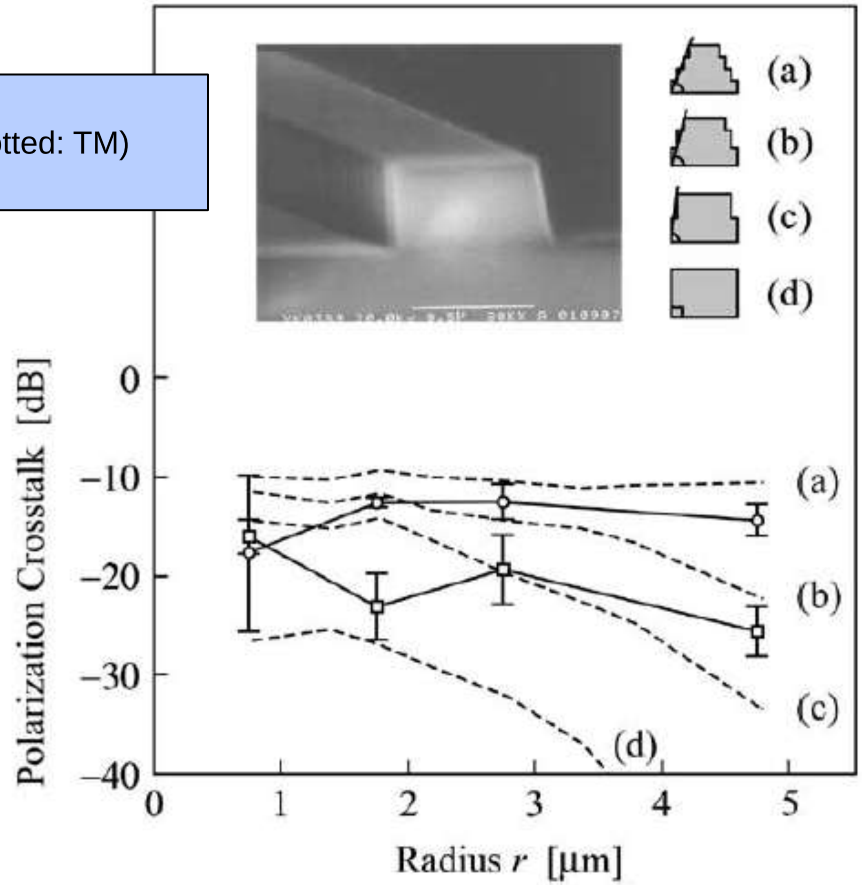
The waveguide bend

FDTD calulcations in line with recent experimental results



Dots: experimental results (outdated)
Lines: FDTD calculations (dash: TE, dotted: TM)

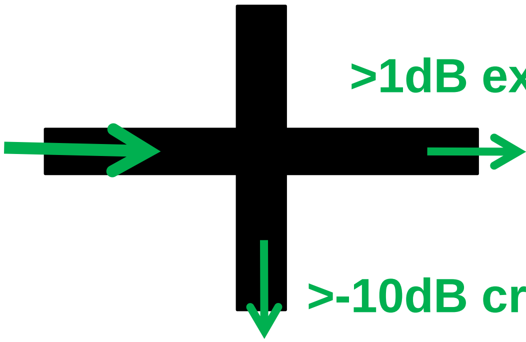
Bends may introduce unwanted polarization rotation



A. Sakai, JLT 22, pp 520 (2004)

Crossings

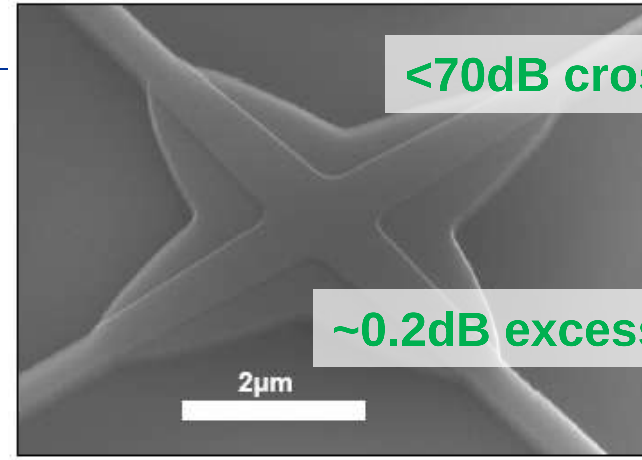
Standard Crossing



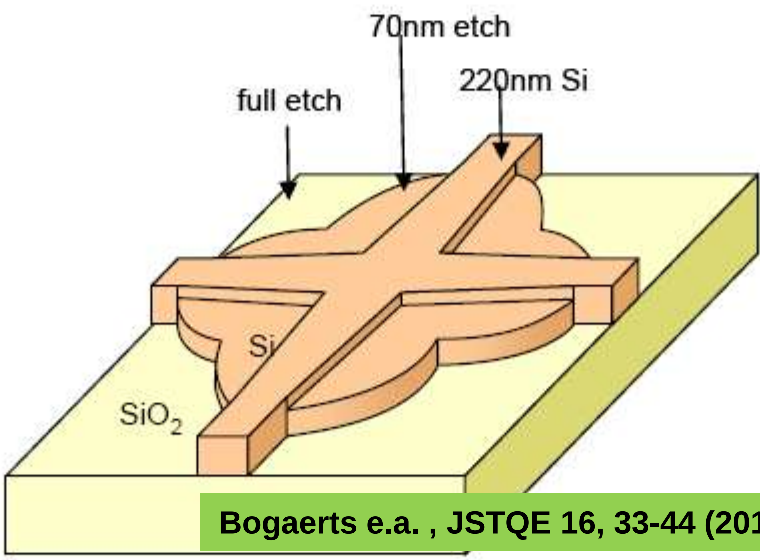
>1dB excess loss

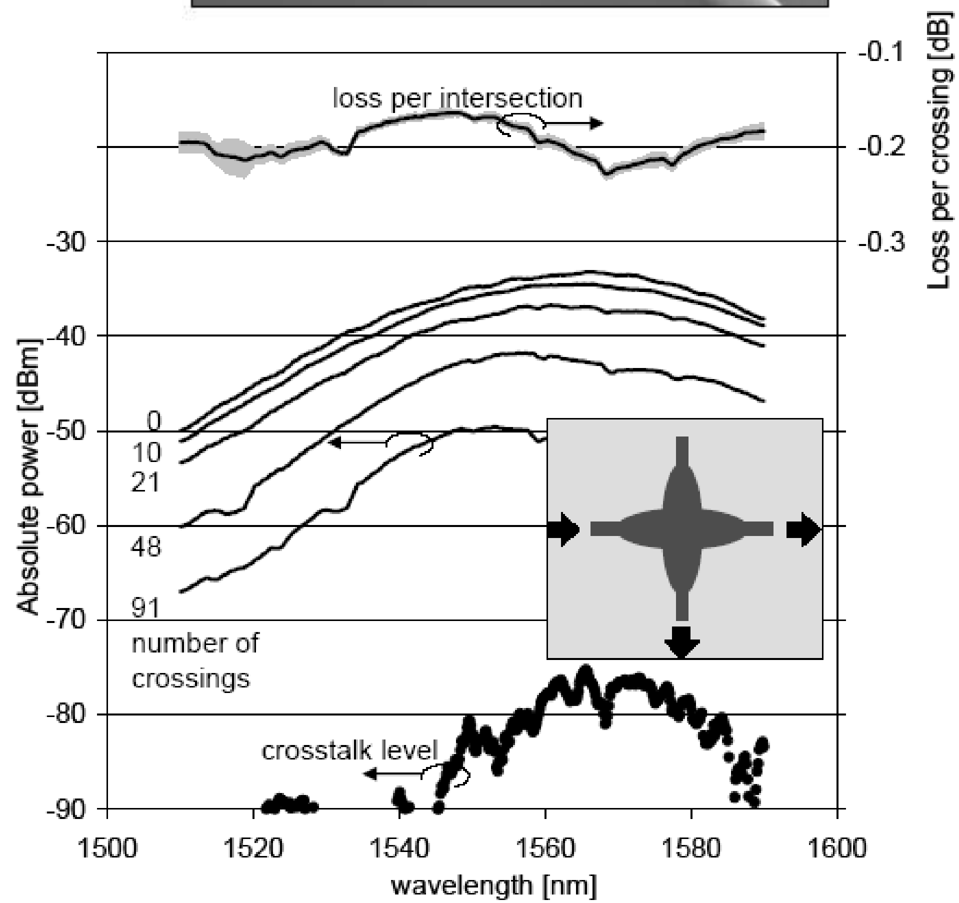
>-10dB crosstalk

Not practical !



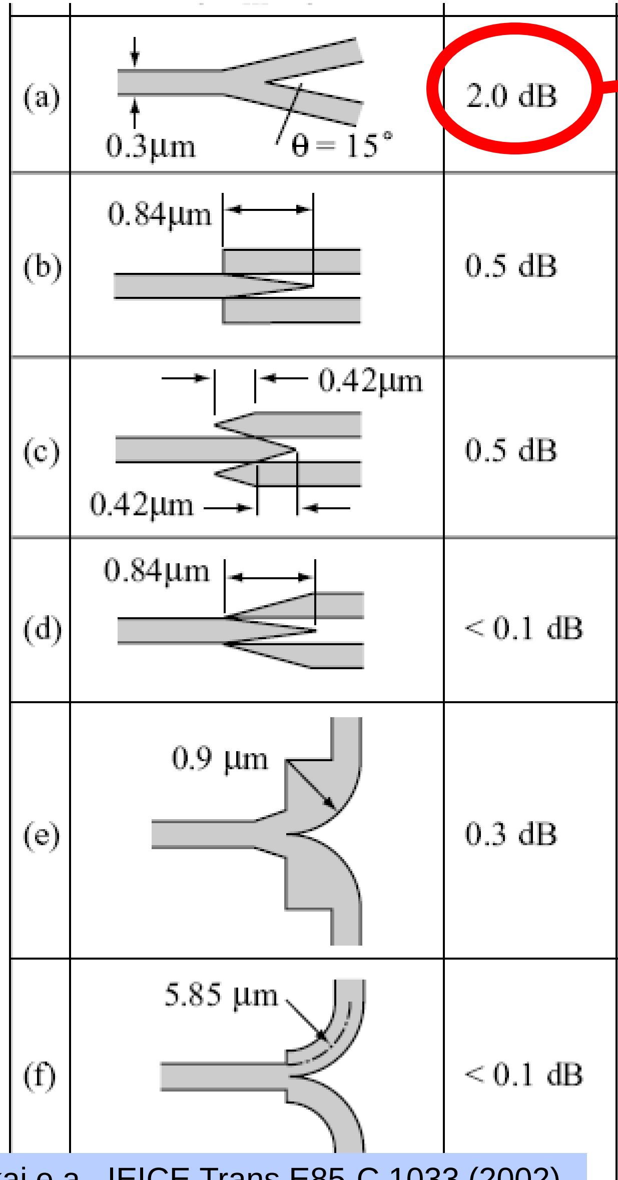
Improved version





Bogaerts e.a. , JSTQE 16, 33-44 (2010)

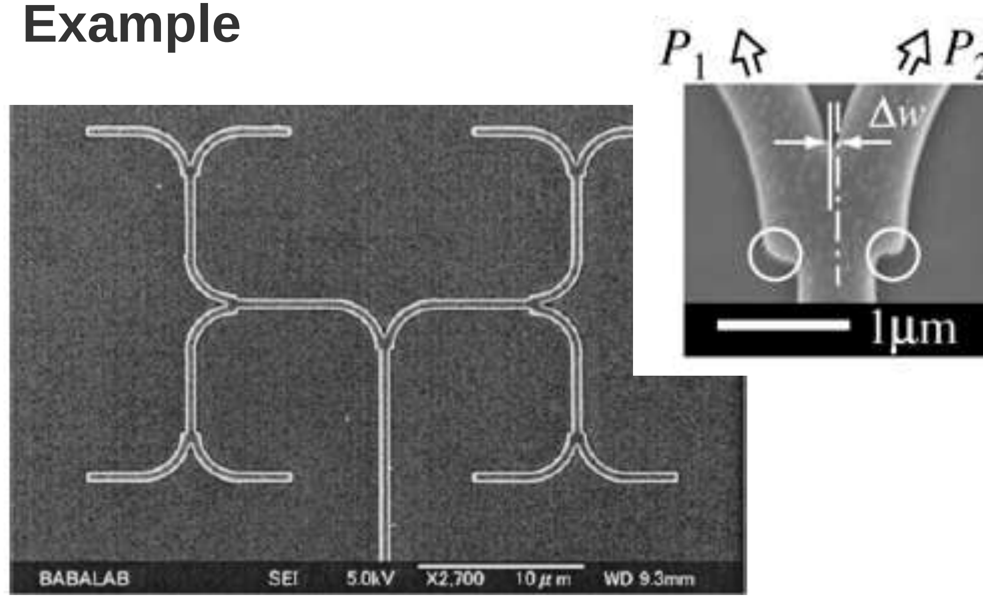
The Y-junction



Sakai e.a., IEICE Trans E85-C 1033 (2002)

Large **losses** for standard Y-junction
Need **improved** design !!!

Example



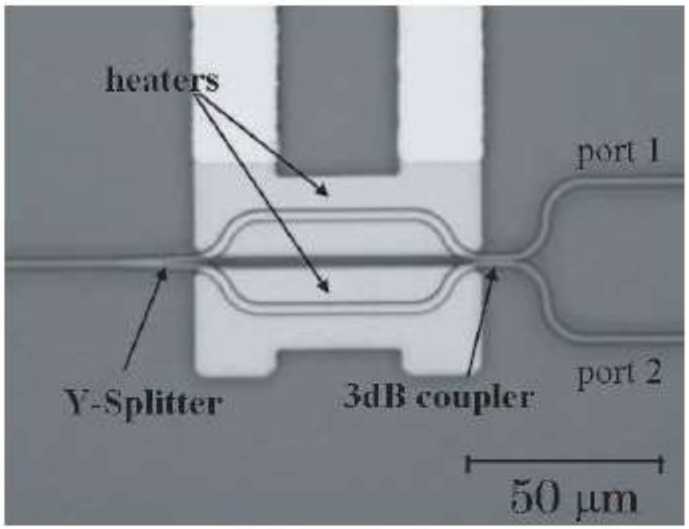
Simulation: <0.1dB excess loss

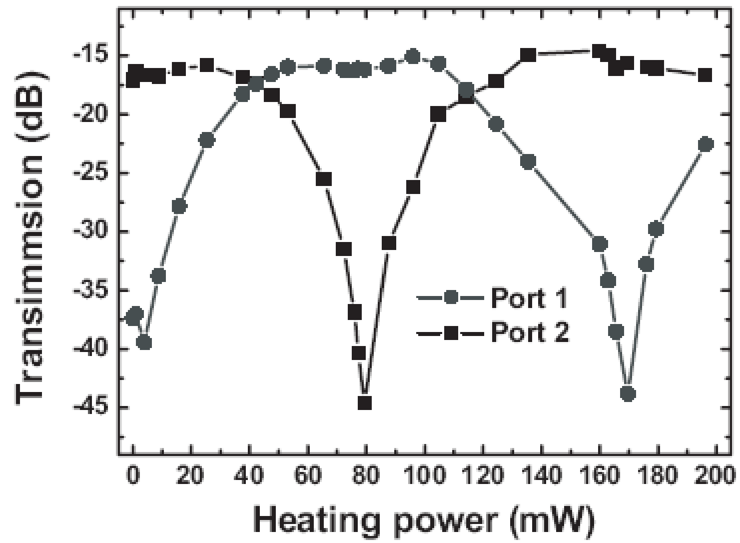
- **Experiment: 0.3dB excess loss**
- **Some imbalance due to opt. Prox.**

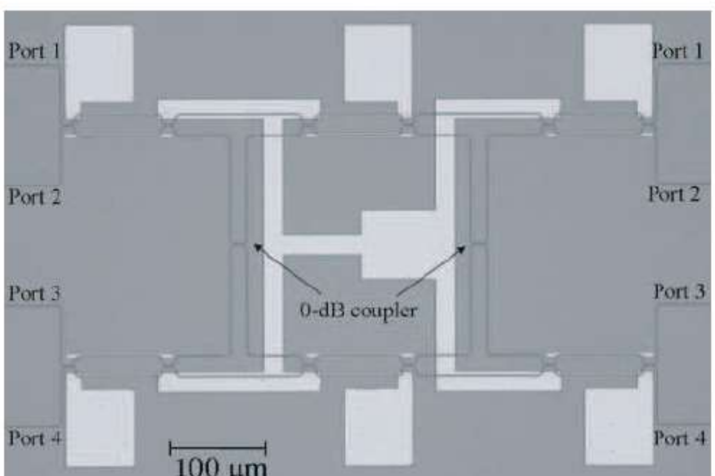
Fukazawa e.a. Jpn JAP 41, p L1461 (2002)

The Y-junction

Use Y-junctions to fabricate TO-switches





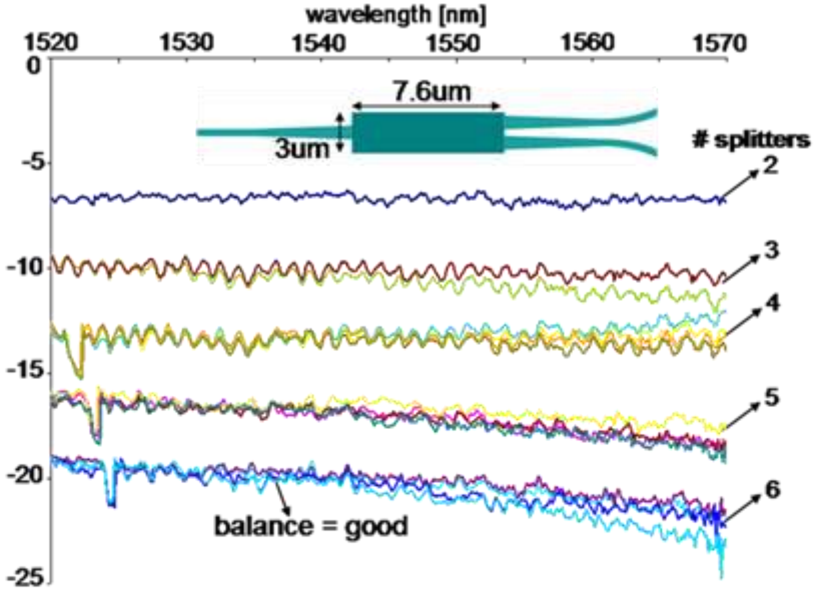


4 x 4 switch

Yamada e.a., PIERS proc., Beijing, p. 22 (2009)

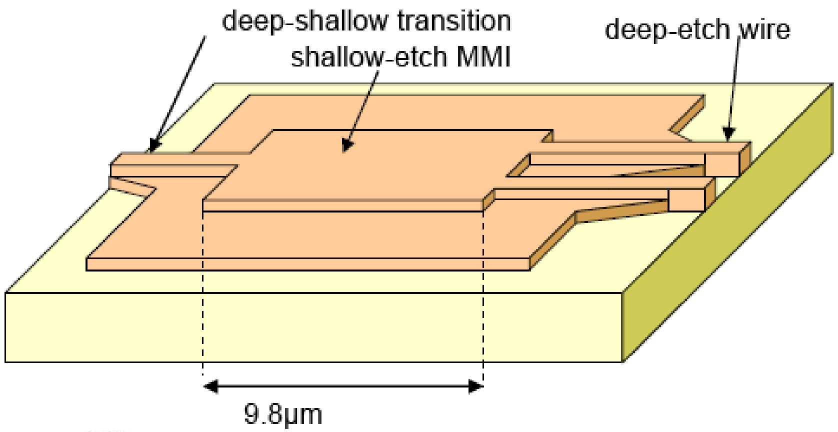
Passive guiding structures

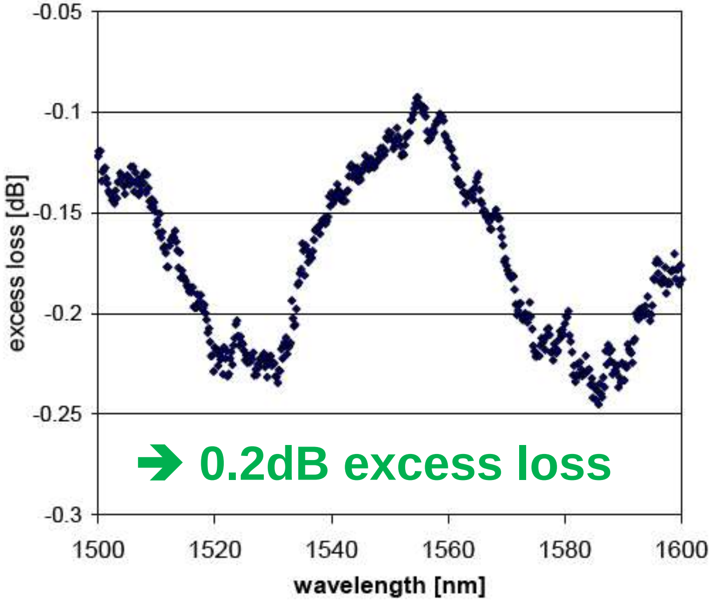
Standard MMI splitter



➔ 0.3dB excess loss

Improved version



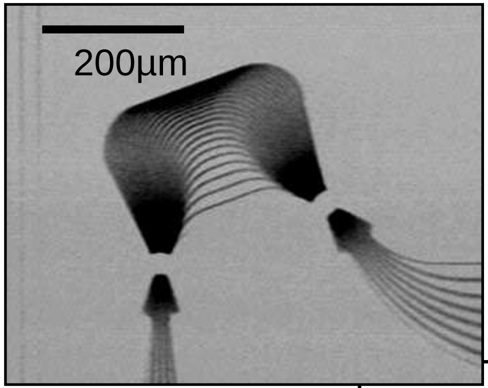


➔ 0.2dB excess loss

Bogaerts e.a. , JSTQE 16, 33-44 (2010)

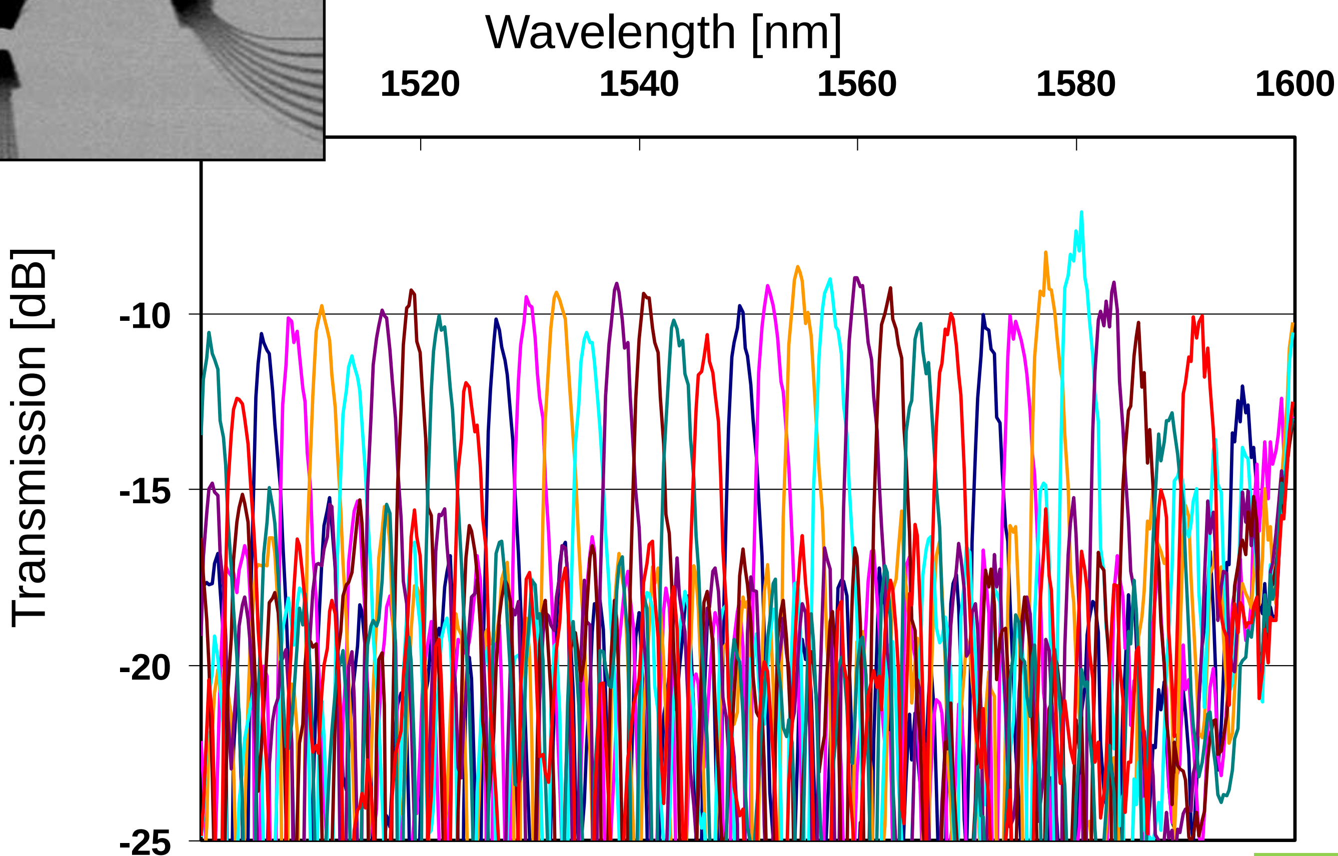
Arrayed waveguide grating routers

Original devices



Compact, but …

- High loss (8dB)
- High crosstalk (only 7dB down)



Dumon e.a. , GFP 2004

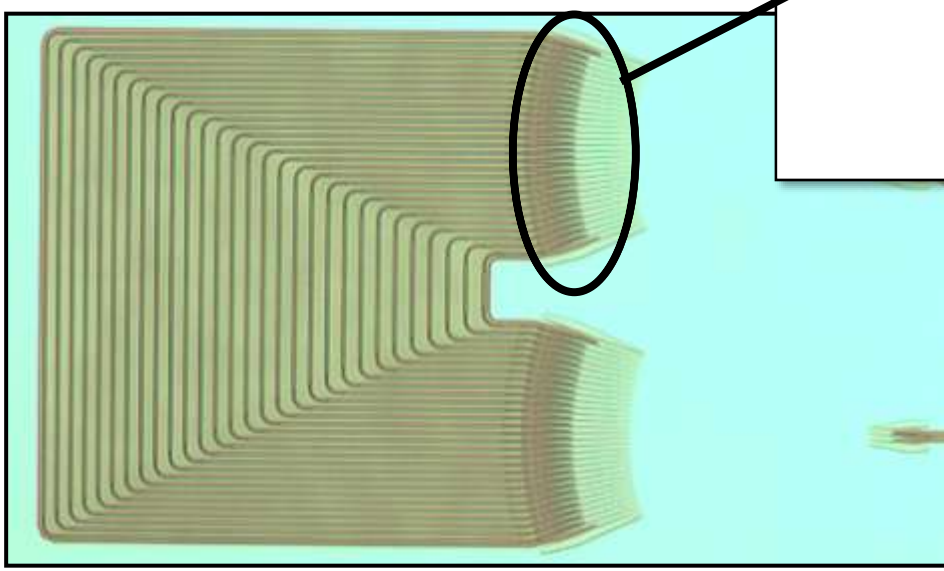
Arrayed Waveguide Grating

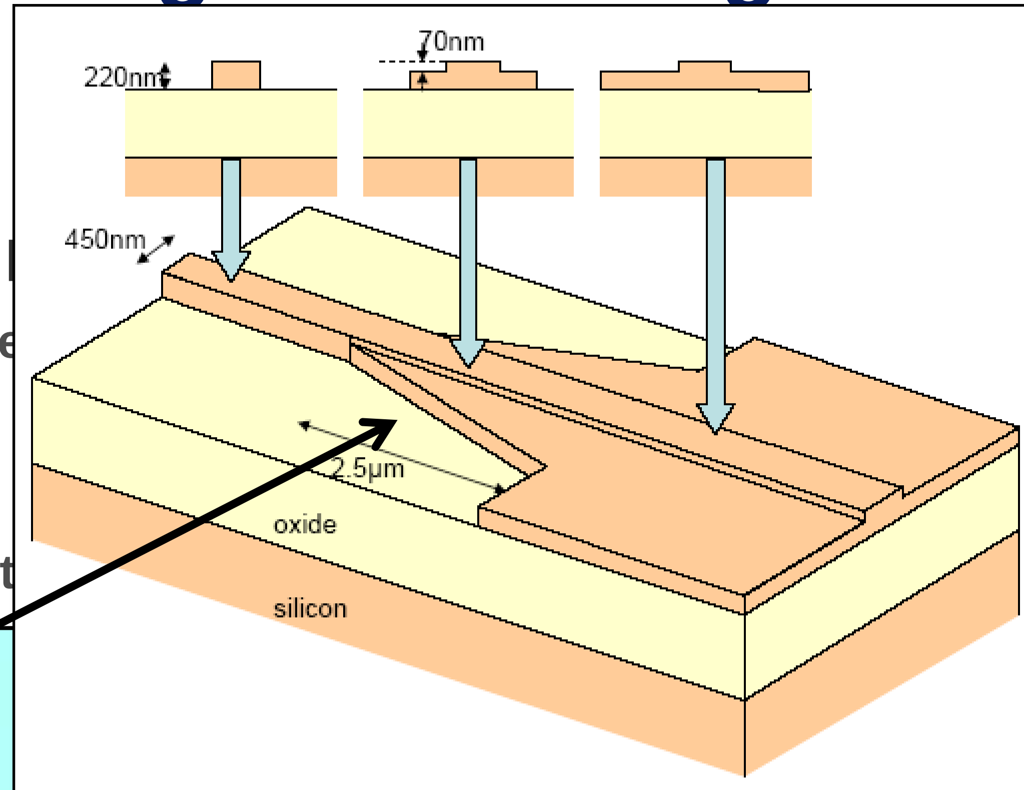
8-channel, 400GHz

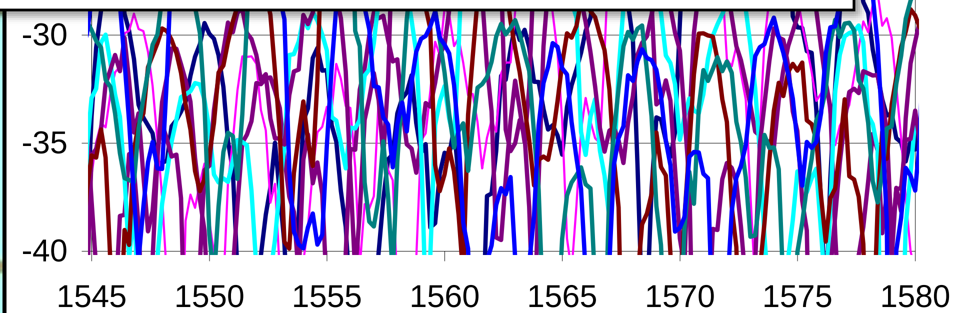
FSR = 30nm

footprint = 200 x 350

- **-25 dB crosstalk leve**
- **-1 dB insertion loss (center channel)**
- **1.5 dB non-uniformit**







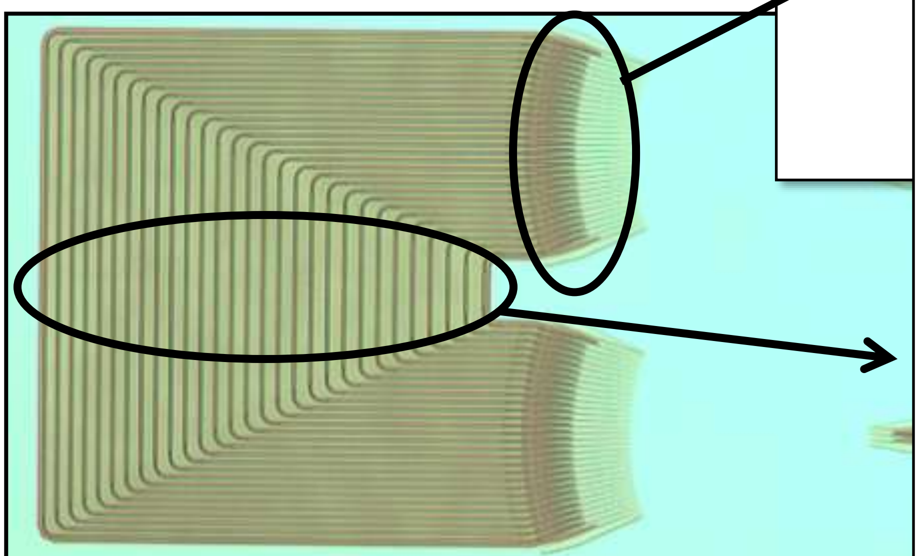
Arrayed Waveguide Grating

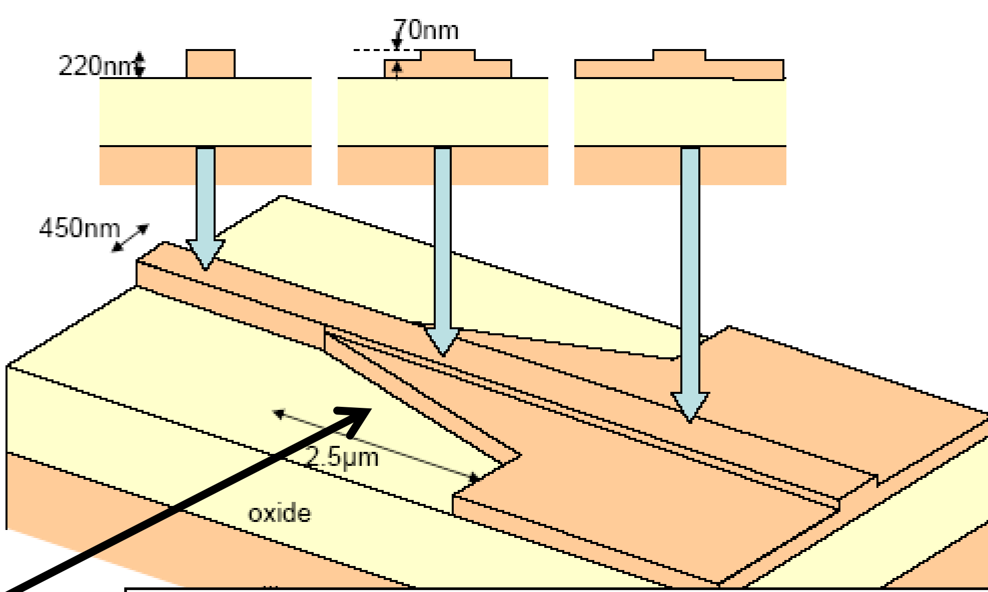
8-channel, 400GHz

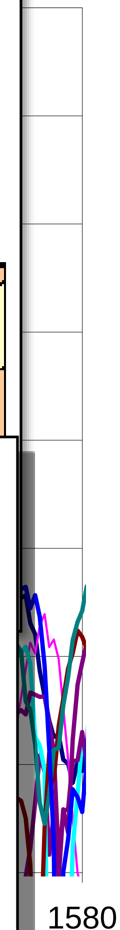
FSR = 30nm

footprint = 200 x 350 |

- **-25 dB crosstalk leve**
- **-1 dB insertion loss (center channel)**
- **1.5 dB non-uniformit**

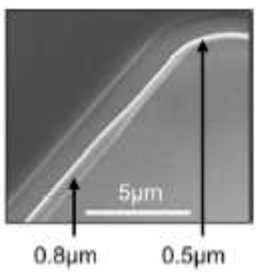






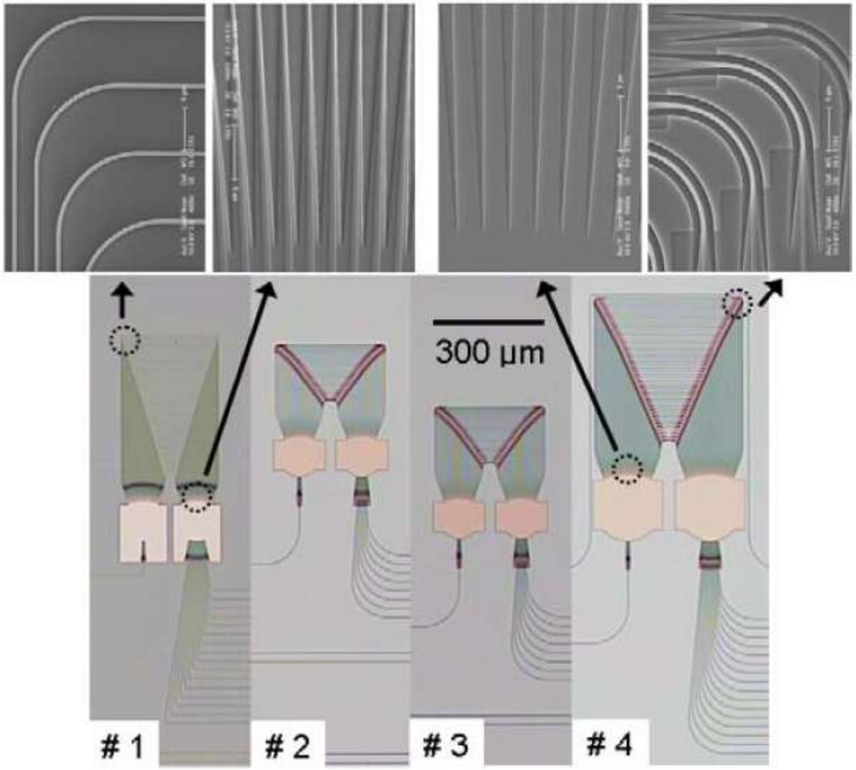
Decrease phase errors

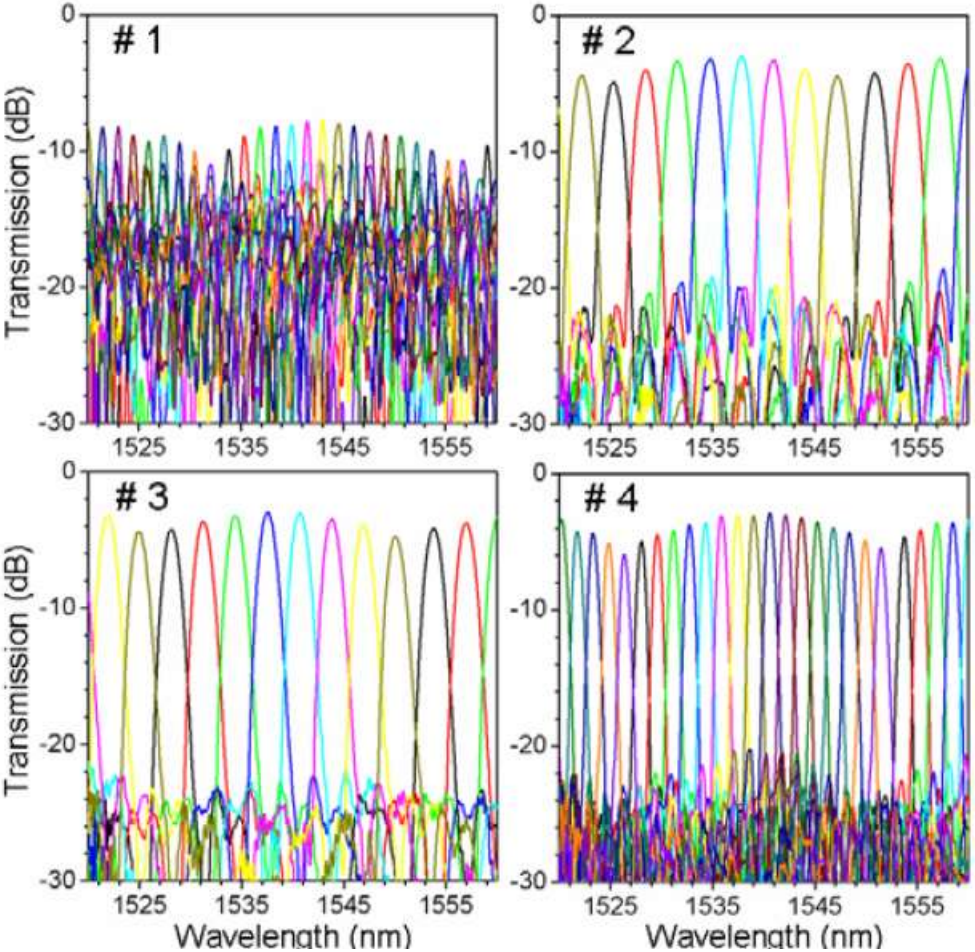
- **Use wider waveguides**



- **Align waveguides to grid**
- **See also:** P. Dumon, PhD thesis UGent 2007 (http://photonics.intec.ugent.be)

Use of shallowly etched waveguides for crosstalk reduction

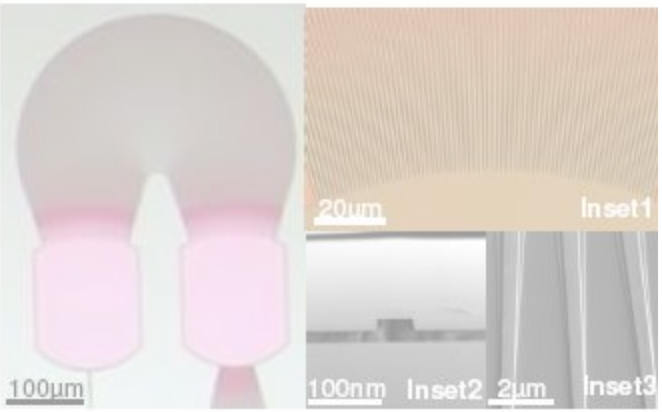


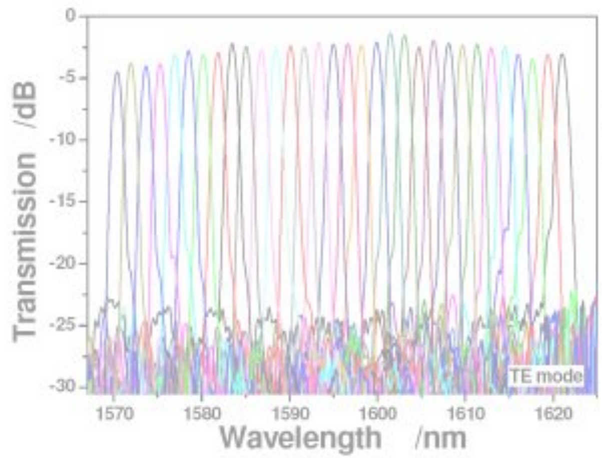


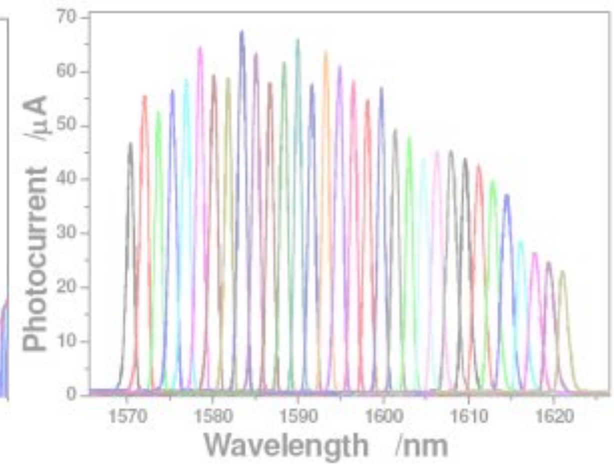
DJ Kim e.a. PTL 20 (17-20) p 1615 (2008)

Arrayed Waveguide Grating

Example: 320GB/s receiver







Fang e.a., OE 18 pp. 5106 (2010)

Silicon AWG for wavelength selective operations

- ☺ Channels spacing globally fixed
- ☺ Low loss (1dB)
- ☺ 1 x N and N x N operation with same device
- ☹ Crosstalk > 25dB difficult to obtain
- ☹ Small channel spacings (<=100GHz) difficult

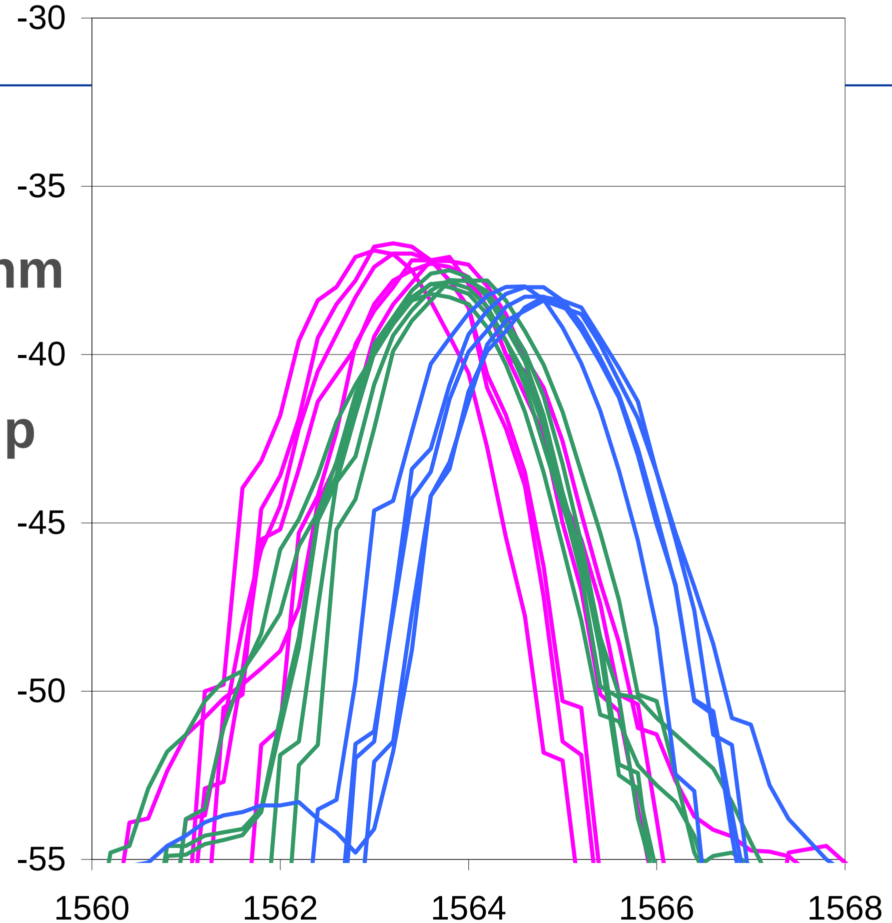
Reproducibility

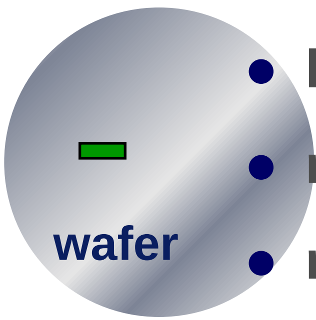
18 identical AWGs

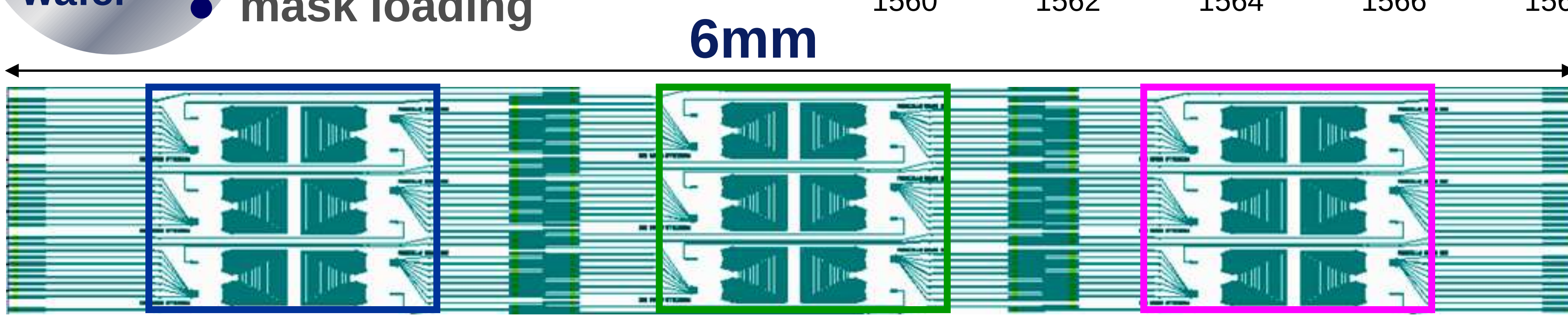
- shift in channel peak ~ 2.5nm
- strong correlation with location of the AWG on chip

Possible causes

- center-to-edge on wafer
- lithography scanning
- mask fabrication
- mask loading

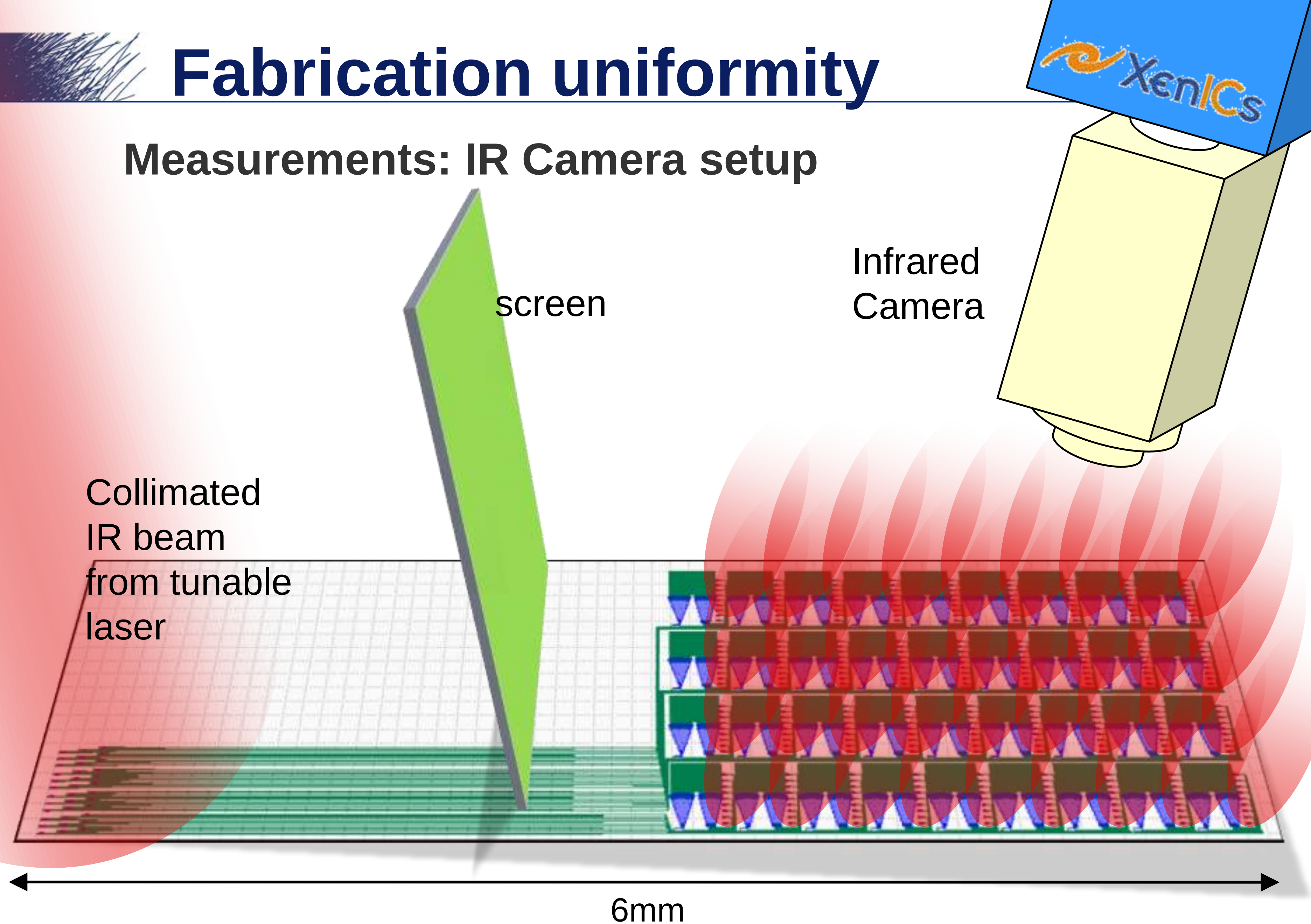




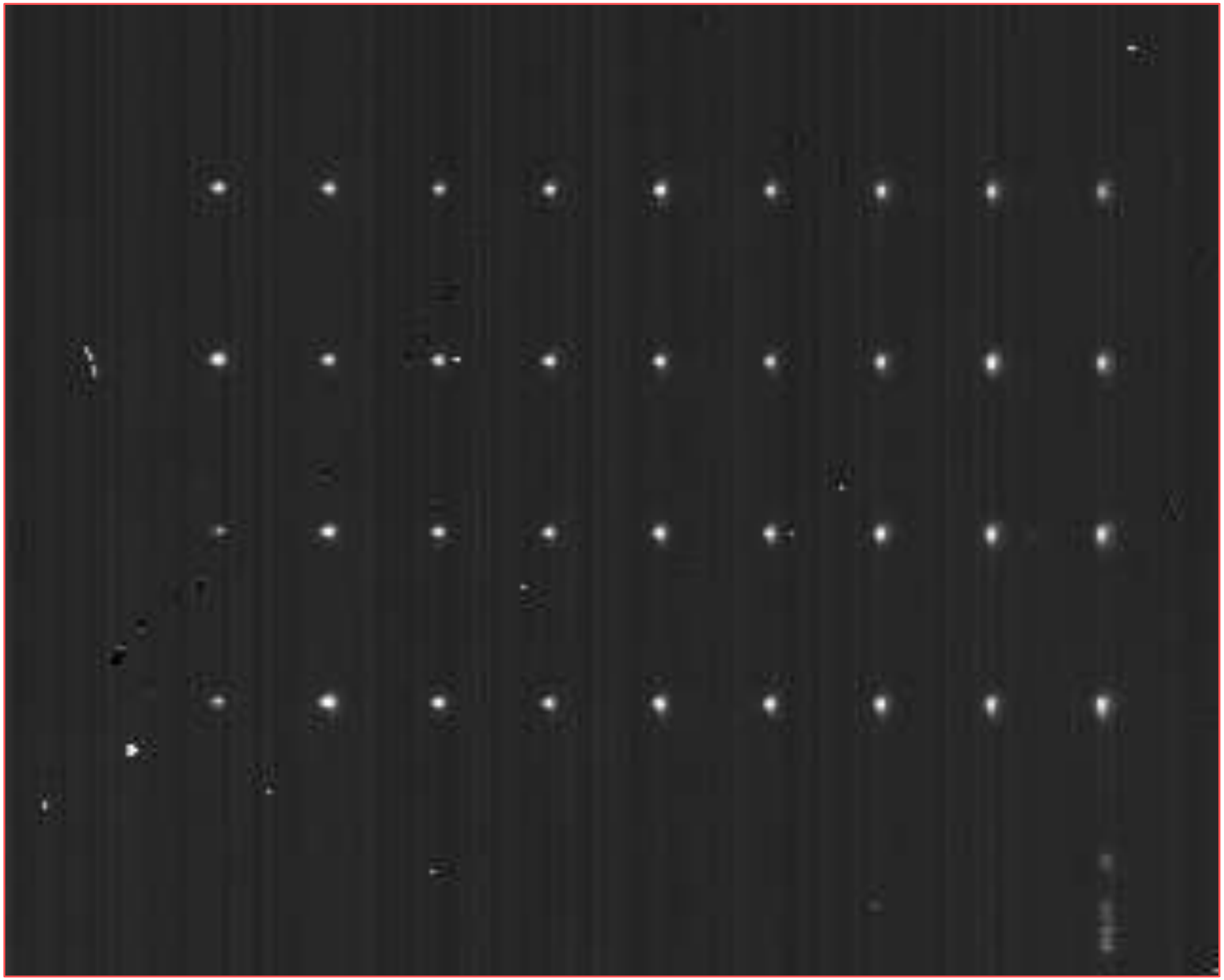


Fabrication uniformity

Measurements: IR Camera setup



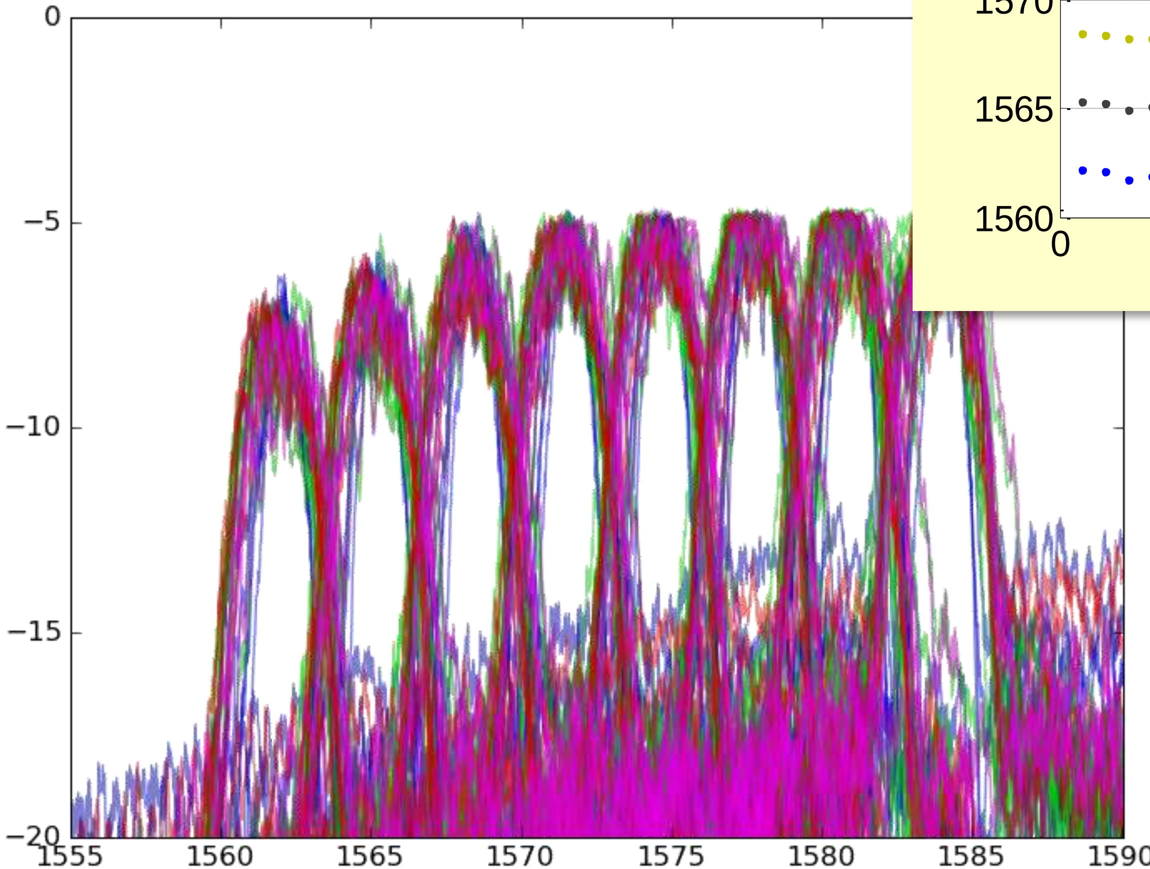
Camera view

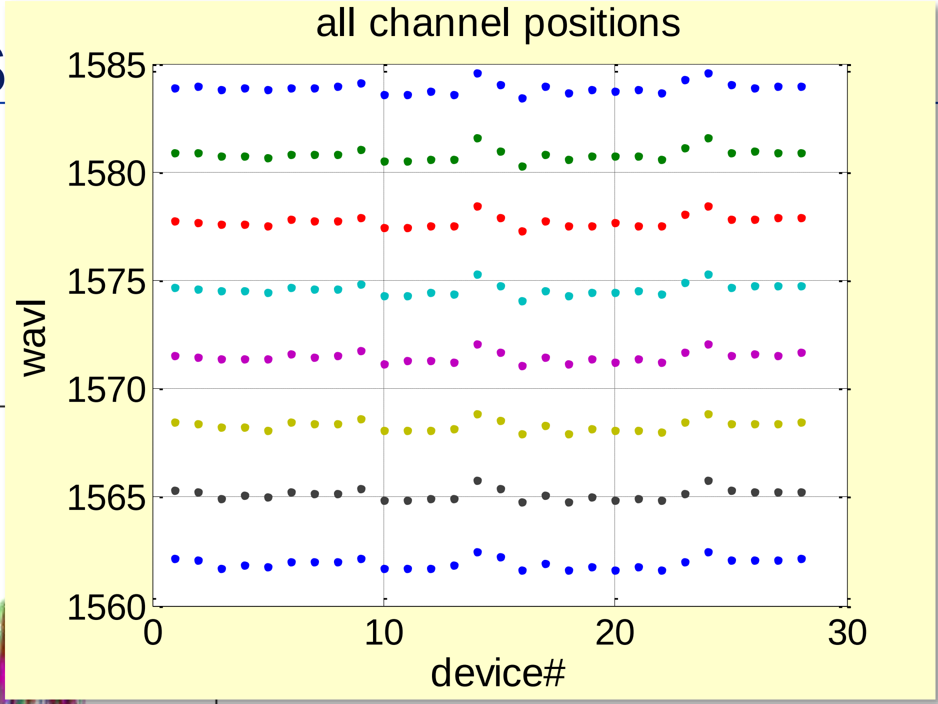


1588nm

Measurements

All rows

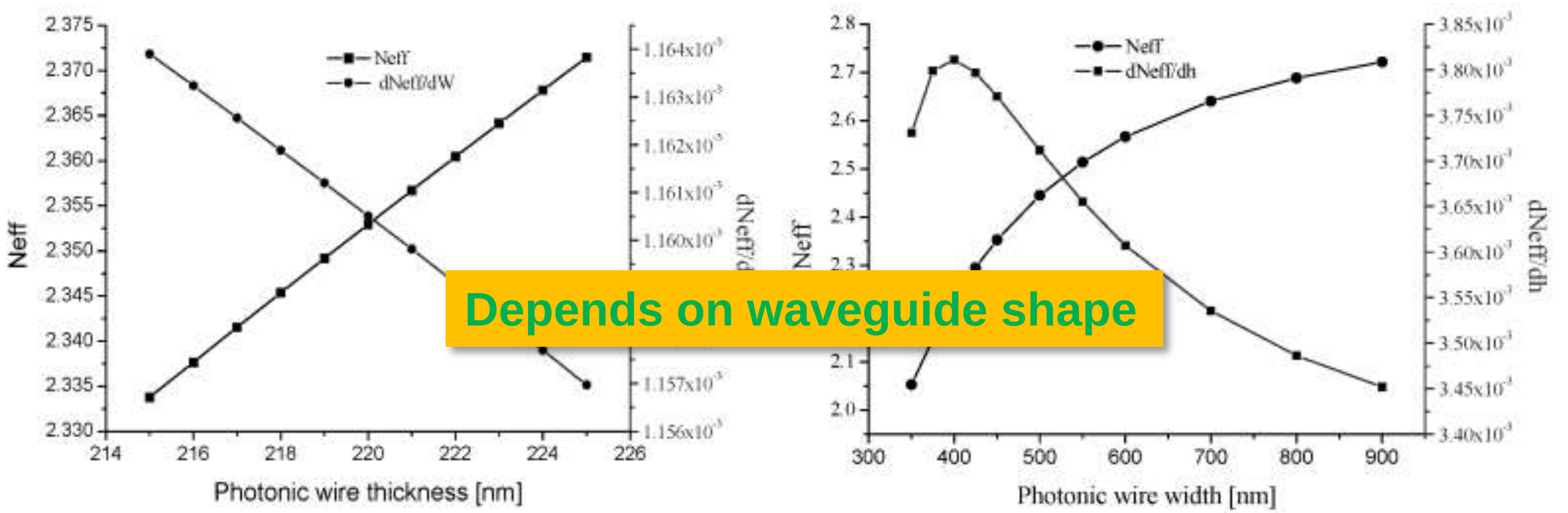




Challenges: sensitivity

Fabrication:

- Sensitivity to fabrication errors

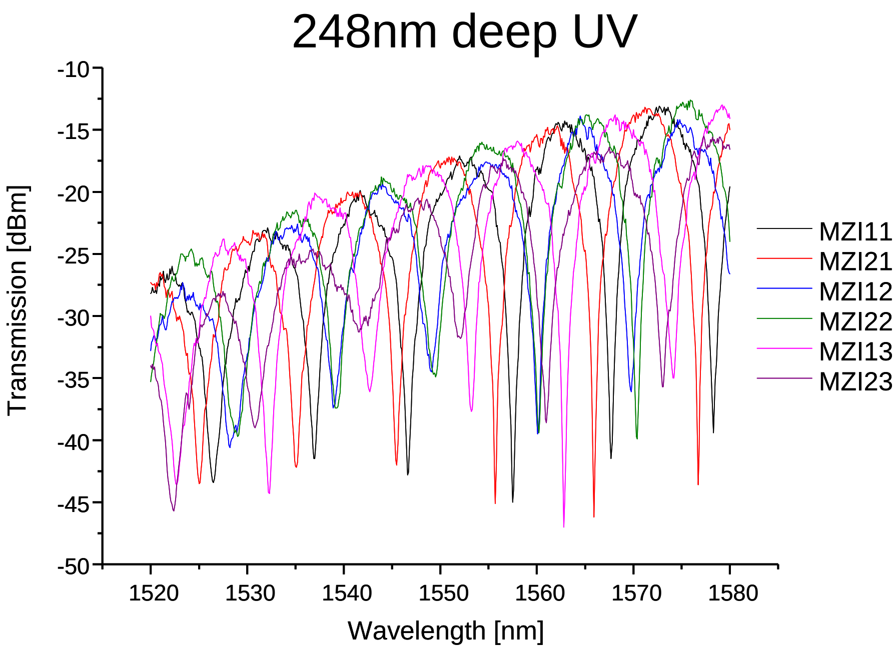


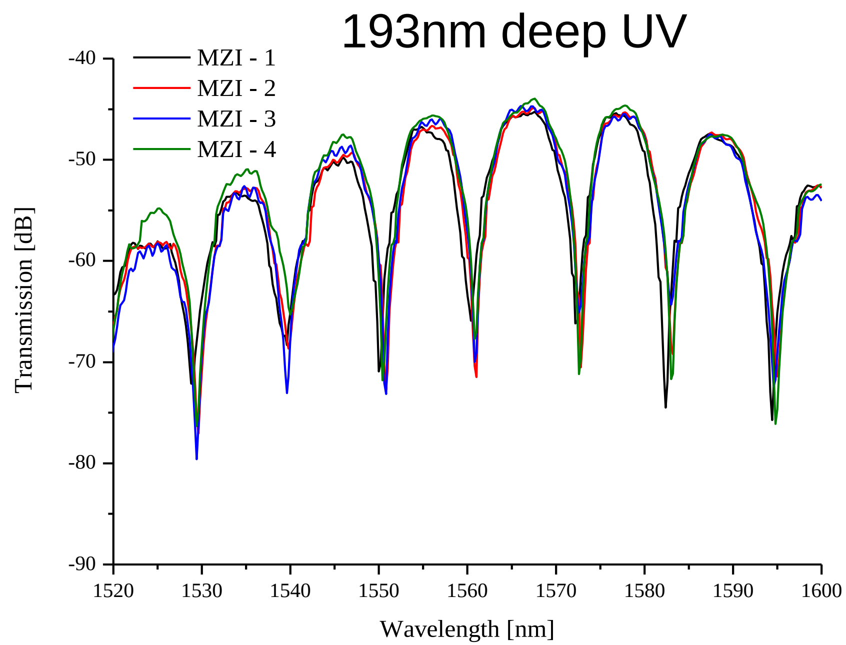
Roughly: 1nm variation in line width / thickness

1nm variation in central wavelength of device

Device uniformity

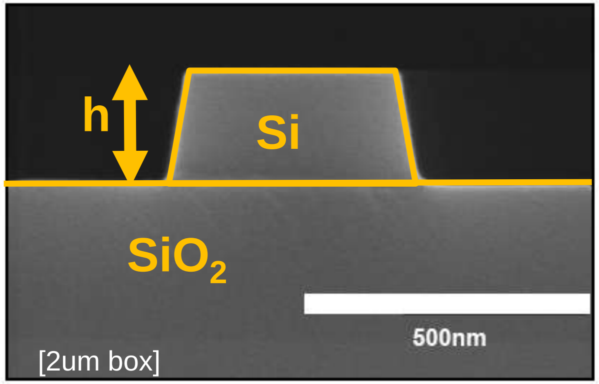
Influence of fabrication technology





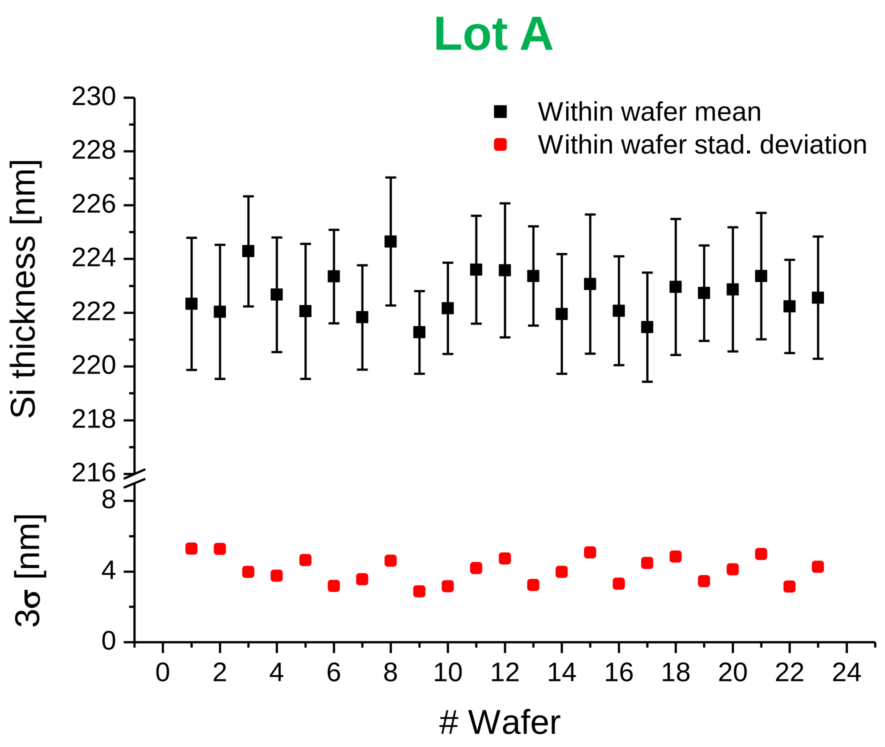
- **6 MZI's located 2mm apart**
  - **248nm very far of from specs**
  - **193nm <2nm variation over die**

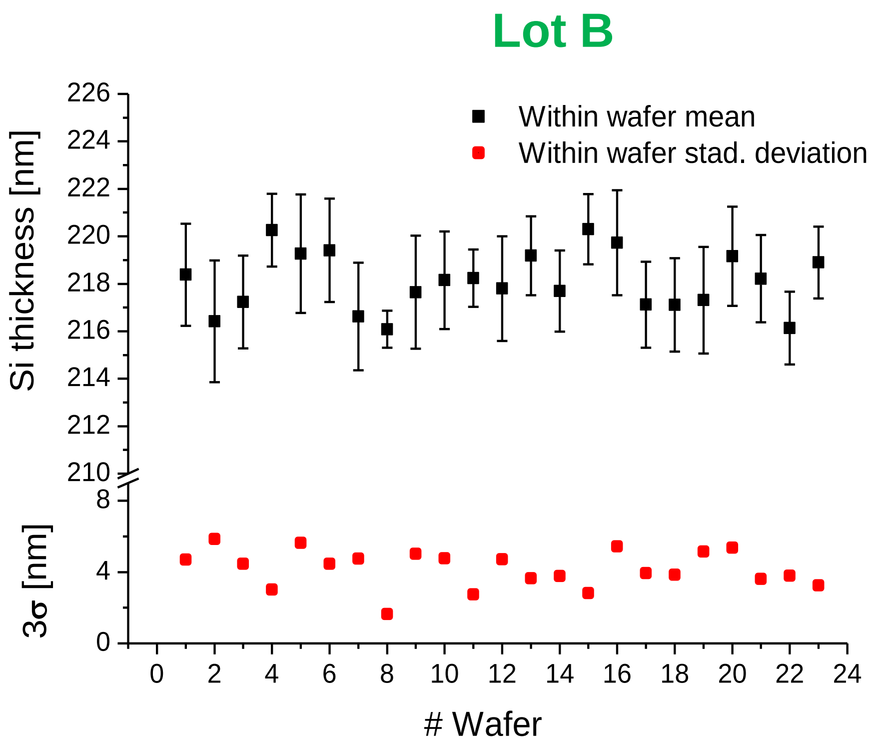
Wafer Uniformity



Thickness variation over incoming wafer (SOITEC©)

- 4nm variation within wafer
- 3nm variation wafer-to-wafer (within lot)
- 4nm lot-to-lot



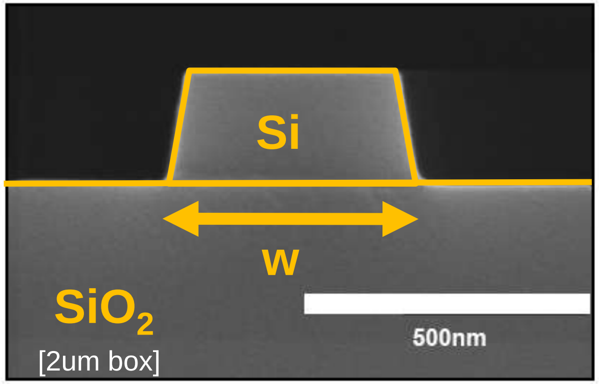


(circular within wafer pattern – determined by CMP process)

Wafer Uniformity

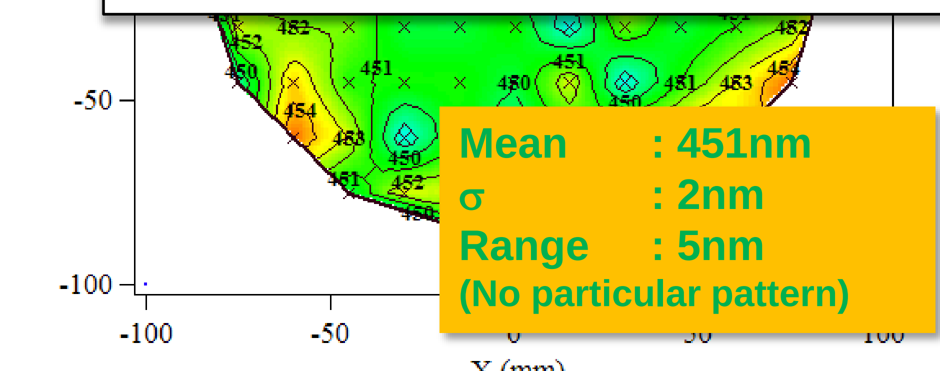
Linewidth variations

- Measured using top-down SEM

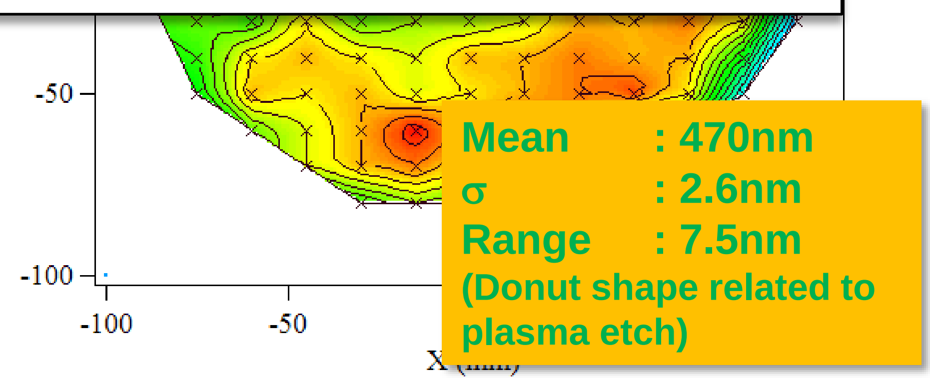


Variations in linewidth over 200mm wafer

- Less than 1% line width variation over 200mm wafer
  - Much better than typical CMOS specs
  - 1% is still 5nm !!
  - Pure passive, further post processing may increase problem (e.g. stress …)
- SEM not accurate enough to characterize within die uniformity !!



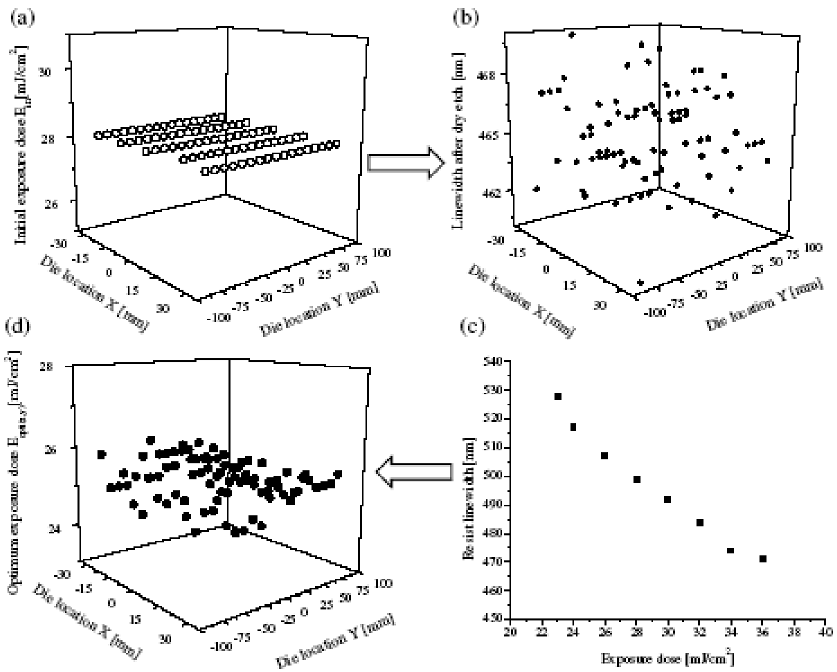
Mean : 451nm
σ : 2nm
Range : 5nm
(No particular pattern)

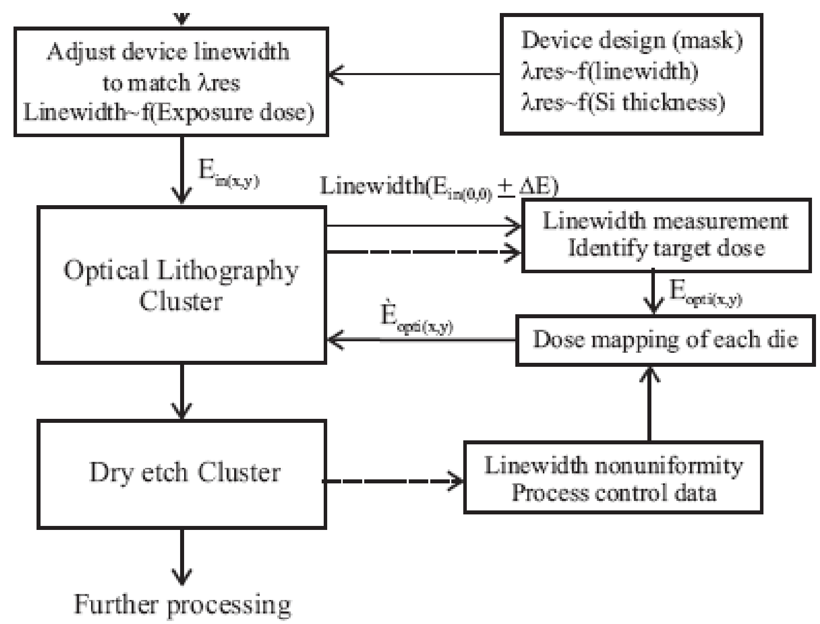


Mean : 470nm
σ : 2.6nm
Range : 7.5nm
(Donut shape related to plasma etch)

Manufacturability

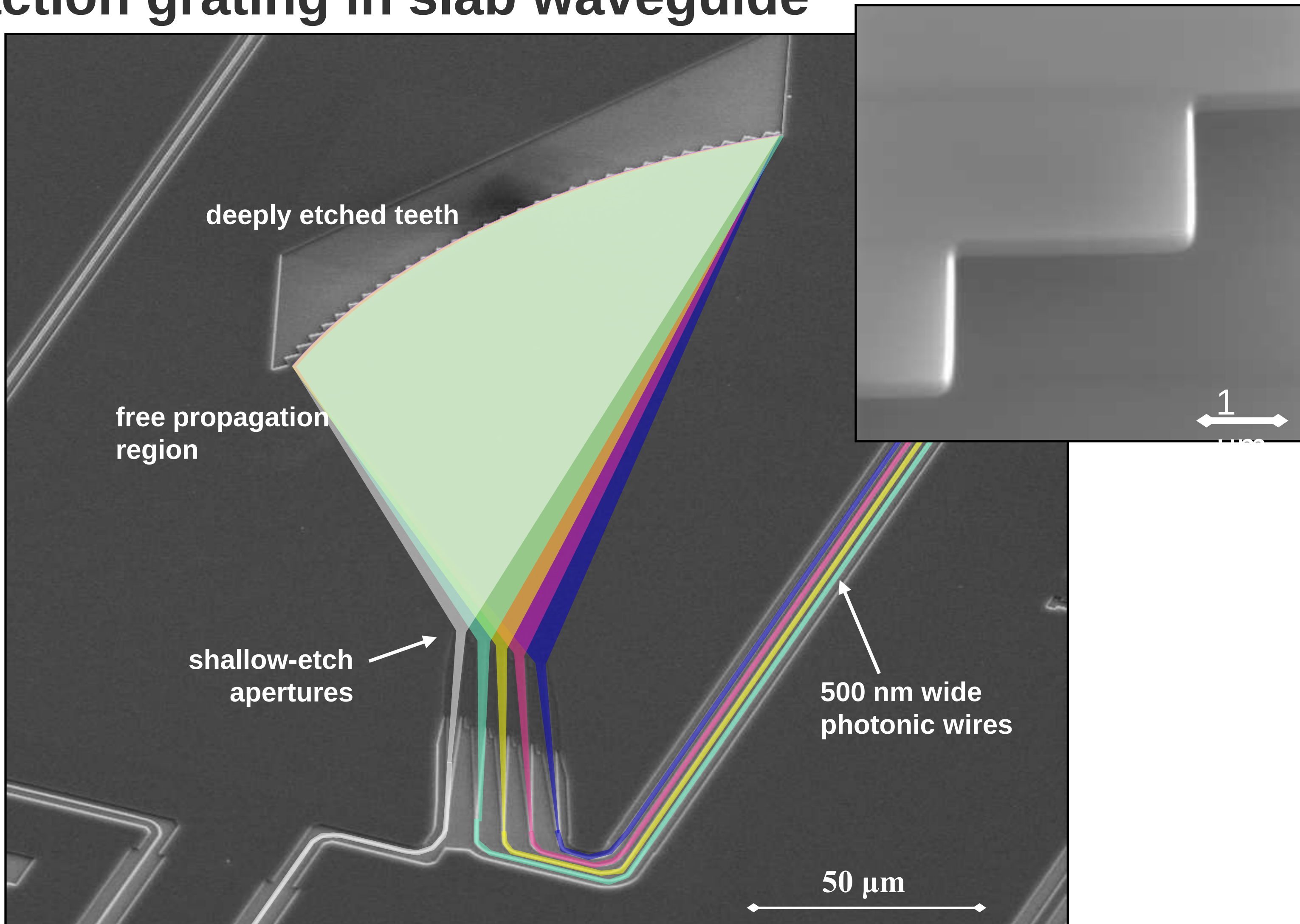
Proposed solution





Planar Concave Gratings

Diffraction grating in slab waveguide



J. Brouckaert et al. JLT 25(5), p1269 (2007)

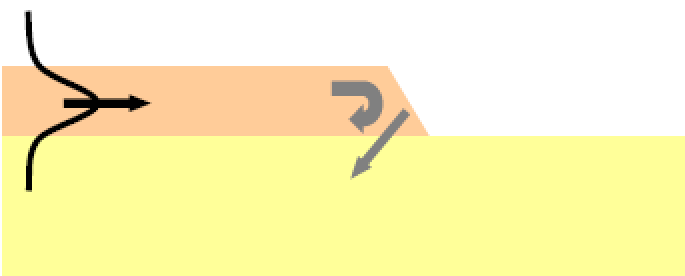
Planar concave gratings

Why PCG in nanophotonic silicon ?

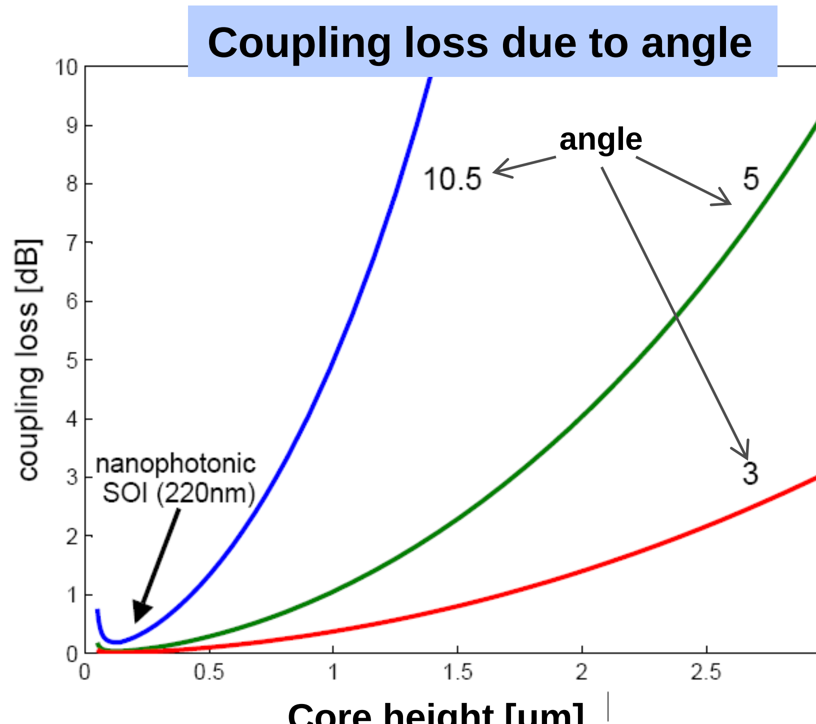
- (Hopefully) Less sensitive to phase errors
  - PCG: transmission in slab
  - AWG: transmission in waveguides
- Properties less sensitive to process variations

Horst, OFC 2010, OWJ3

- Compared to other material systems:
  - No deep etch required
  - Less sensitive to side wall angle

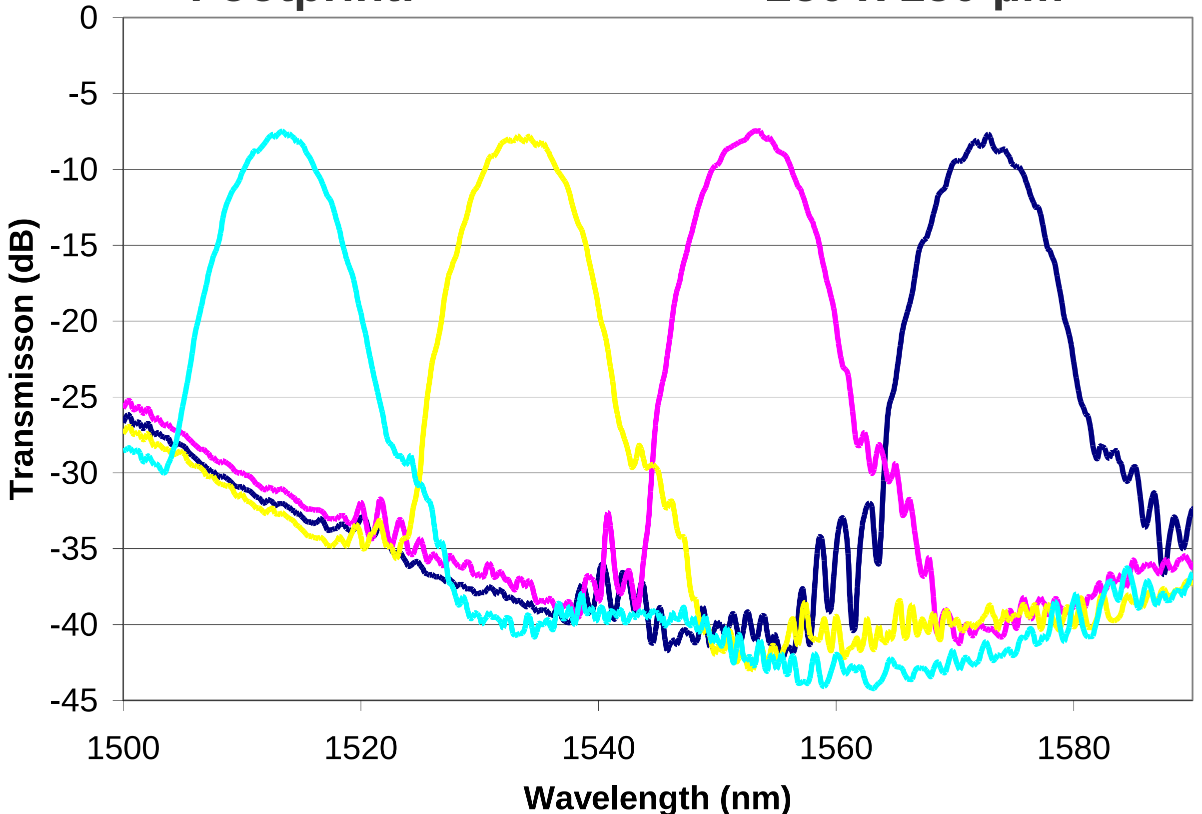


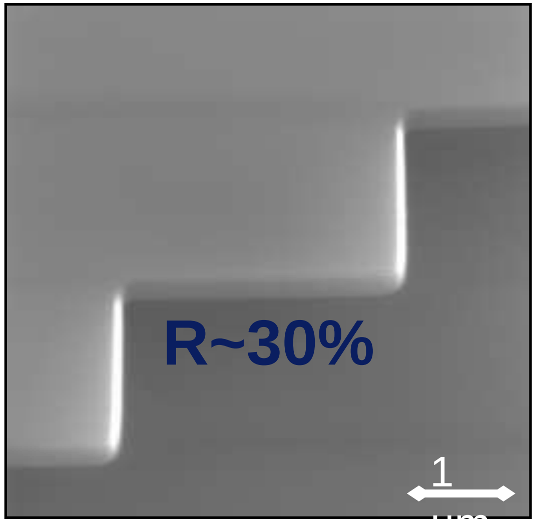
Si waveguide has high NA !!

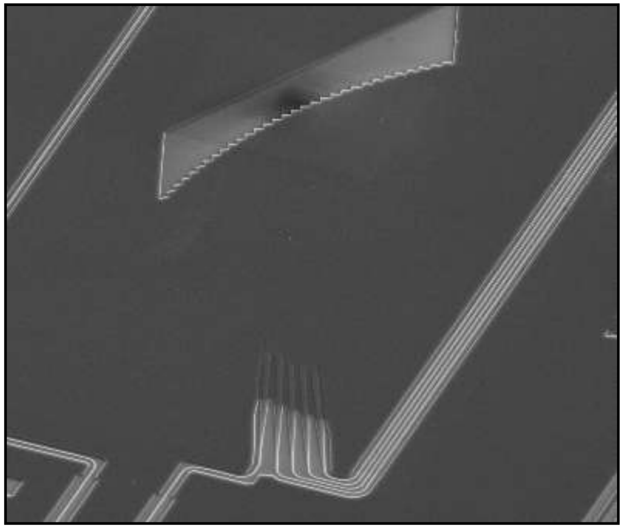


Grating Demultiplexer

Channel spacing:	**20nm**
Insertion loss:	**7.5dB**
Channel uniformity:	**0.6dB**
Crosstalk:	**better than -30dB**
Footprint:	**250 x 150 μm^2**





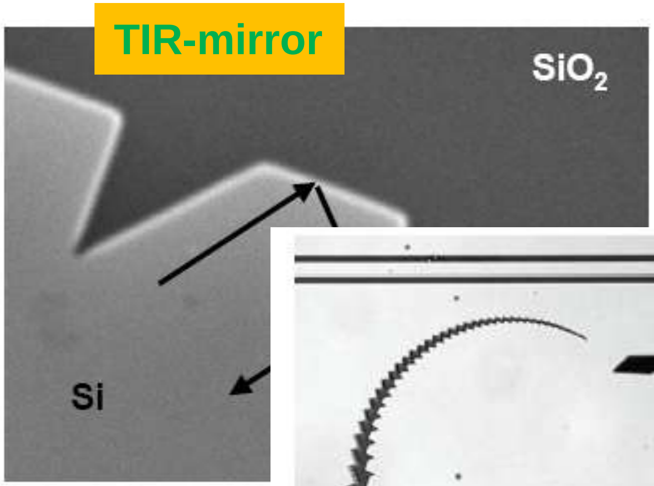


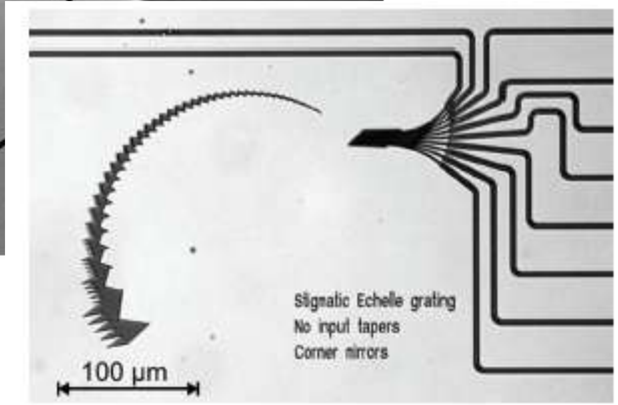
J. Brouckaert et al. JLT 25(5), p1269 (2007)

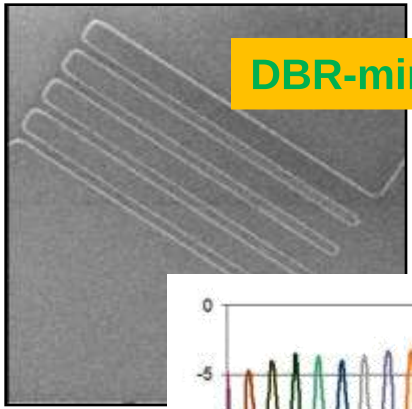
Grating Demultiplexer

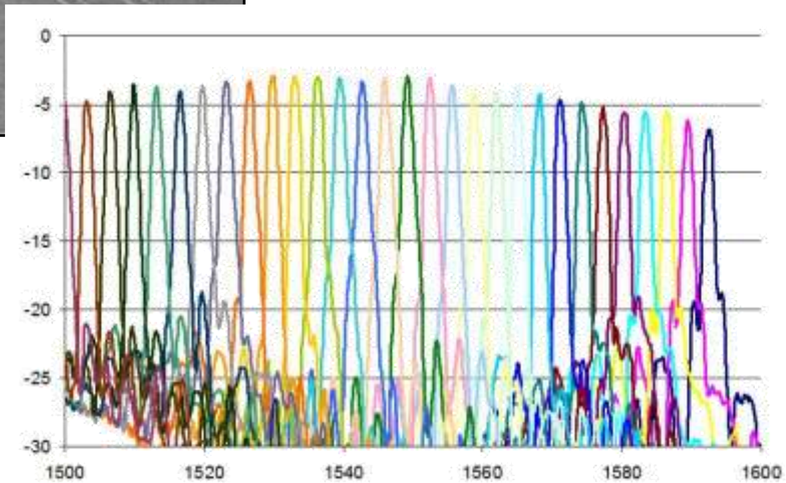
High Fresnel reflection loss at grating ?

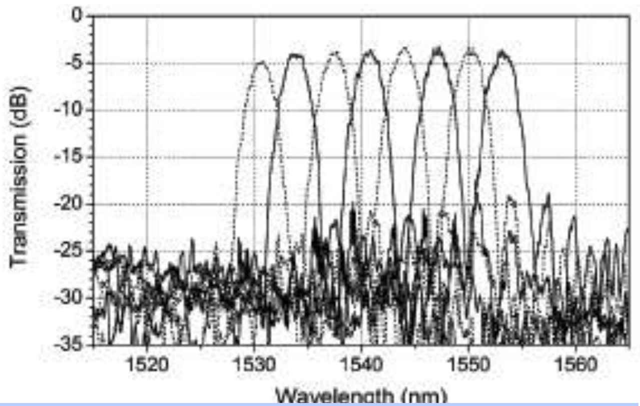
- Use metal coating
- Use DBR mirror
- Use TIR mirror







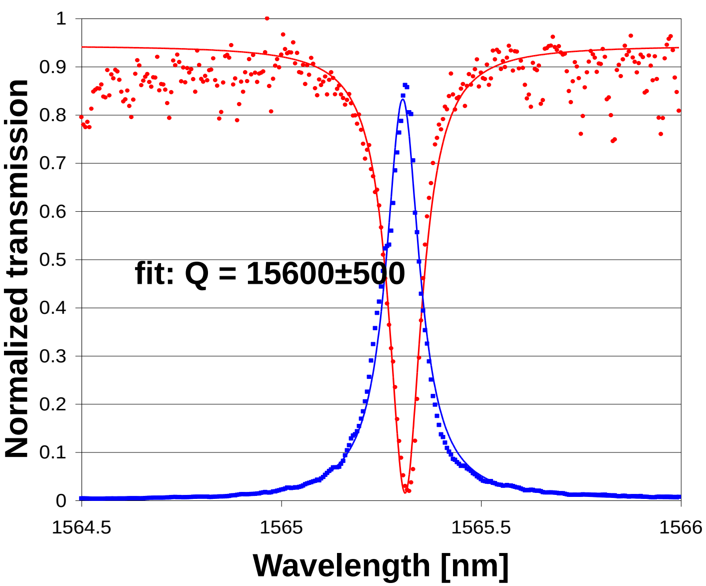




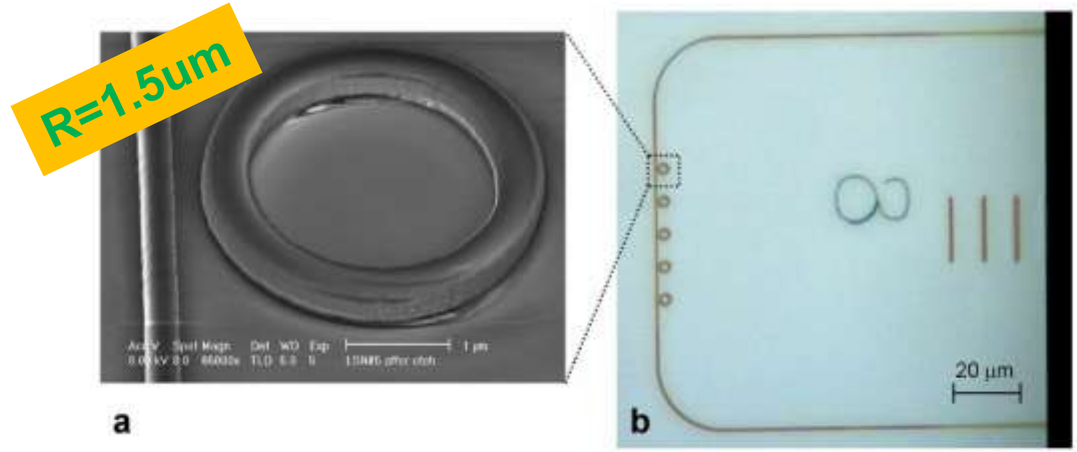
J. Brouckaert et al. PTL 20(4), p309 (2008)

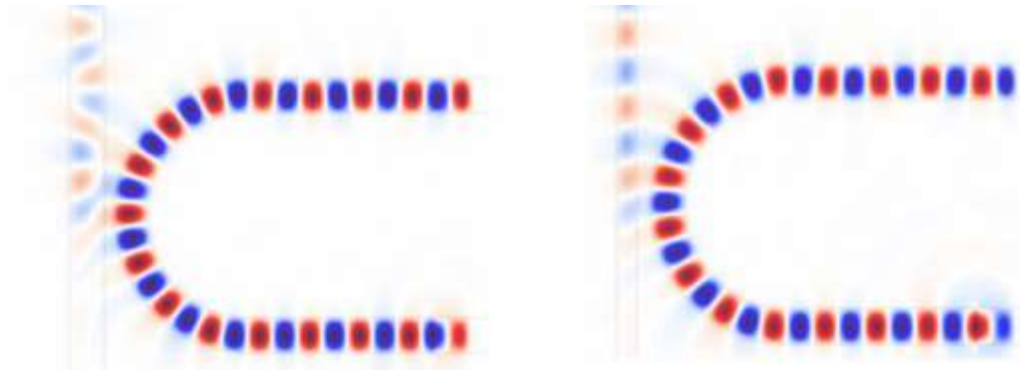
Horst e.a., PTL 21, pp 1743 (2009)
See also: Horst, OFC 2010, OWJ3 (invited)

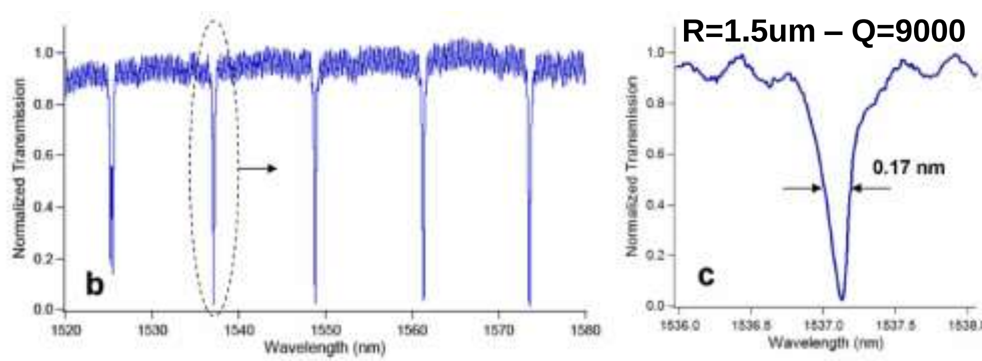
Ring resonators



Bogaerts e.a. , JSTQE 16, 33-44 (2010)

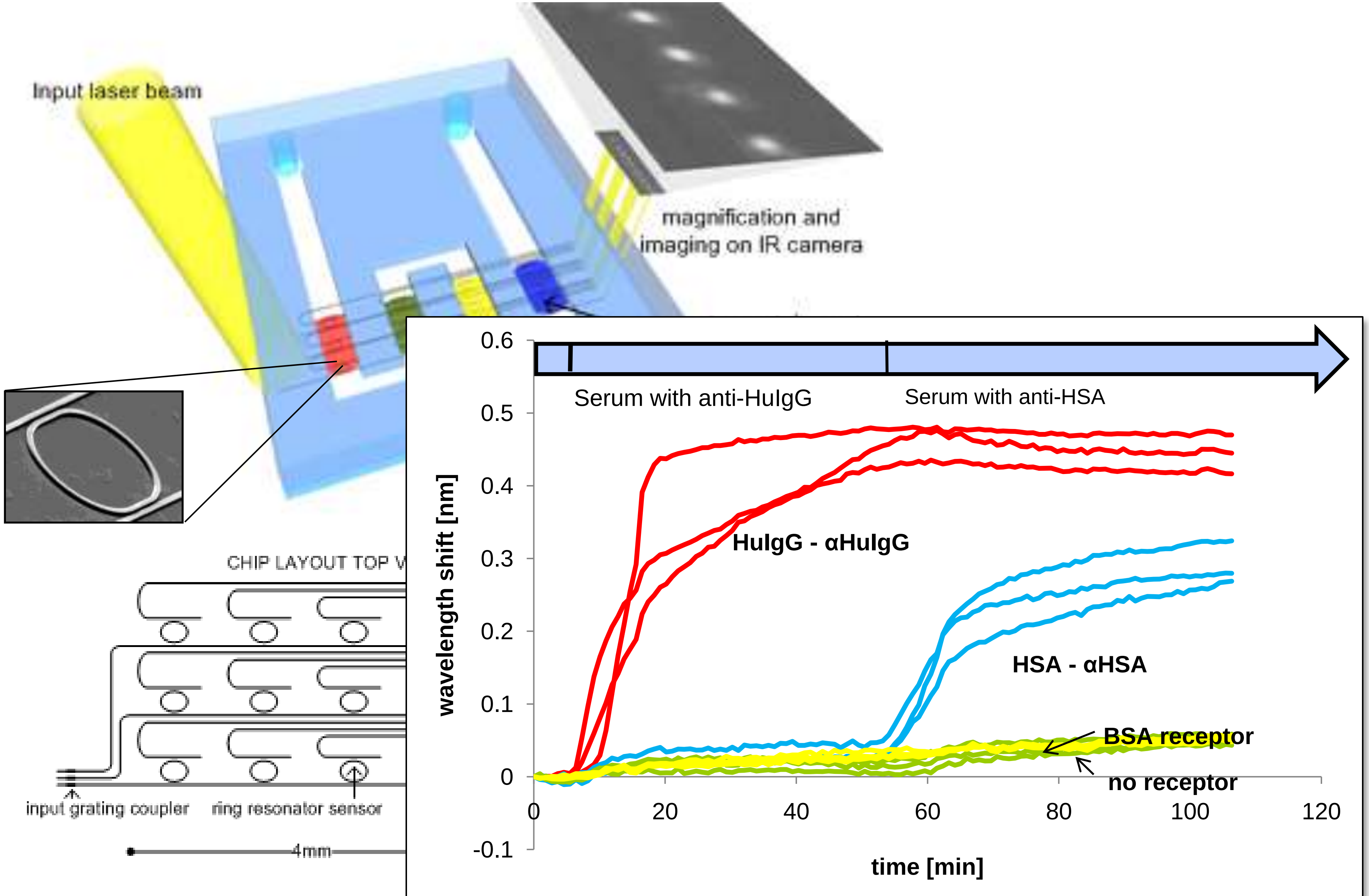






Xu e.a. , OE 16, pp 4309 (2008)

Ring resonators for sensing



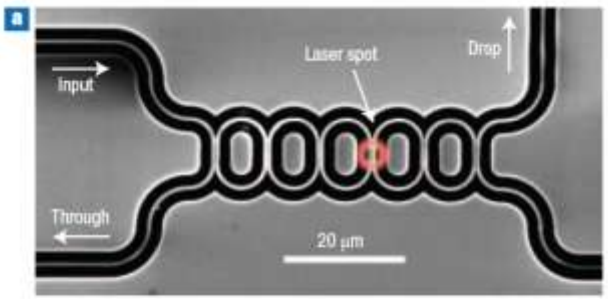
Devos e.a., IEEE Photonics Journal, 1(4), p.225-235 (2009)

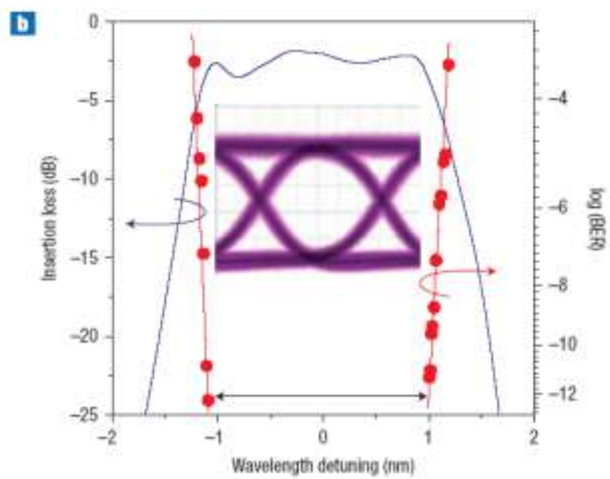
Ring resonator based devices

For applications in data- and telecom

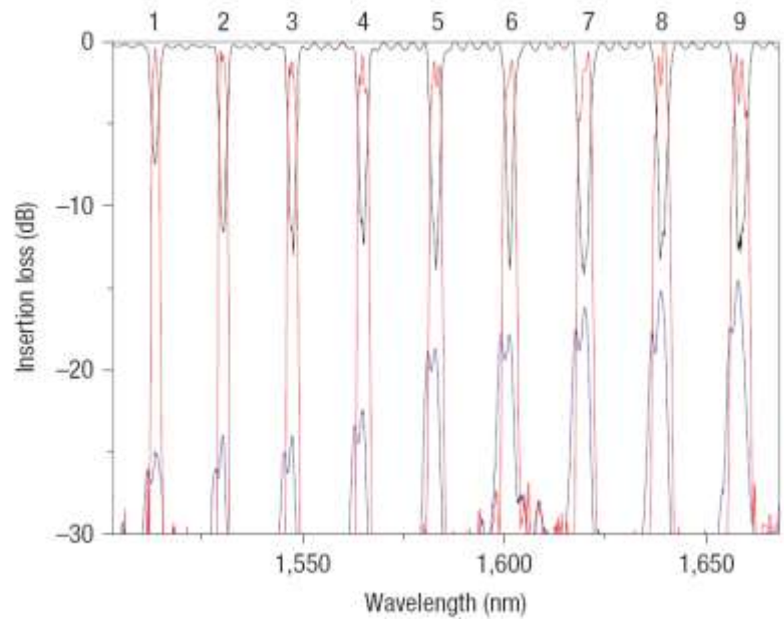
- Need **multi-ring devices** with tailored pass band

Layout and channel transfer

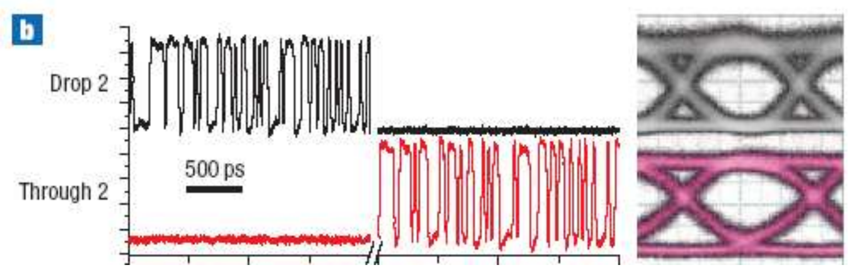




Response of 8-channel device



Switching 40Gb/s signal using probe

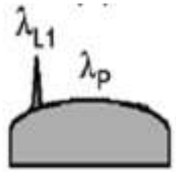


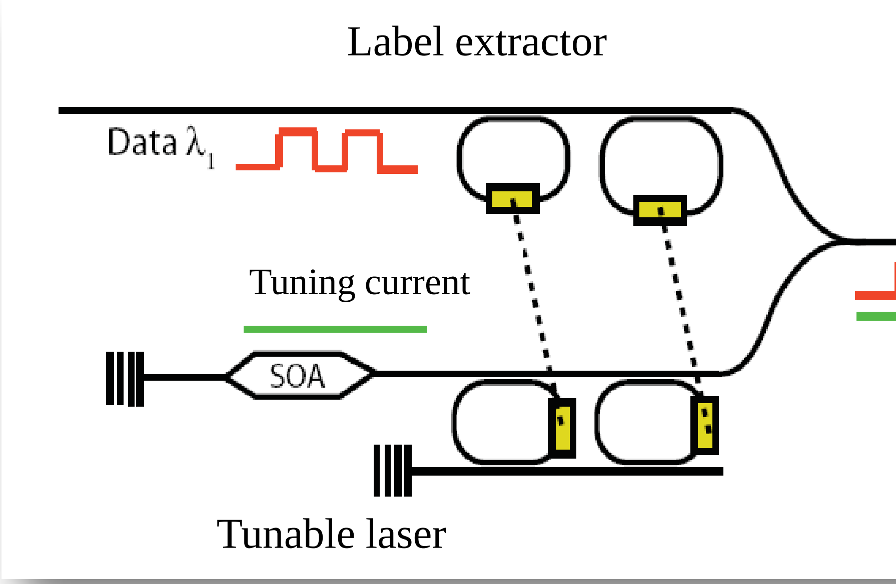
Vlasov e.a., Nat Phot 2 pp. 242 (2008)

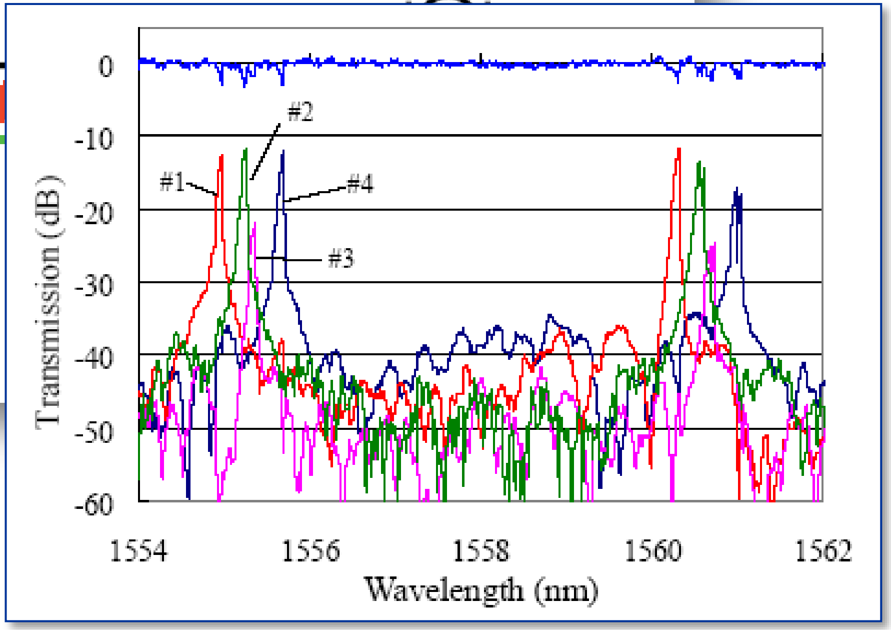
Ring resonators

Ring resonators for label extractor

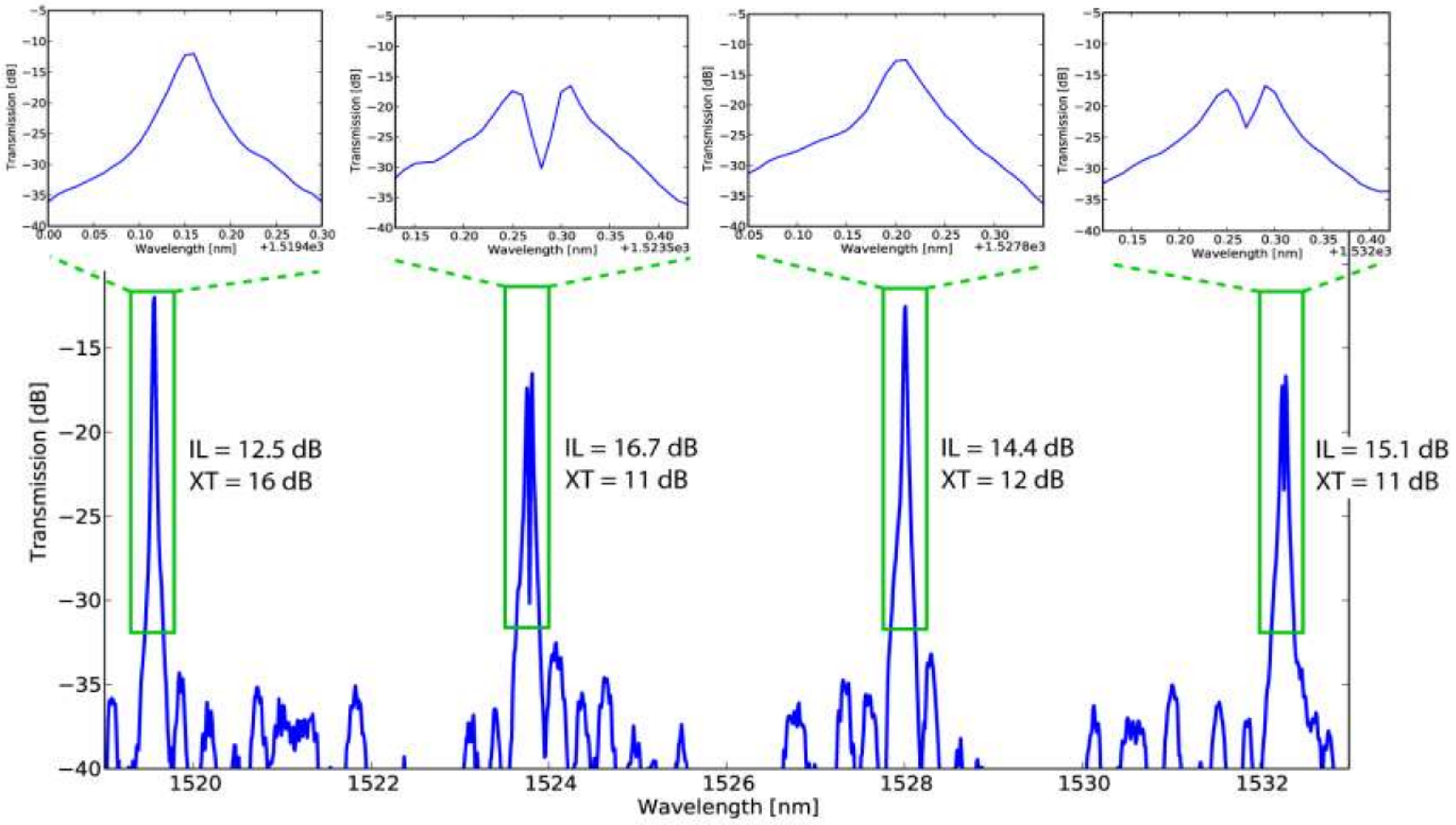
- EU-project BOOM
- Need 0.1nm bandwidth filter
- Use silicon ring resonator ??







TE-Microring meeting BOOM specs? NO



R = 20um, gap = 400nm

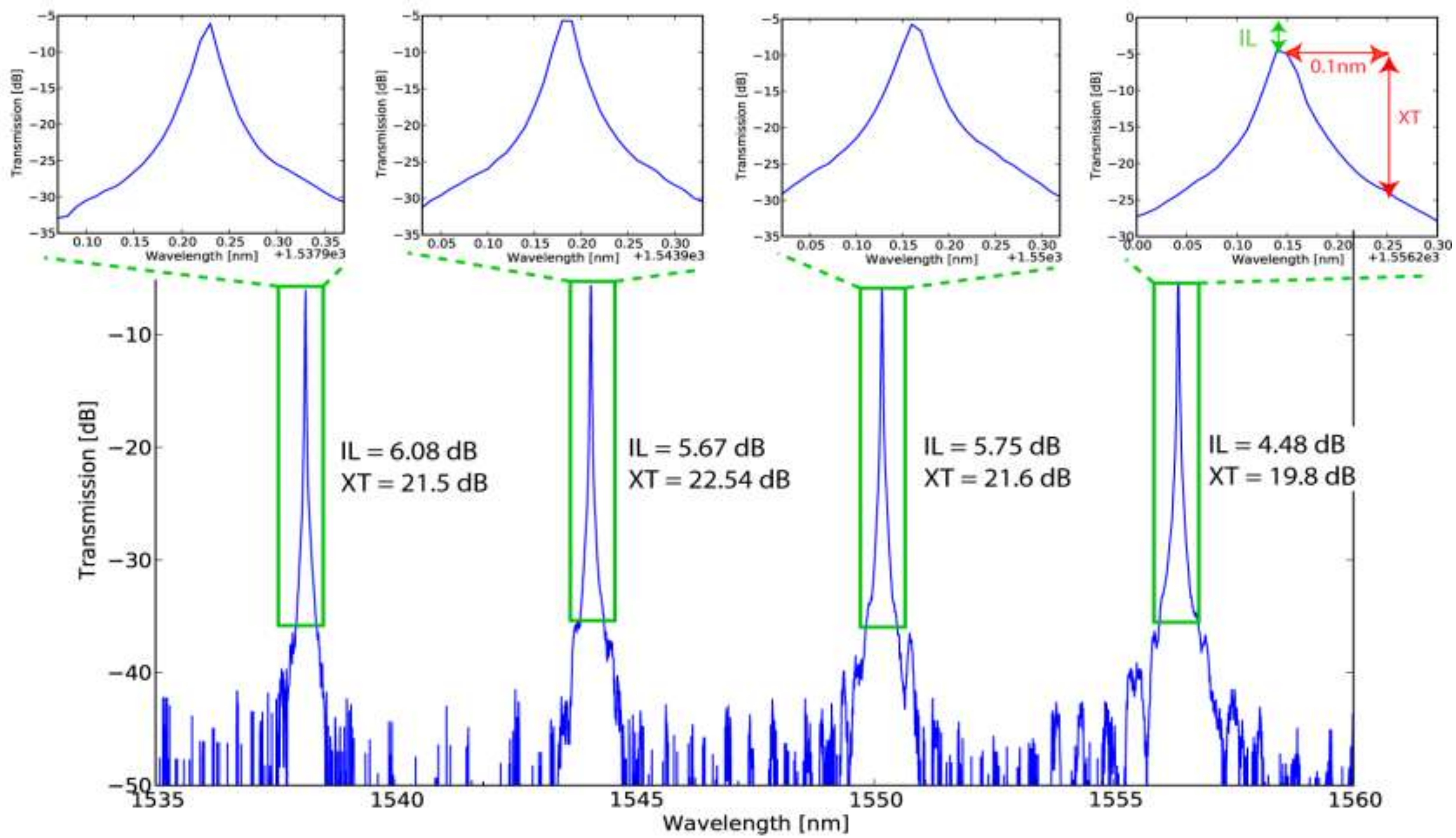
Ring resonators conclusion

TE ring resonators

- Very sensitive to random back scattering
- Behaviour very unpredictable
- High losses

TM ring resonators ?

TM-Microring meeting BOOM specs? YES !



R = 20um, gap = 1um

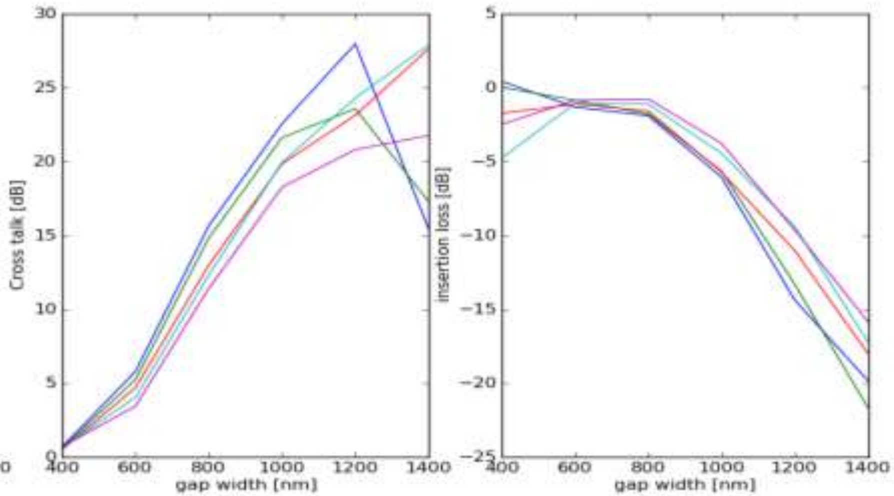
Ring resonators conclusion

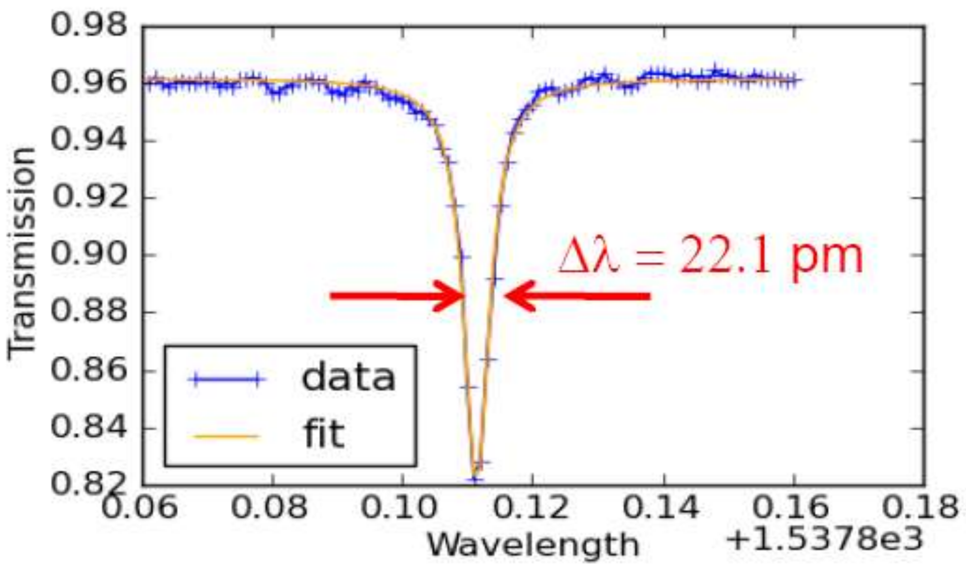
TE ring resonators

- Very sensitive to random back scattering
- Behaviour very unpredictable
- High losses

TM ring resonators

- Lower confinement at side walls
- Lower loss, lower back scattering
- Record high Q values demonstrated (Q_i=340.000)

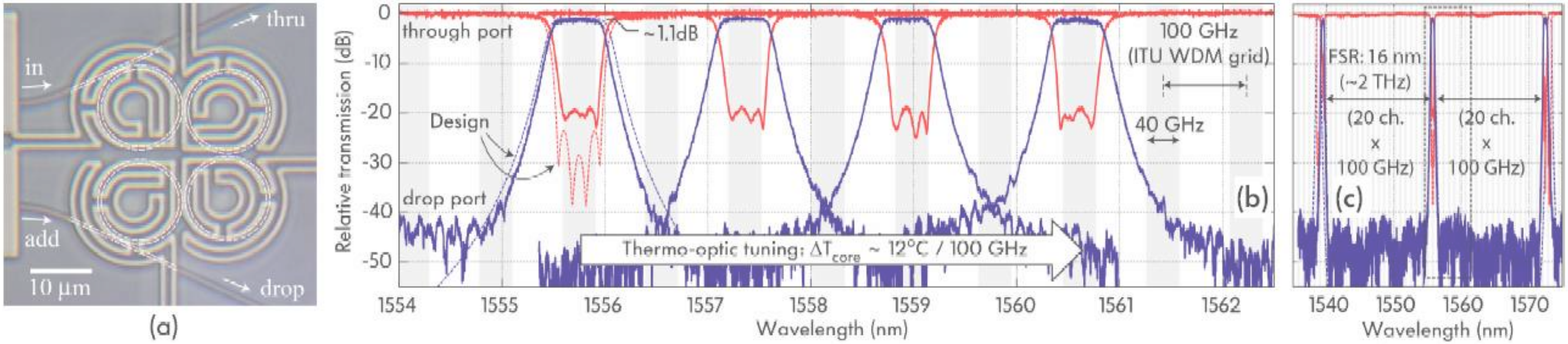




DeHeyn e.a. , submitted to OFC 2011

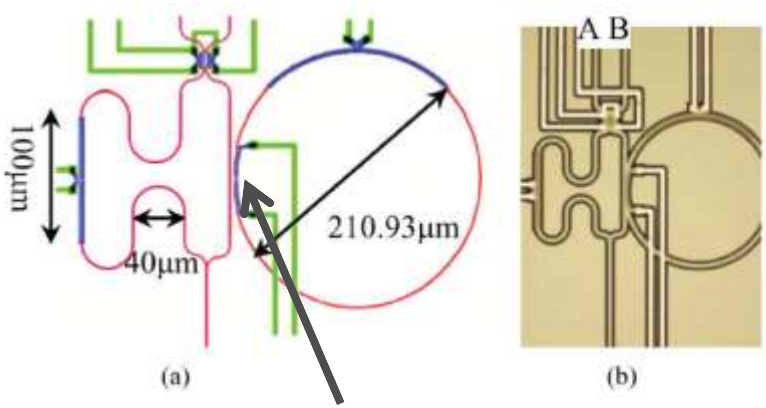
Higher order devices

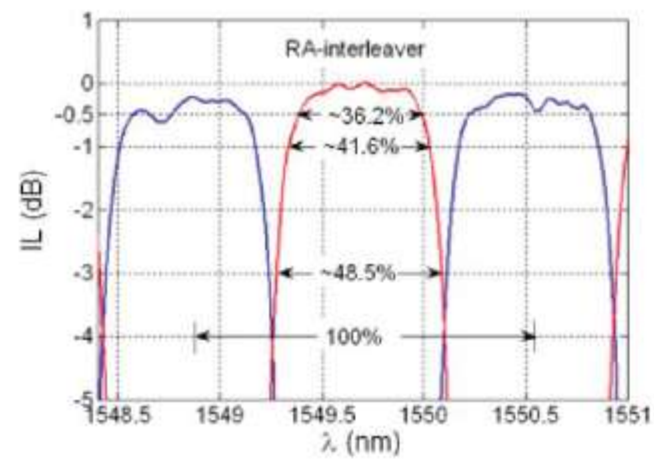
Hitless add-drop filter



Popovic e.a. , OFC2008, paper OTuF4

Interleaver





Assymmetric heating of directional coupler for optimizing coupling ratio

Song e.a. , IEEE PTL 20, pp 2165 (2008)

Thermo-optic effect

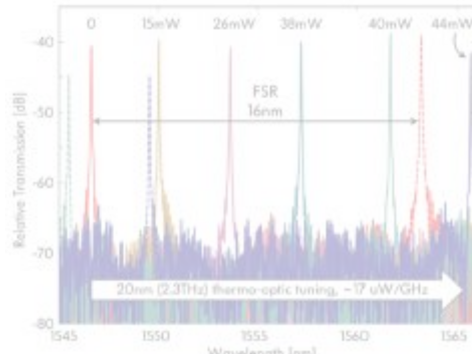
Silicon strongly temperature dependent

- Roughly: 80pm/K

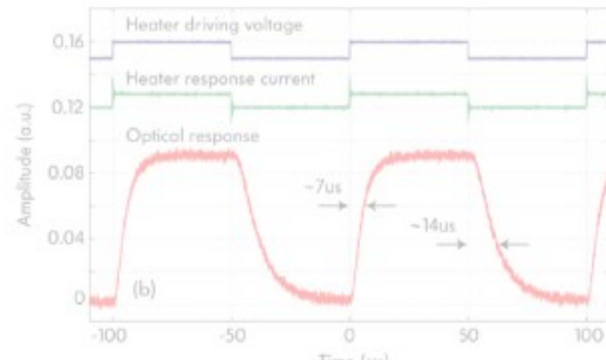
P. Dumon, PhD Thesis UGent (2007)
(http://photonics.intec.ugent.be)

Opportunity for tuning & trimming devices

Gnan e.a. , Photonics in Switching 2007, paper TuB3.3

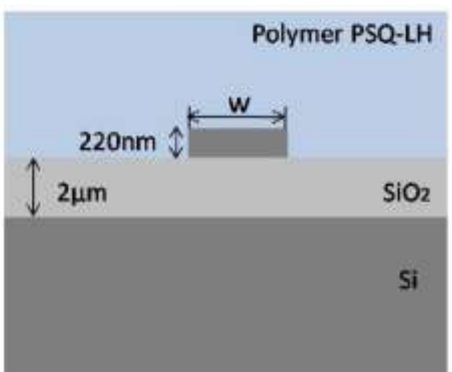


17uW/GHz

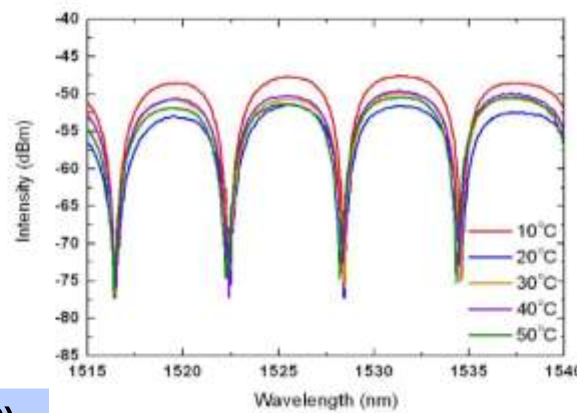


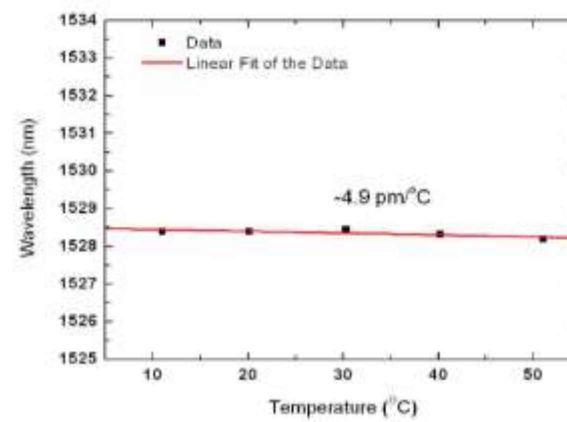
~10us switching

Problem for fixed filters: need for athermal devices



Teng e.a. , OE 17 p.14627-14633 (2009)



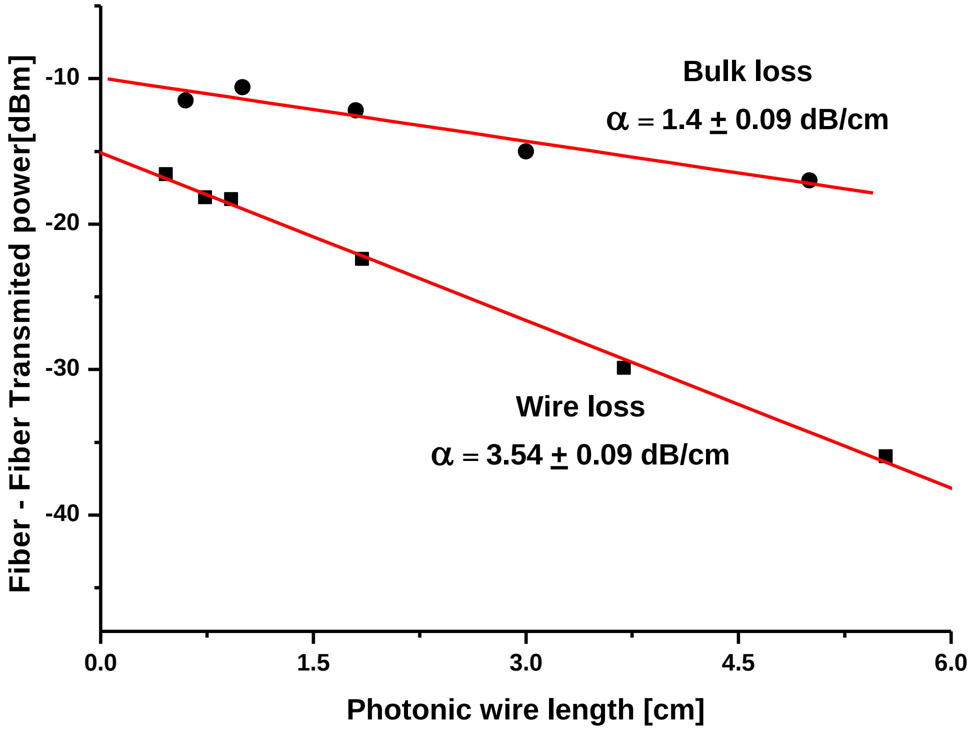


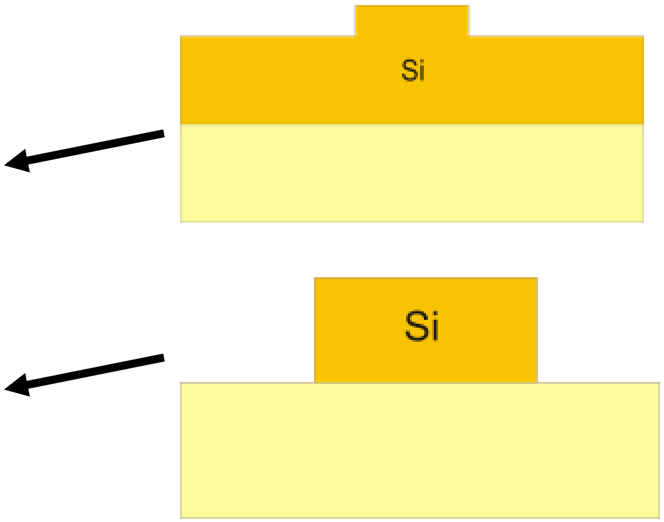
Amorphous silicon wires

Low-temperature PECVD a-Si:H deposition

Low material losses

- deep-etch wire (480nm width): 3.54dB/cm
- shallow rib waveguide: 1.4dB/cm

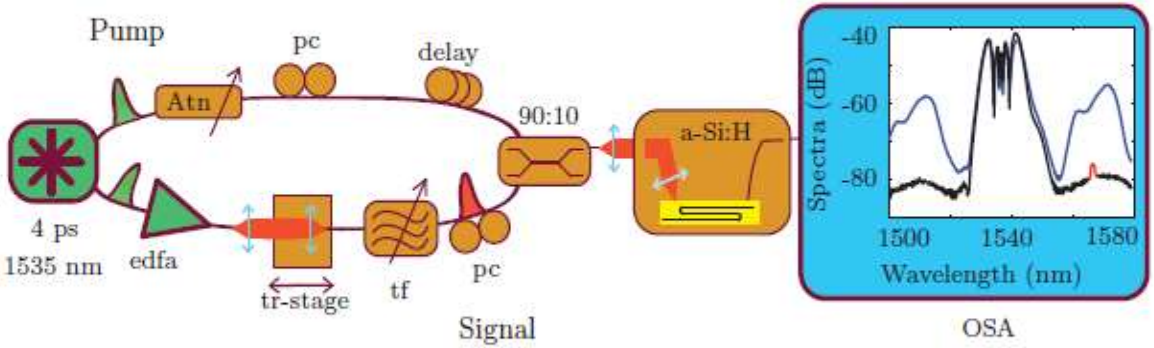


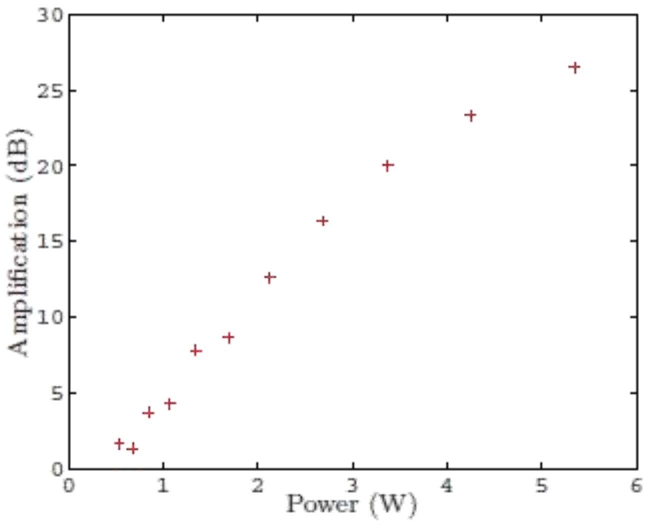


Amorphous silicon wires

Amorphous silicon

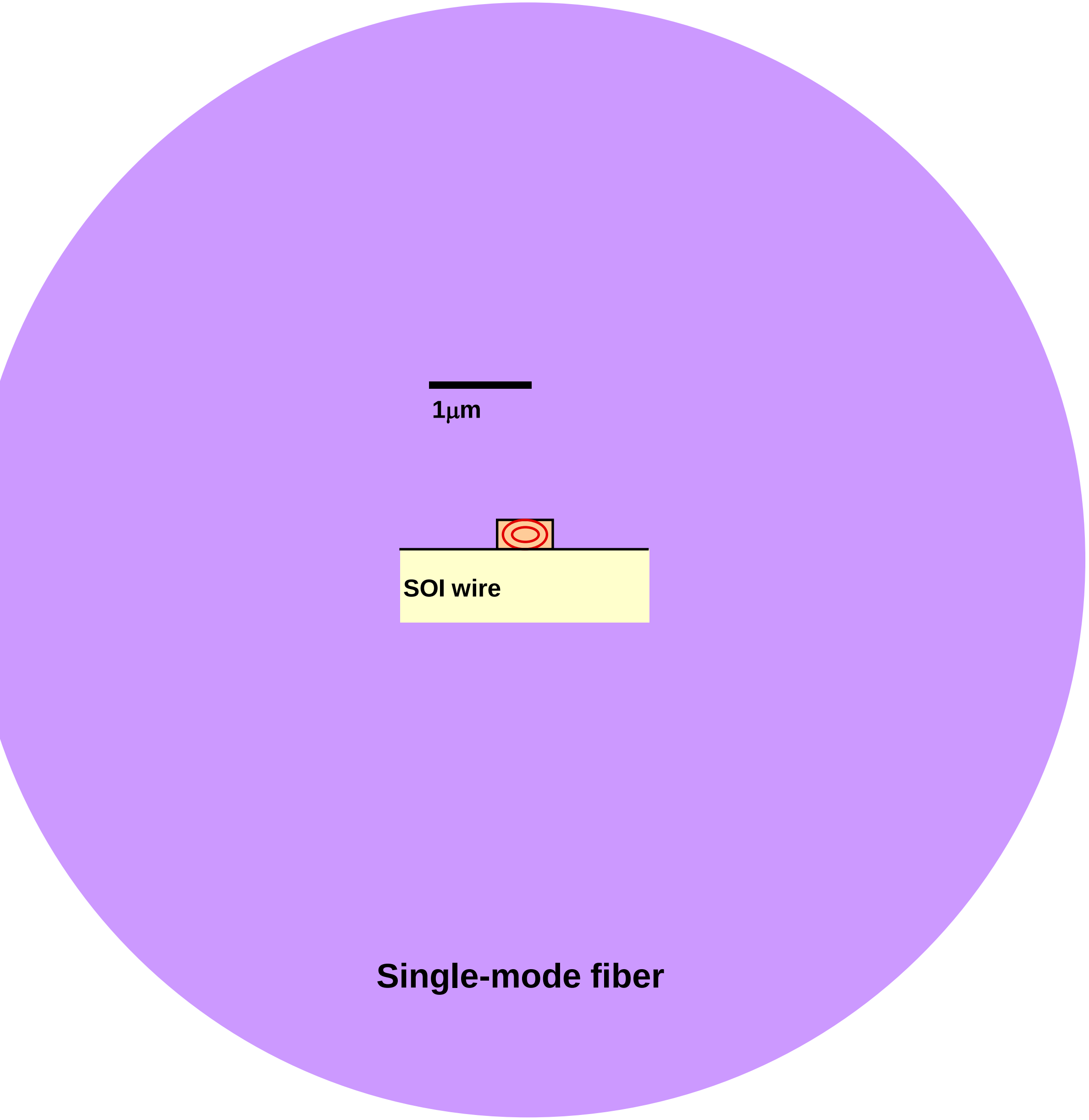
- **Shows improved non-linear performance**
  - Lower non-linear absorption
  - Higher non-linear n_2
- **Demonstrated 26dB parametric gain (on-chip)**





Results presented at IEEE Photonics Society annual meeting (Denver, 2010)

Fiber chip coupling



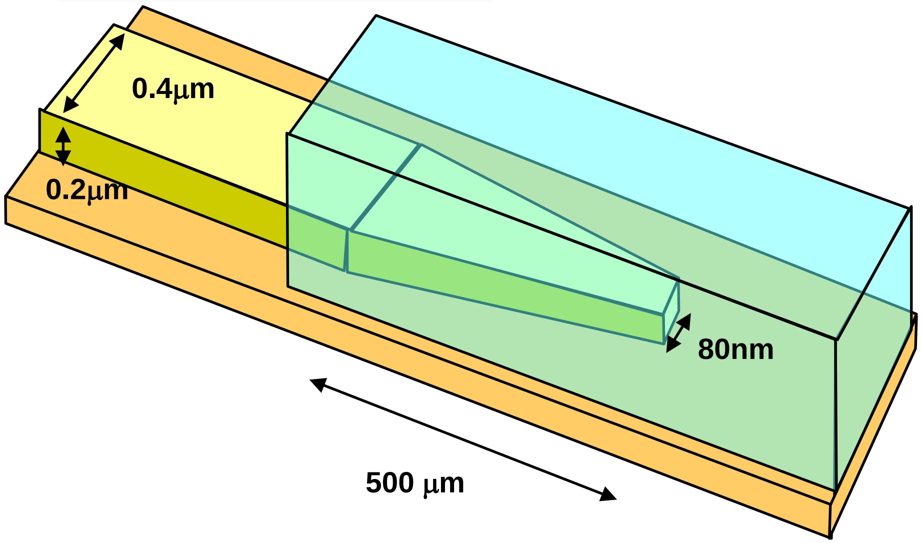
We would like

- Low loss
- Broadband
- High coupling tolerance
- No facet reflections
- Waferscale testability
- Easy to fabricate
- A solution for the polarization problem

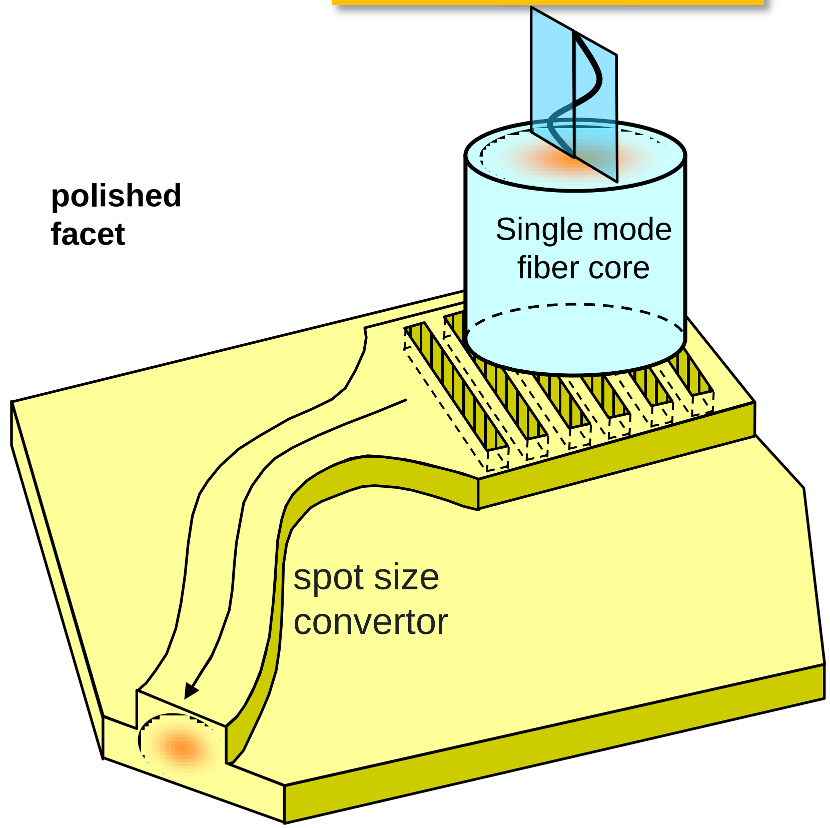
Two solutions

Two widely used solutions

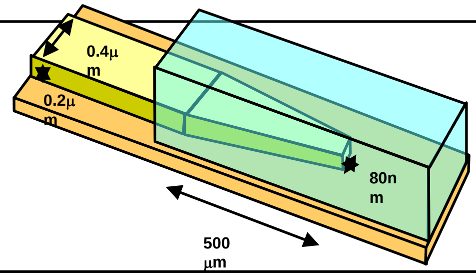
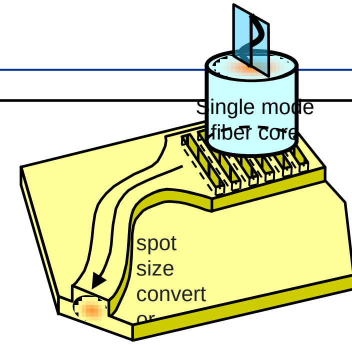
Inverted taper



Grating coupler



Comparison

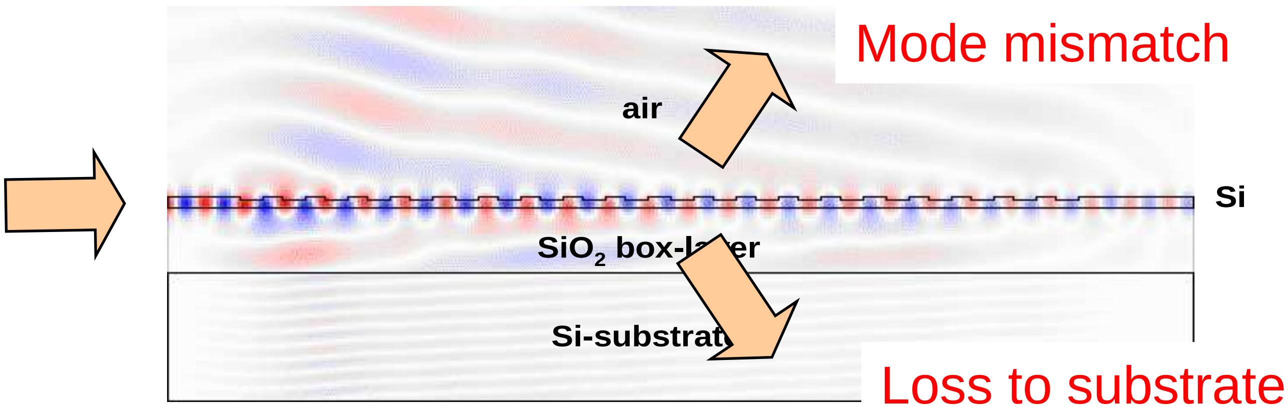
		
Loss (best)	<1dB	<1dB
Loss (in real live)	3dB-7dB	3dB-7dB
Broadband	> 100nm	35nm (1dB)
Misalignment tolerance	1um (1dB)	2.5um (1dB)
Facet reflections	Low	-20dB
Waferscale testing	No	Yes
Fabrication	Additional layer Facet critical	Easy to difficult
Robustness	Facet preparation	Etch depth control
Polarization	Need additional	Build in polarization

High performance applications

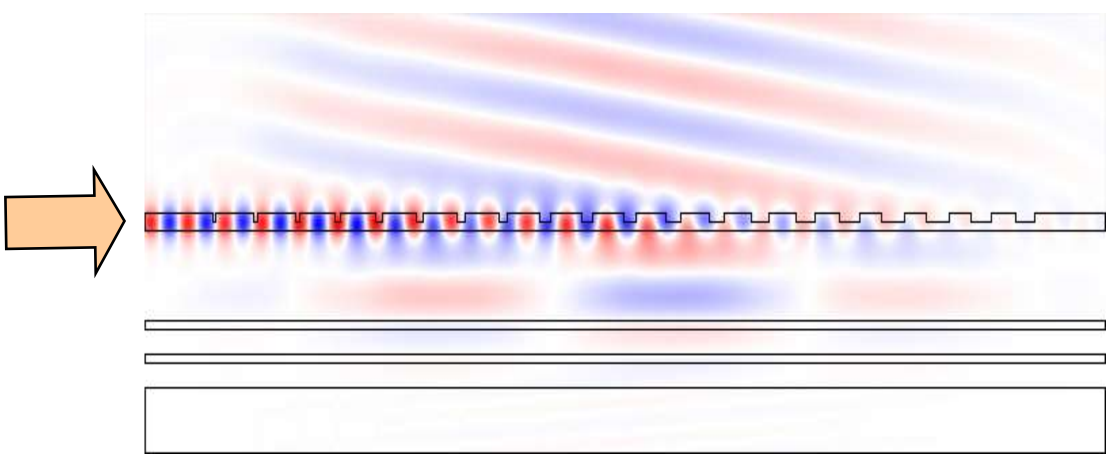
Low cost applications + Testing

Increase effieciency standard coupler ?

Standard coupler (33%)



Improvement: add bottom mirror + apodize

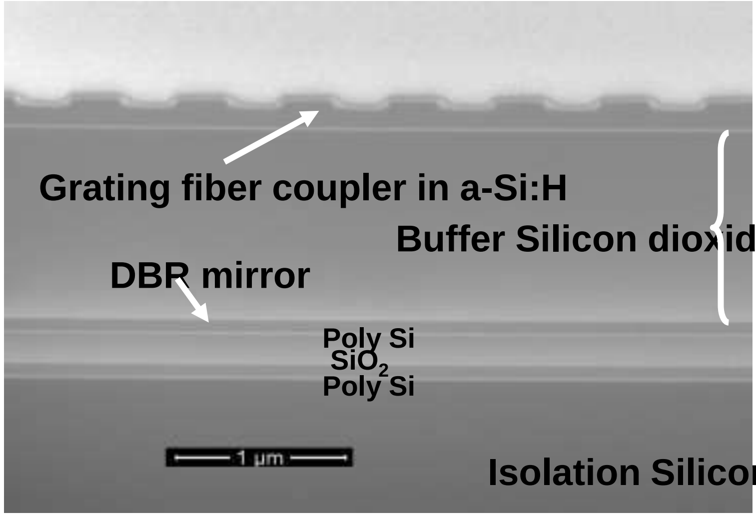


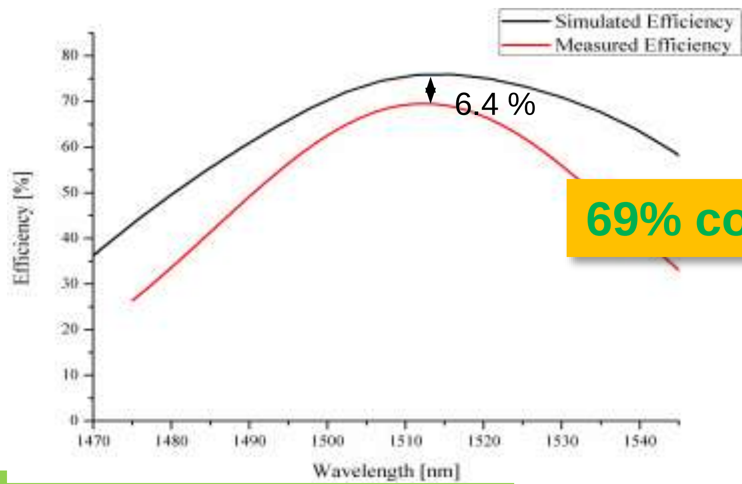
90% simulated !

Gratings with bottom mirror

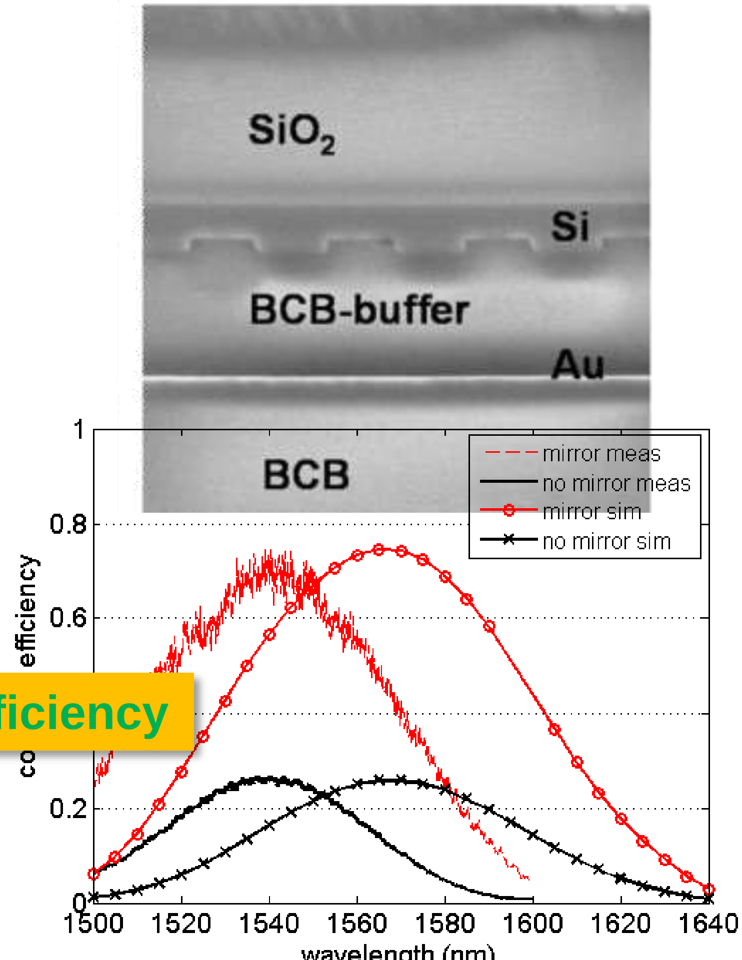
DBR bottom mirror
- Poly silicon DBR mirror
- a-Si waveguides

Gold bottom mirror
- Use waferbonding
- c-Si waveguides





Selvaraja et al. CLEO/IQEC 2009

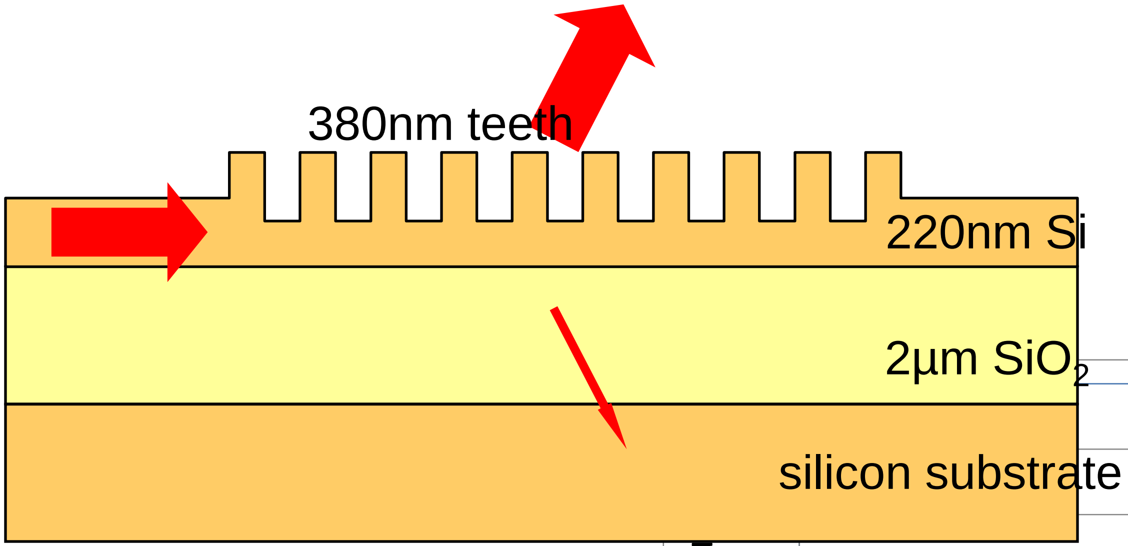


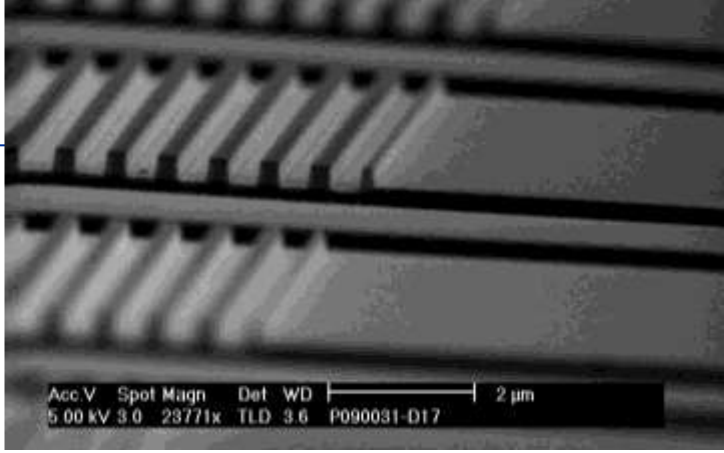
69% coupling efficiency

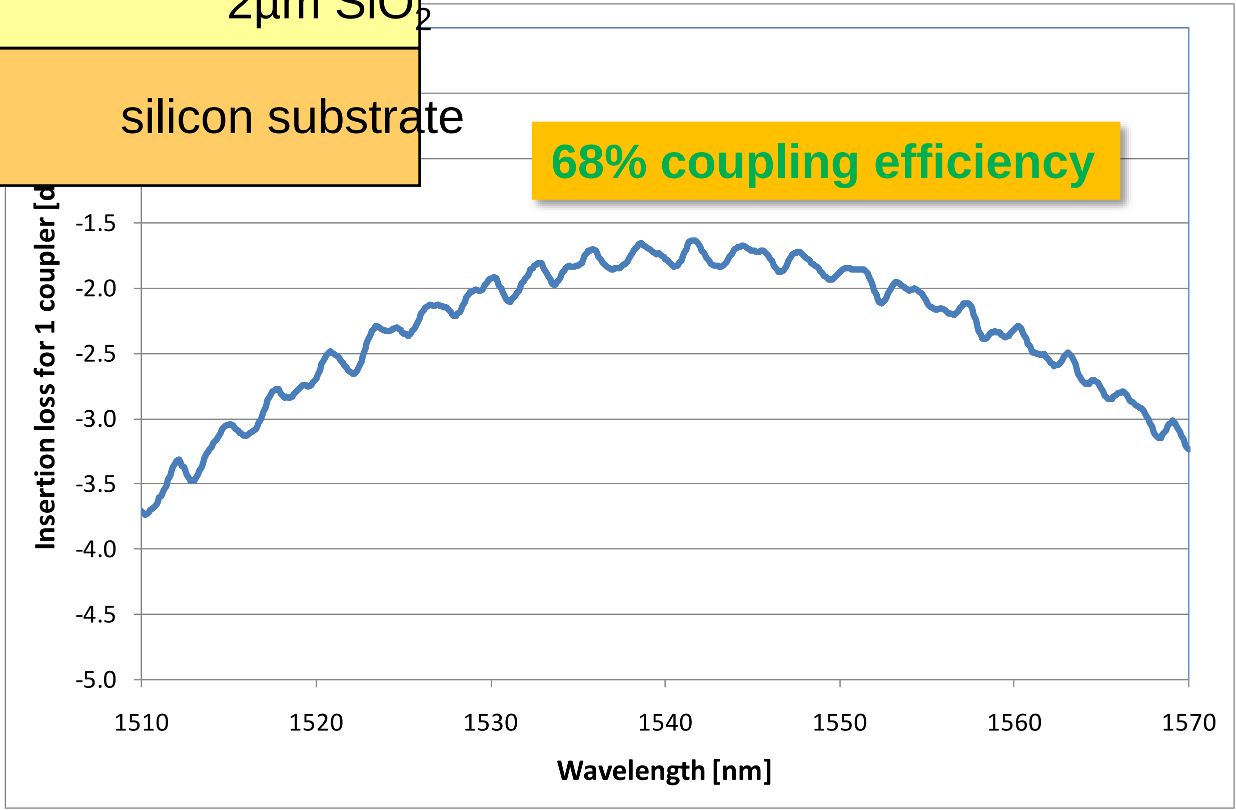
Van Laere et al., JLT 25(1), p.151 (2007)

Overlay gratings

Break top-bottom symmetry

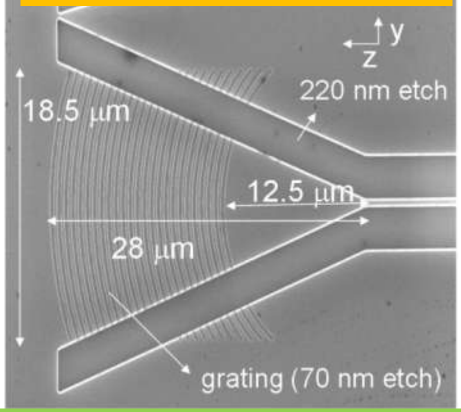






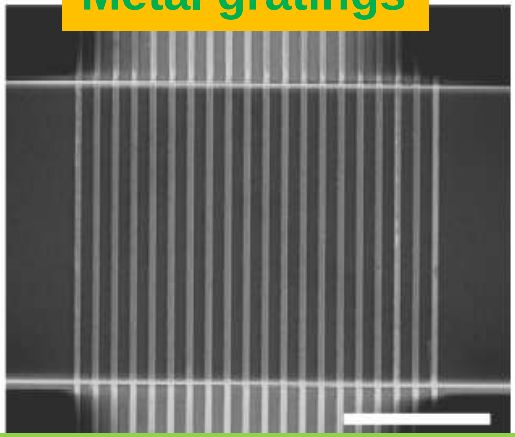
Grating zoo

Focusing grating



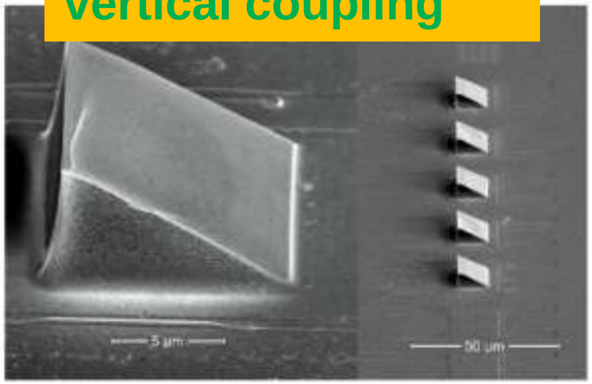
F. Van Laere, PTL 19, p. 1919 (2006)

Metal gratings



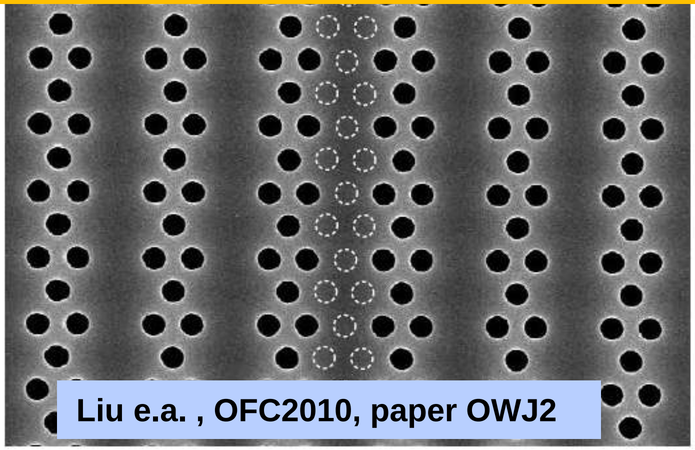
Scheerlinck, APL 92 p.031104 (2008)

Polymer wedge for vertical coupling



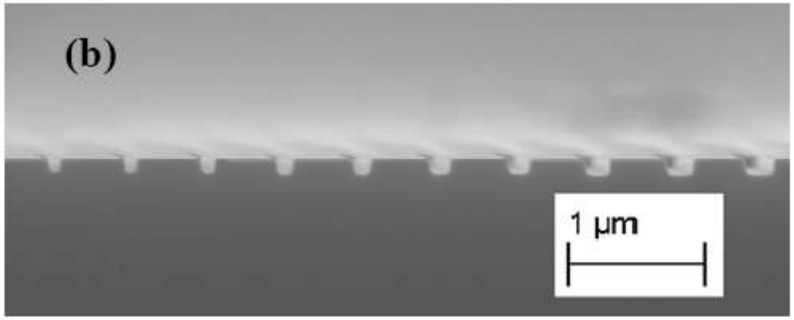
Schrauwen e.a. Phot. West, 7218, , p.72180B (2009)

Photonic crystal grating for low reflection deep etch



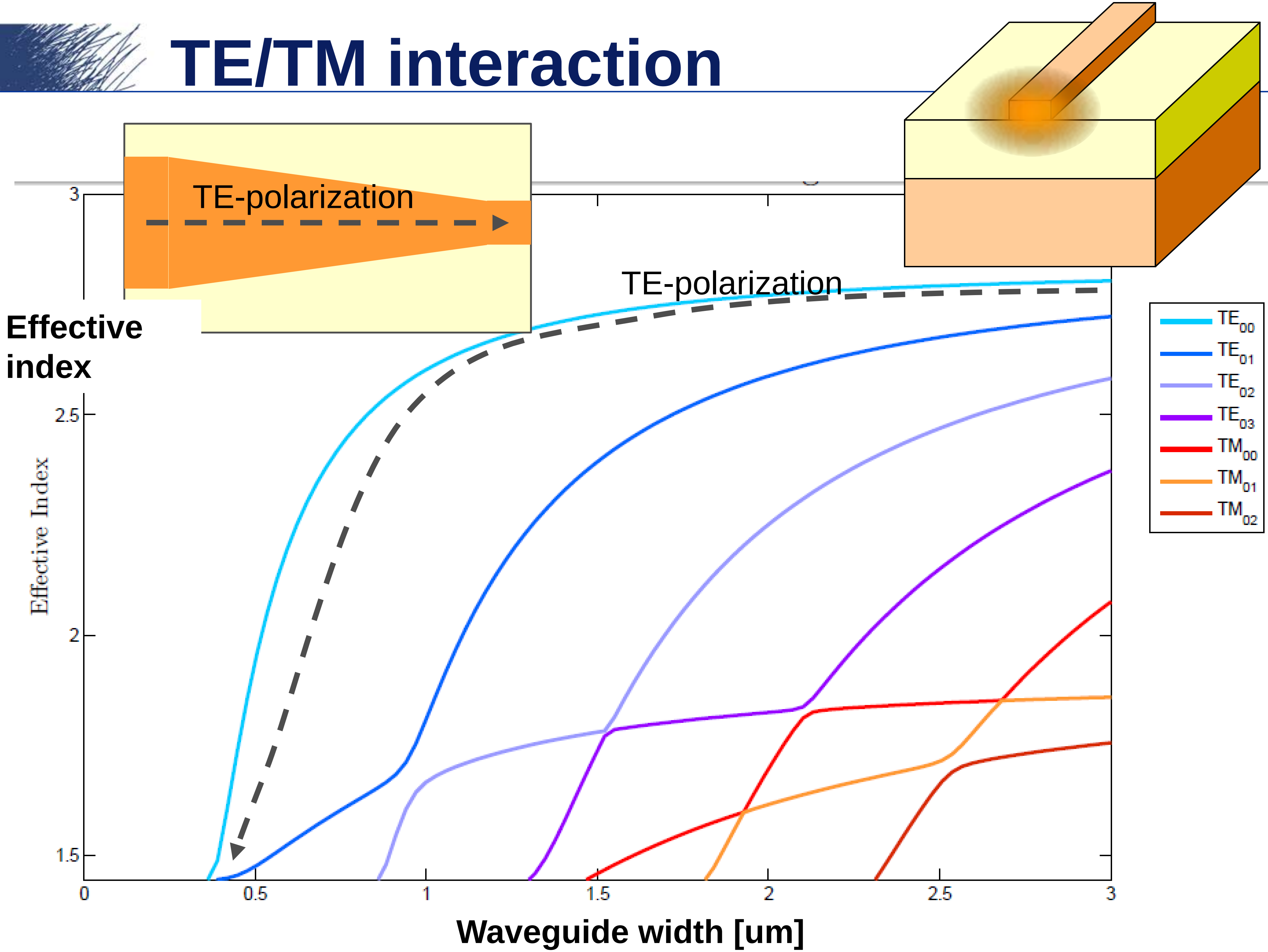
Liu e.a. , OFC2010, paper OWJ2

Apodized grating

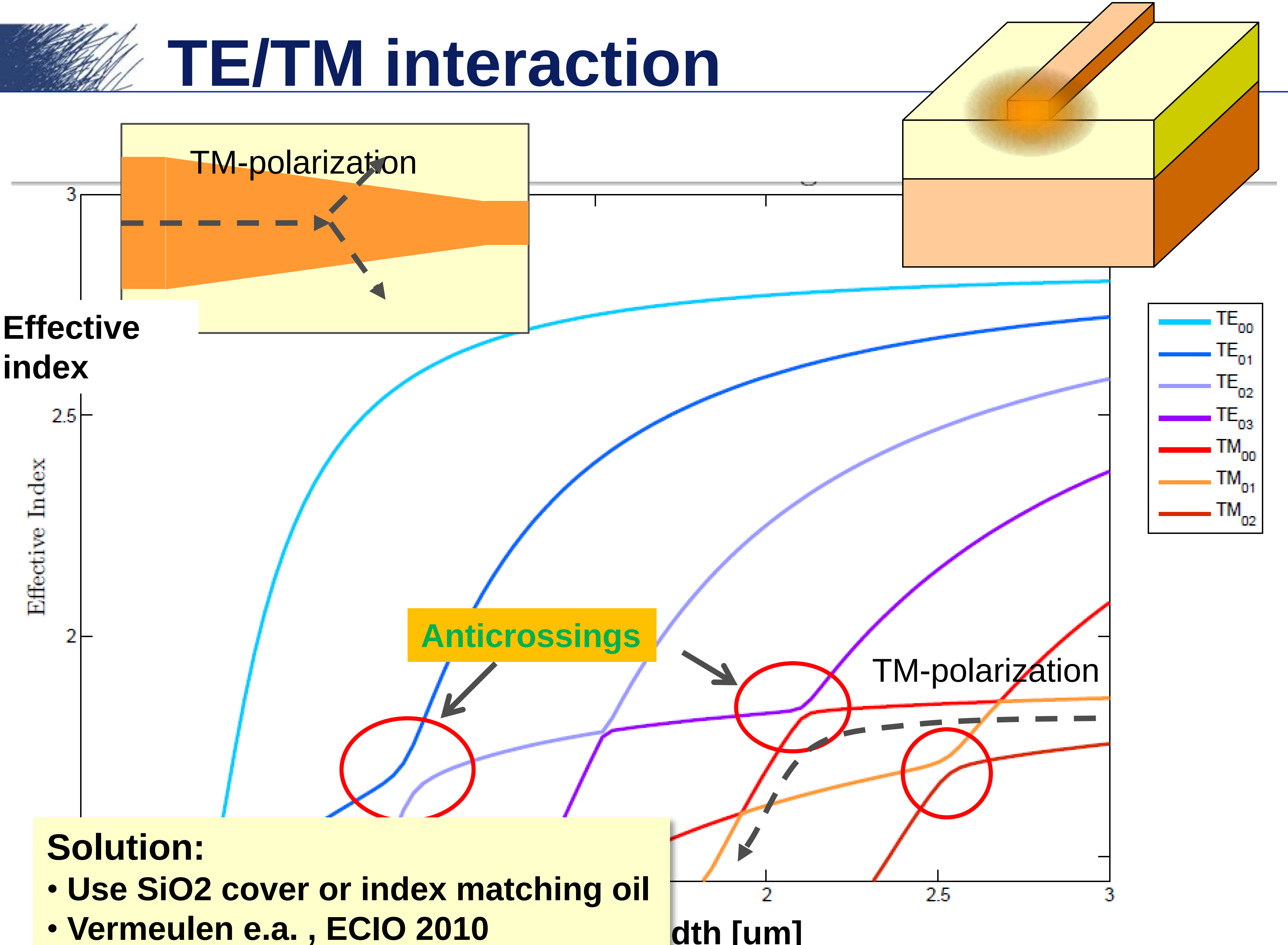


Tang e.a. , OFC2010, paper OWJ6

TE/TM interaction



TE/TM interaction

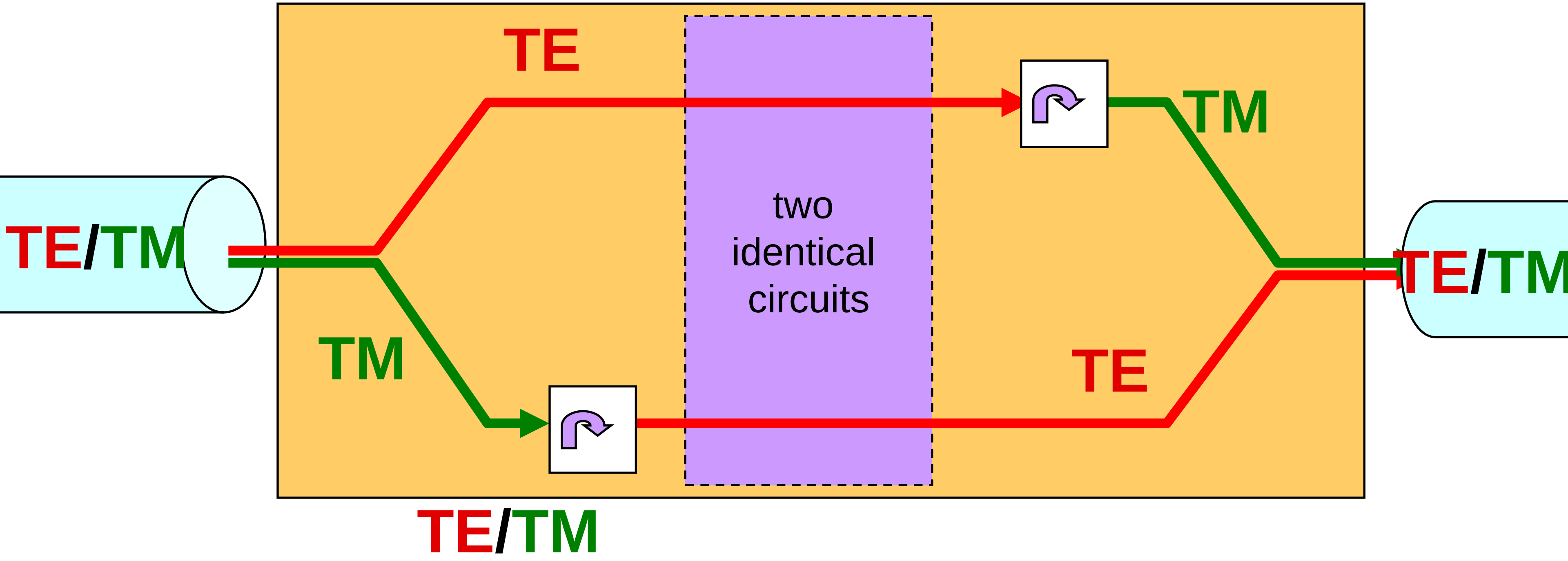


Solution:
- **Use SiO2 cover or index matching oil**
- **Vermeulen e.a. , ECIO 2010**

Polarization diversity

Process both polarizations separately

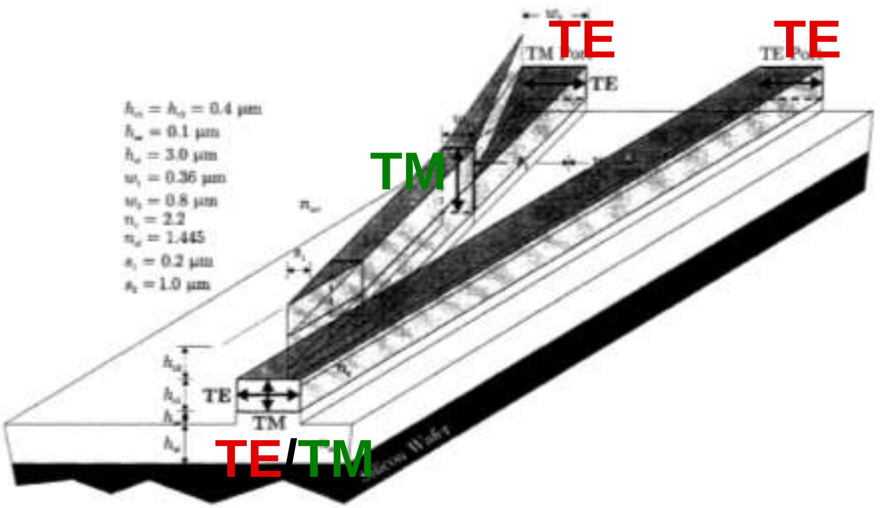
- split polarizations
- convert to the same polarization on the chip
- combine polarization back into the fiber



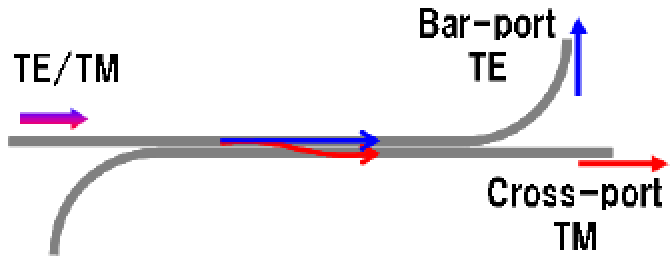
Polarization diversity

Polarization diversity with inverted taper

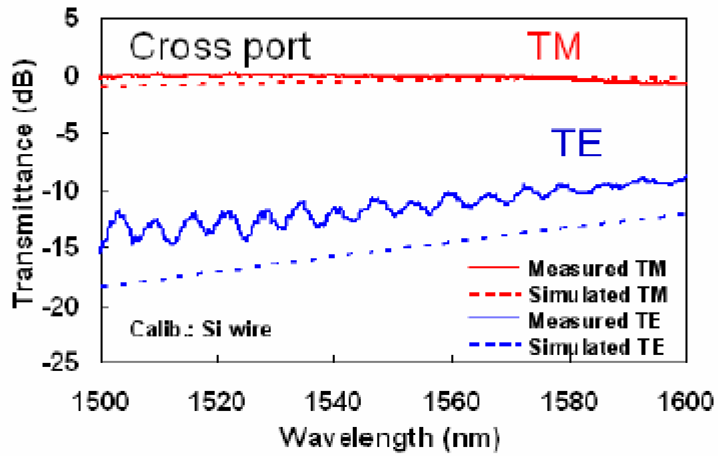
- Need on-chip polarization splitter + rotator



Watts et al, OL 30(9), p.937 (2005)



Coupling length TM << TE

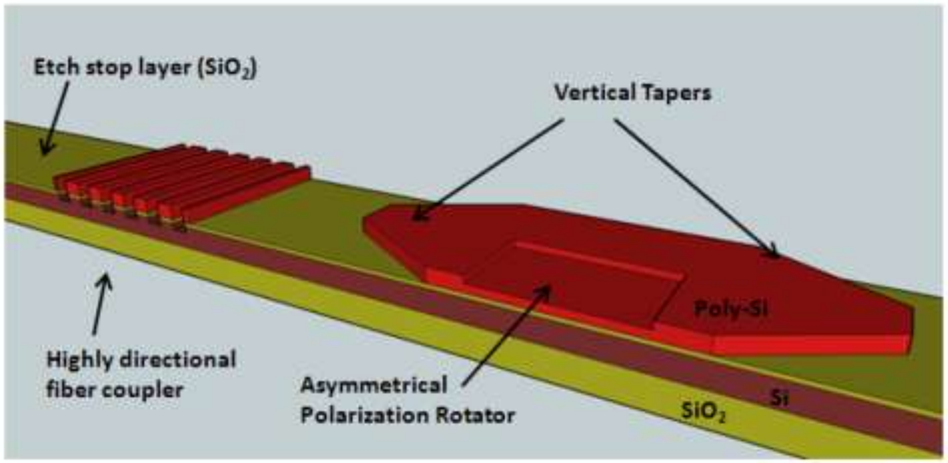


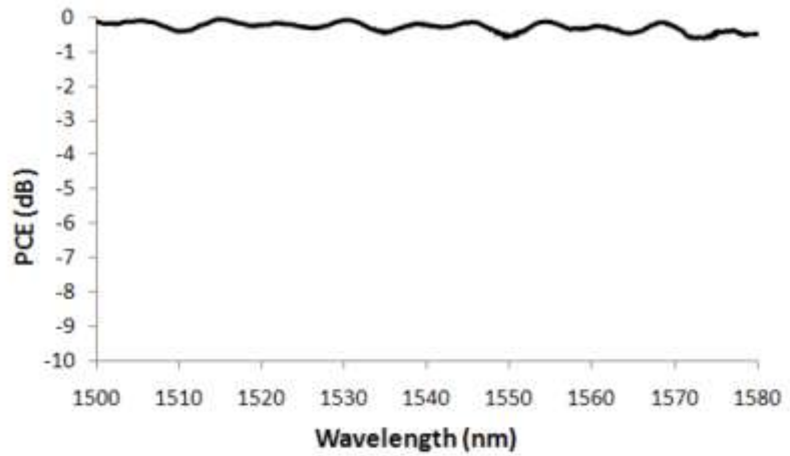
Fukuda e.a., OE 14(25), p. 12401 (2006)

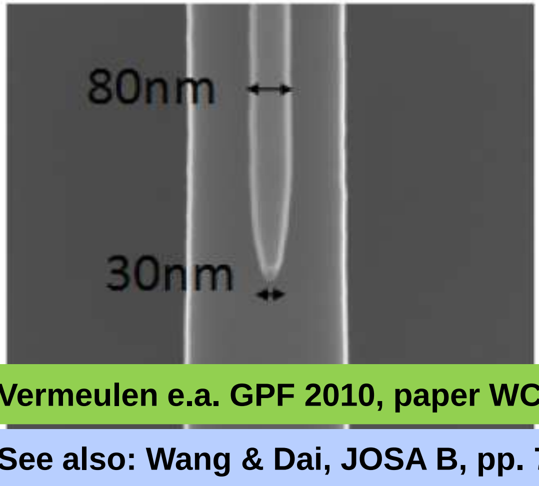
Polarization diversity

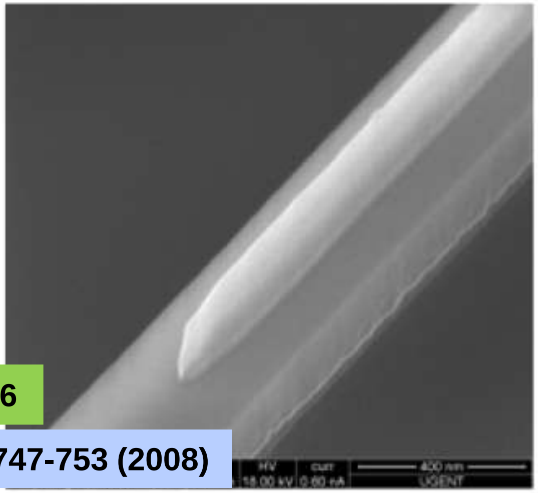
Polarization diversity with inverted taper

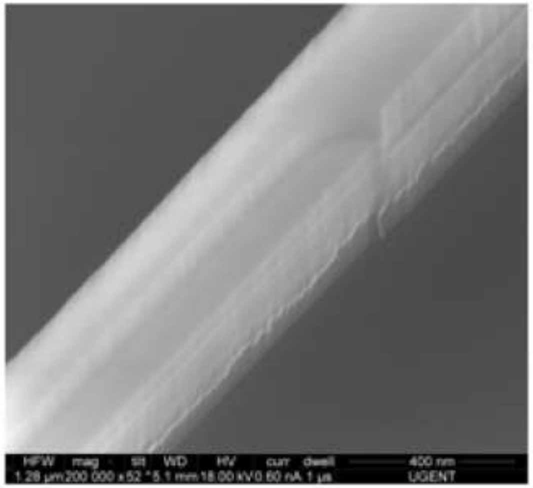
- Need on-chip polarization splitter + rotator









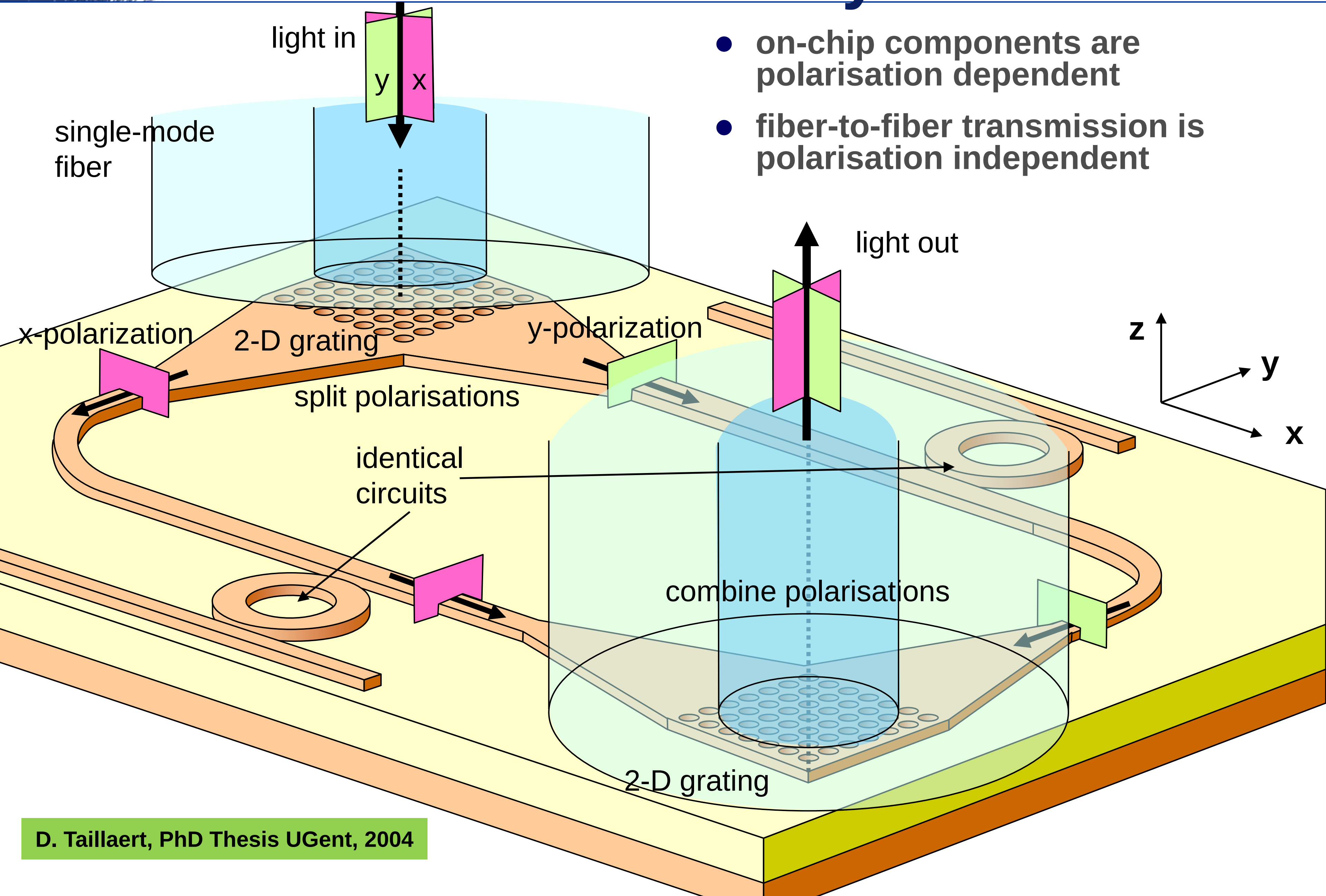


Vermeulen e.a. GPF 2010, paper WC6

See also: Wang & Dai, JOSA B, pp. 747-753 (2008)

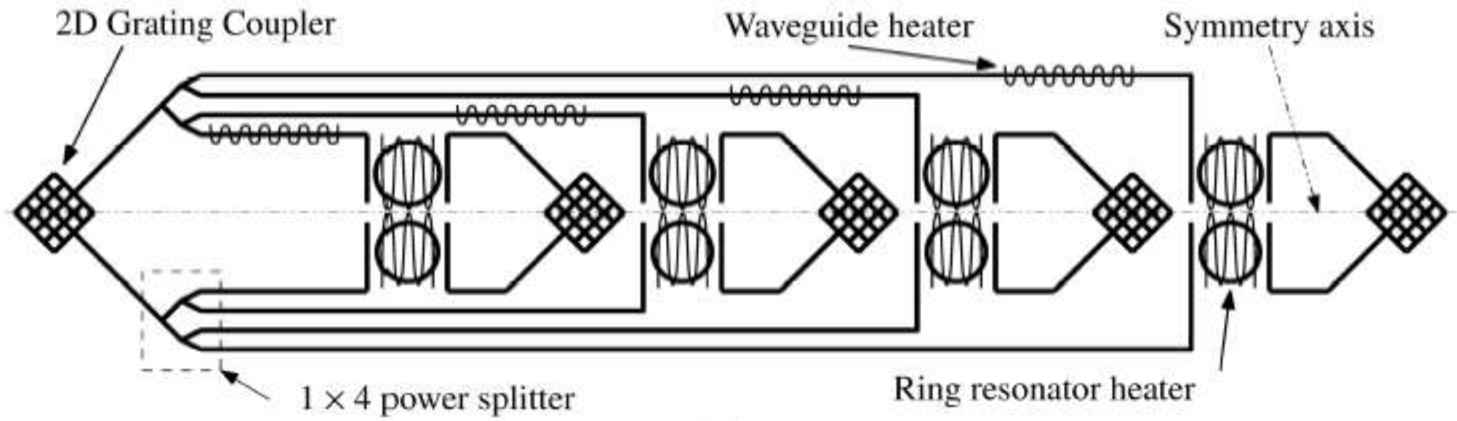
Polarisation Diversity Circuit

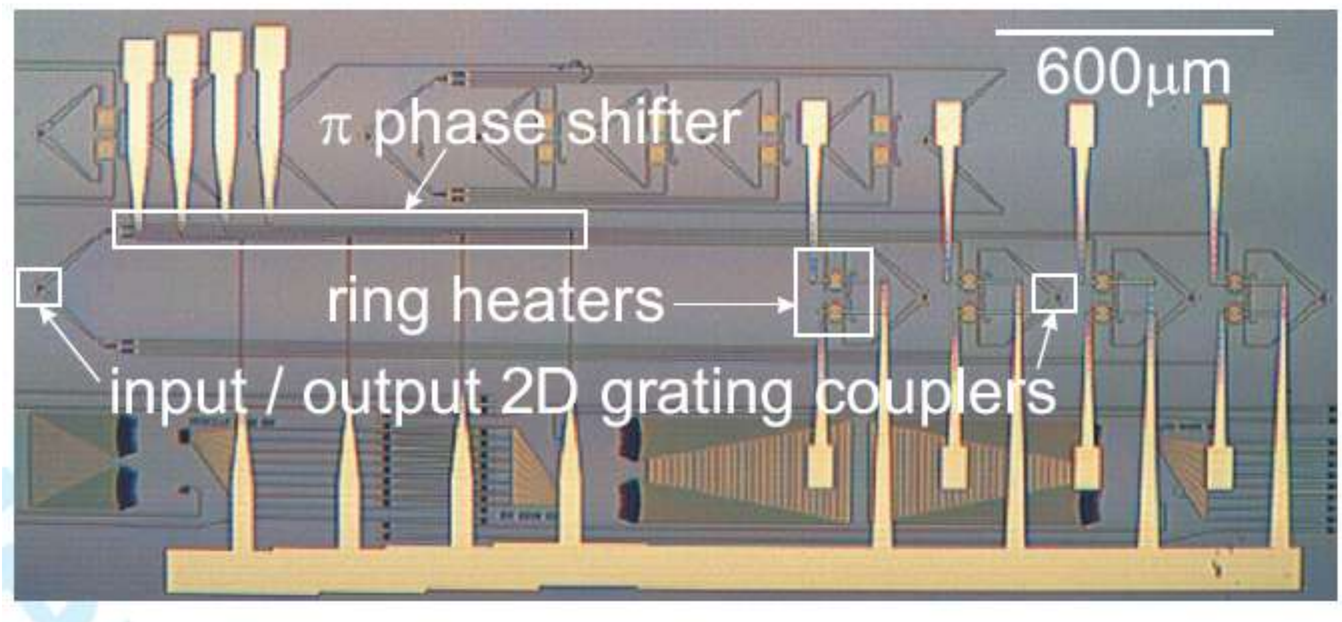
- on-chip components are polarisation dependent
- fiber-to-fiber transmission is polarisation independent



D. Taillaert, PhD Thesis UGent, 2004

Polarization diversity circuit





See Halir e.a. , OFC 2010, paper OWJ1

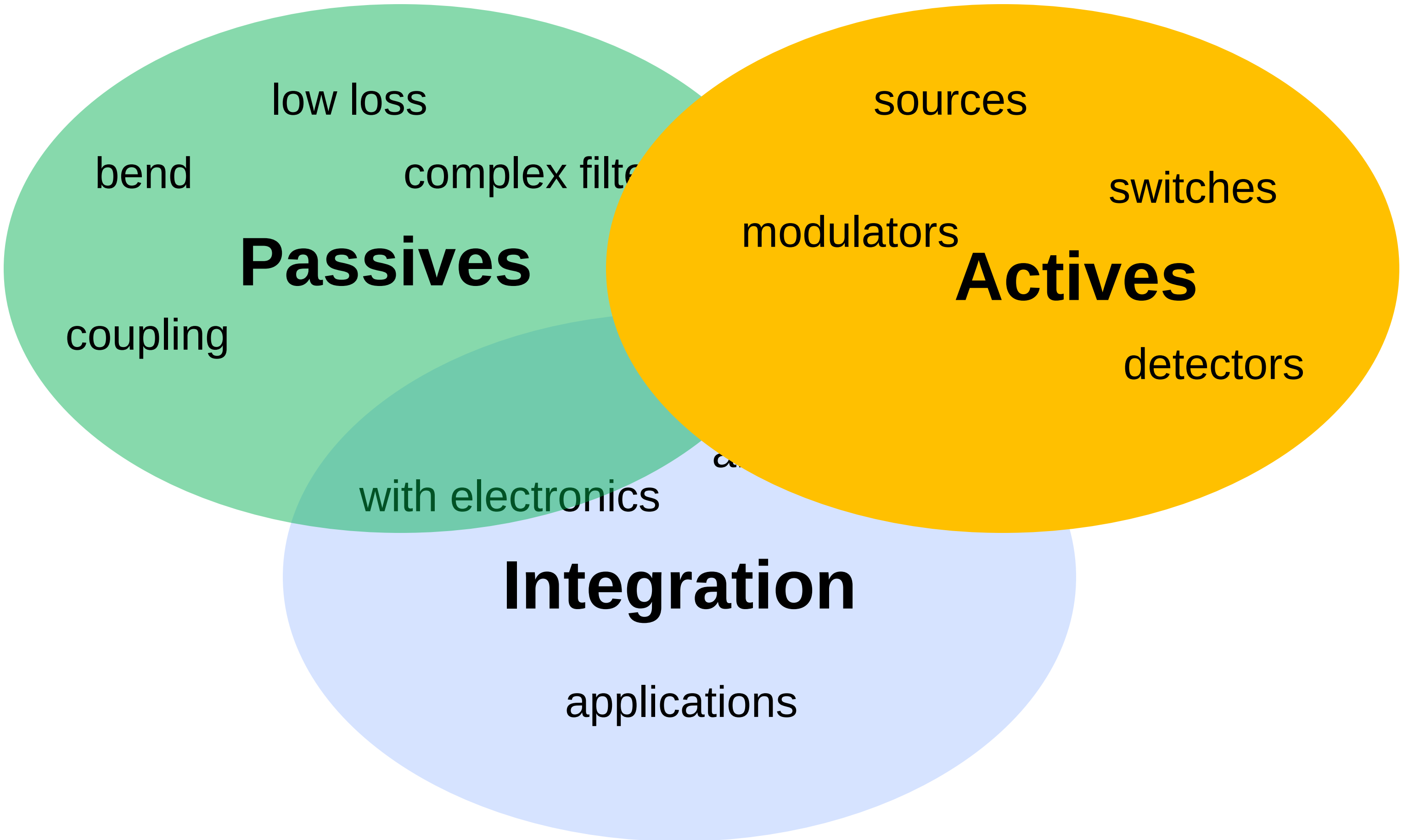
What we did not cover in passives

- Details of fabrication

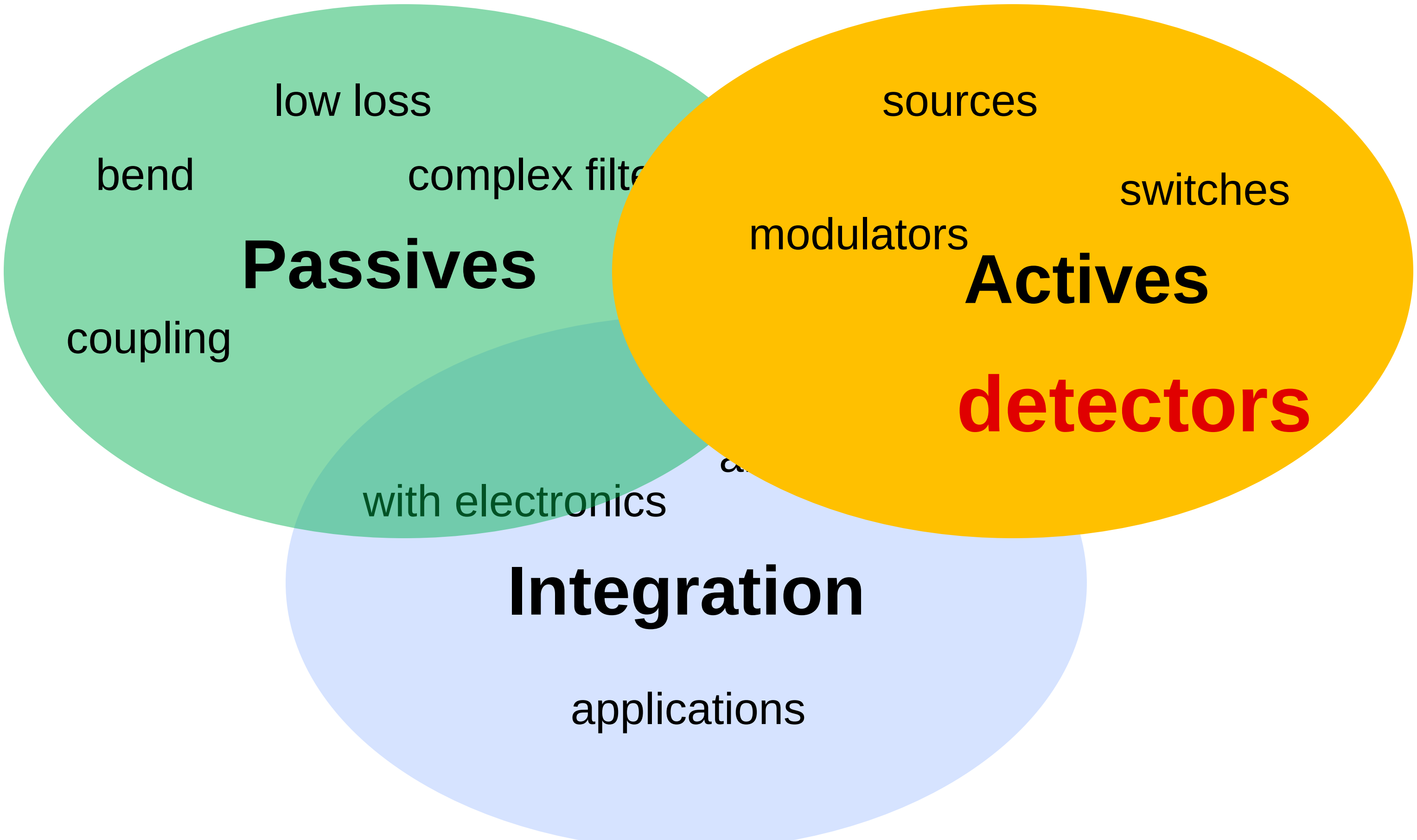
S.K. Selvaraja, JLT 27, p.4070 (2009)

- Special waveguides
  - Slot waveguides
  - Photonic crystal waveguides
- Non linearities
  - Interesting science
  - But also: big headache
- And much more …

Outline


low loss
bend
complex filte
Passives
coupling
sources
switches
modulators
Actives
detectors
with electronics
Integration
applications

Outline


low loss
bend
complex filte
Passives
coupling
sources
switches
modulators
Actives
detectors
with electronics
Integration
applications

Detector

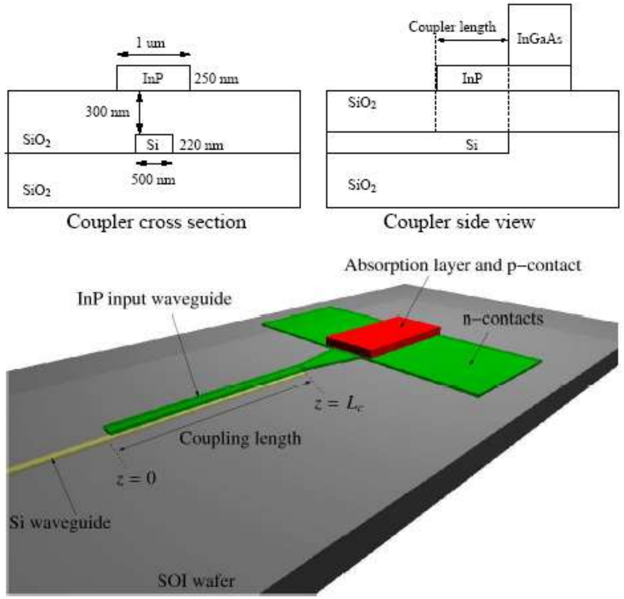
1. Hybrid integration

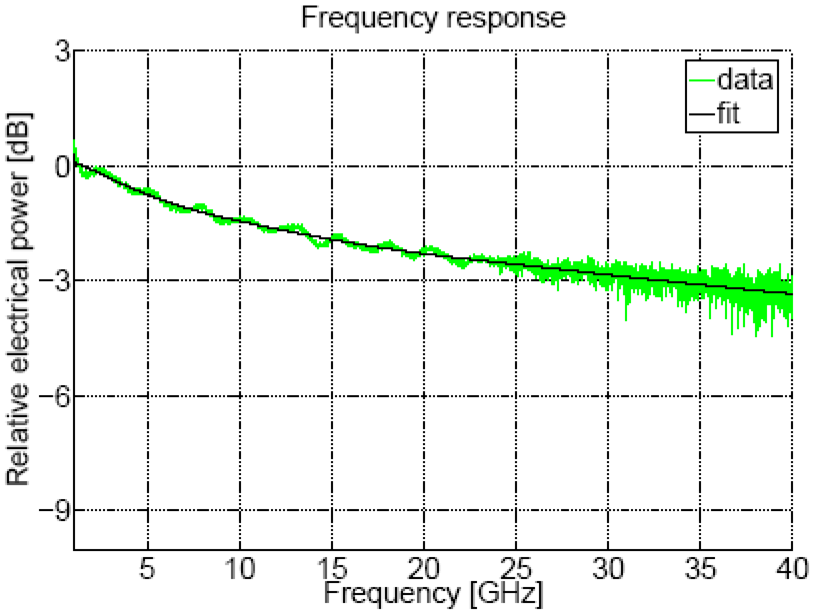
- Prefabricated diode,
- E.g. flip-chip on top of grating coupler
- Cost effective for low density, medium speed

Detector

1. Hybrid integration
2. Heterogeneous integration through waferbonding
   - See next section
   - Example: 33GHZ, 0.45A/W

Binetti e.a., EU PICMOS project





Detector

1. Hybrid integration
2. Heterogeneous integration through waferbonding
3. Implanted silicon, silicides …
   - Low efficiency + ~~slow~~
   - Easy to process
   - Useful monitor

Kotura, OFC2010, Monday

Detector

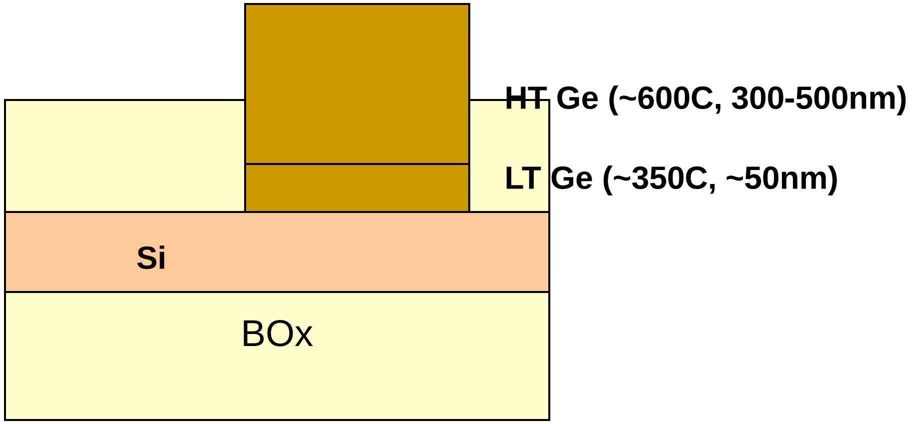
1. Hybrid integration
2. Heterogeneous integration through waferbonding
3. Implanted silicon, silicides …
4. Germanium
   - Efficient absorber up to 1600nm ← (Due to strain!)
   - Large lattice mismatch (~4%). How to integrate ?
     - ☹ Buffer layer ? Requires 1-10um : Too thick !!
     - ☺ Two step growth process
     - ☺ Rapid melt growth

Ge-epitaxy

Two-step growth process:

- **Direct growth of Ge on Si at low temperature (~350°) CVD**
  - **Thin (a few 10nm) highly-dislocated Ge layer**
- **Growth of thick Ge layer (few 100nm) at high temperature (~600°)**
  - **High quality Ge absorbing layer**
- **Thermal annealing to reduce the dislocation density**

Using MBE, UHV-CVD, RP-CVD …



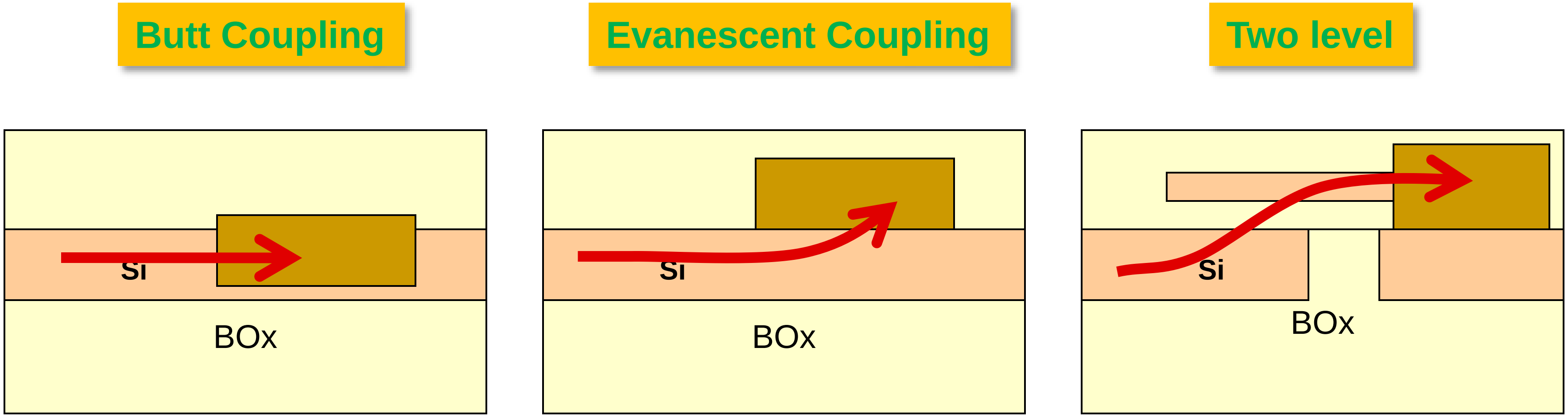
Ge-epitaxy

Two-step growth process:

- Direct growth of Ge on Si at low temperature (~350°) CVD
  - Thin (a few 10nm) highly-dislocated Ge layer
- Growth of thick Ge layer (few 100nm) at high temperature (~600°)
  - High quality Ge absorbing layer
- Thermal annealing to reduce the dislocation density

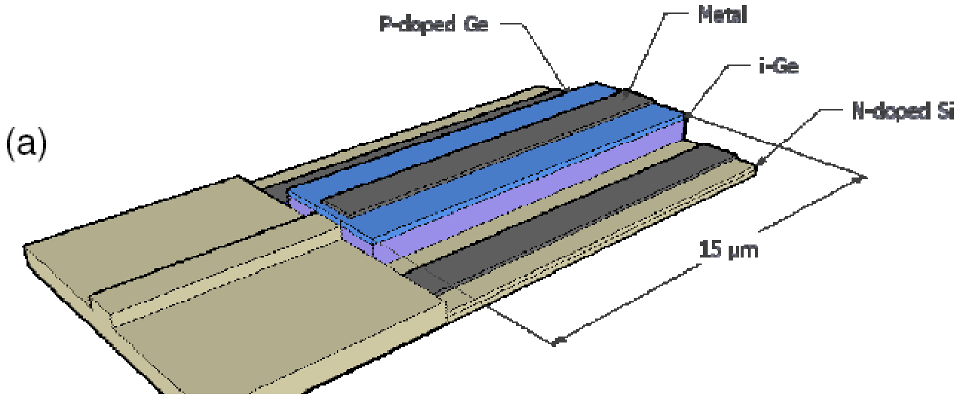
Using MBE, UHV-CVD, RP-CVD …

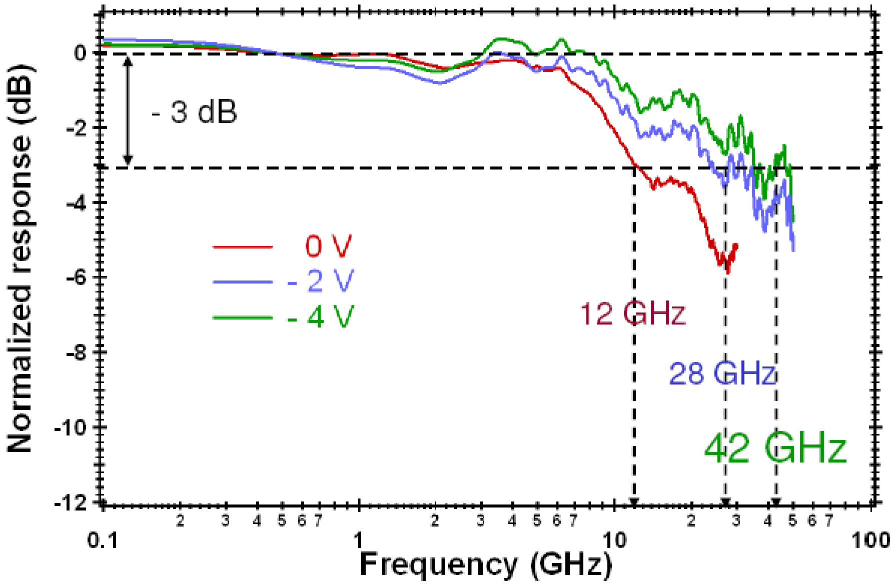
Different integration approaches:

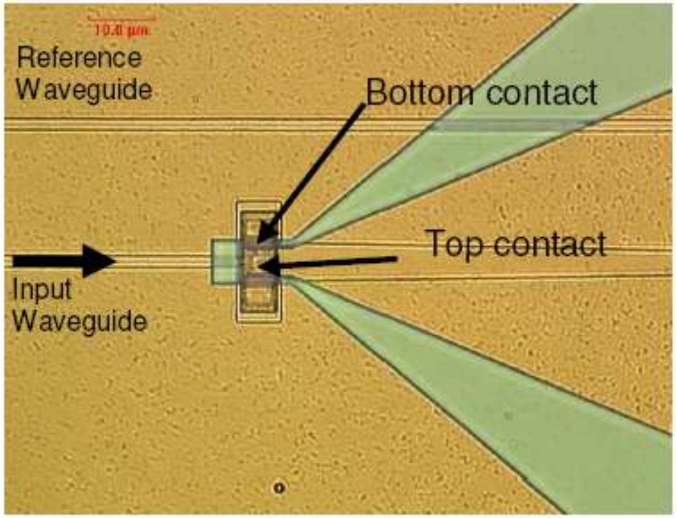


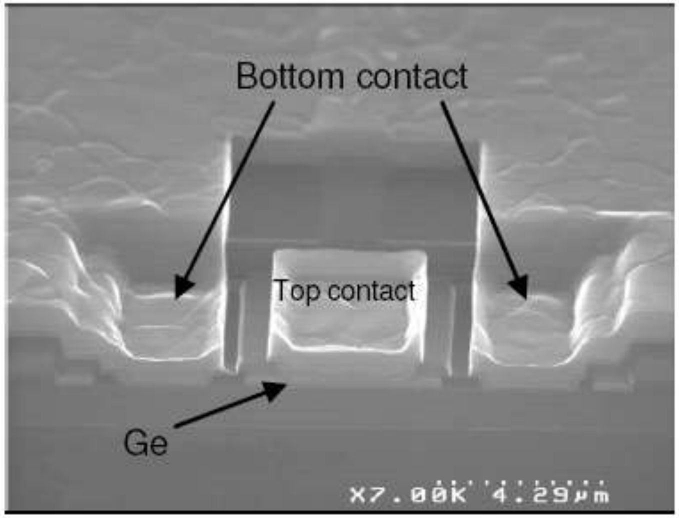
Ge-detector

Two step growth – butt coupling







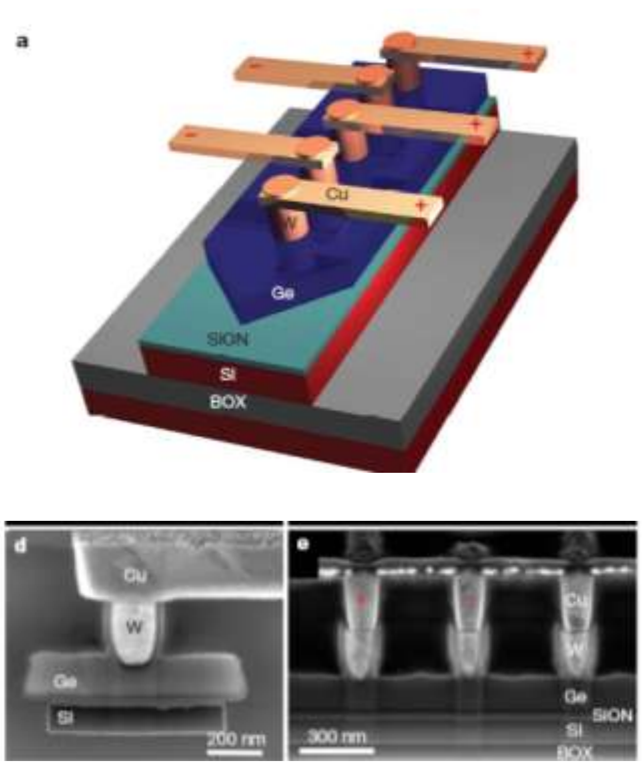


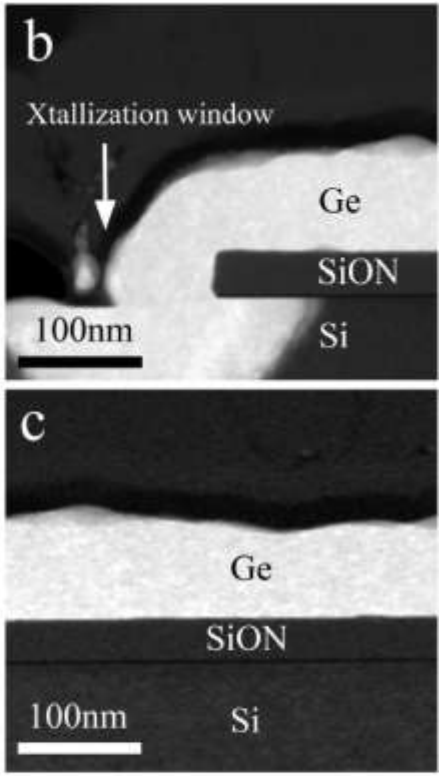
Vivien e.a. , OE 17, pp. 6252 (2009)

Ge-detector

Rapid melt growth

1. Ge CVD deposition on SiON mask with small opening
2. Encapsulation
3. RTA induces melt + recristallisation to single crystal





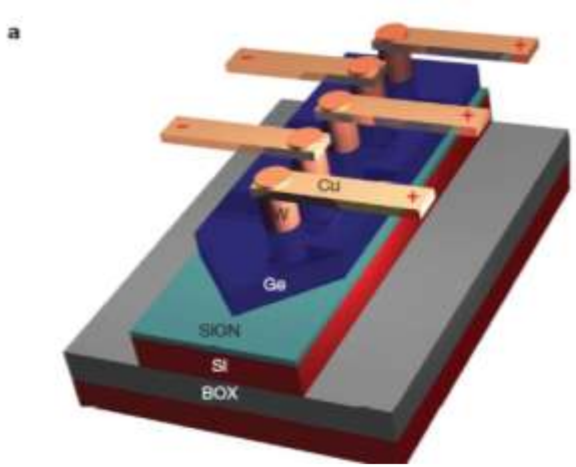
Assefa e.a. , OE 18, pp4997 (2010)
Assefa e.a. , Nature (2010)

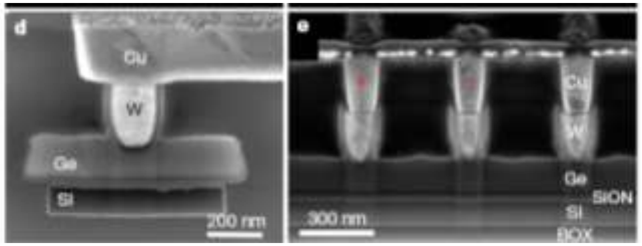
Ge-detector

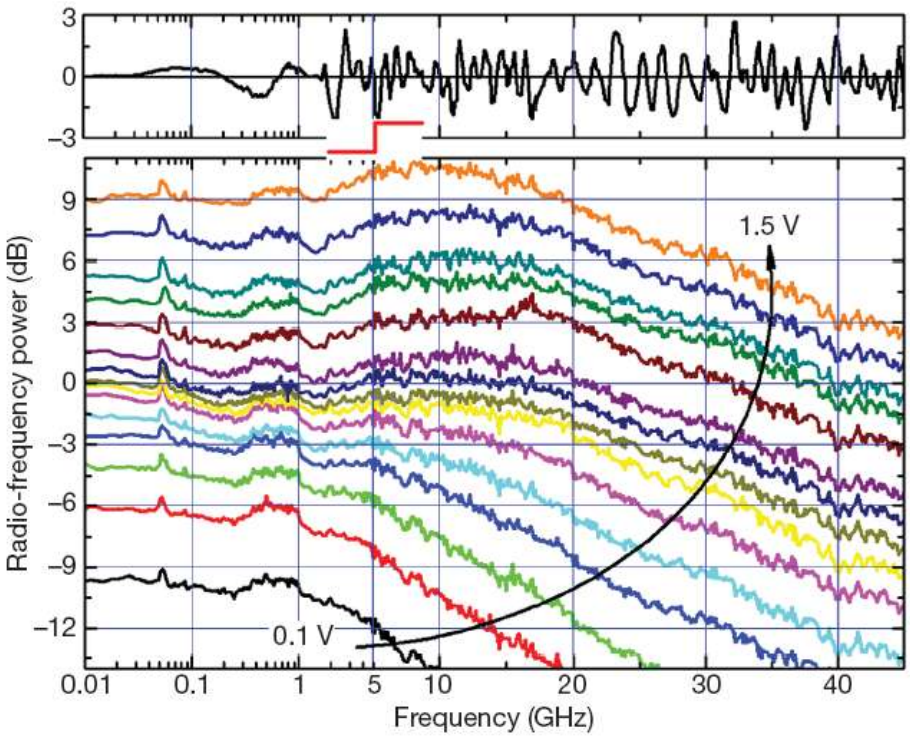
Rapid melt growth: results

Assefa e.a. , OE 18, pp4997 (2010)
Assefa e.a. , Nature (2010)

- 40GB/s operation as PD
- APD operation with
  - 10dB gain at low bias !!
  - >30GHz bandwidth







Detector – state-of-the-art

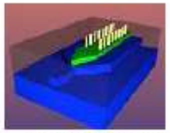
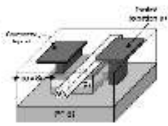
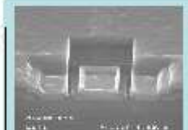
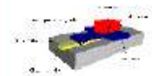
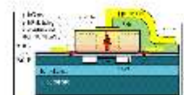
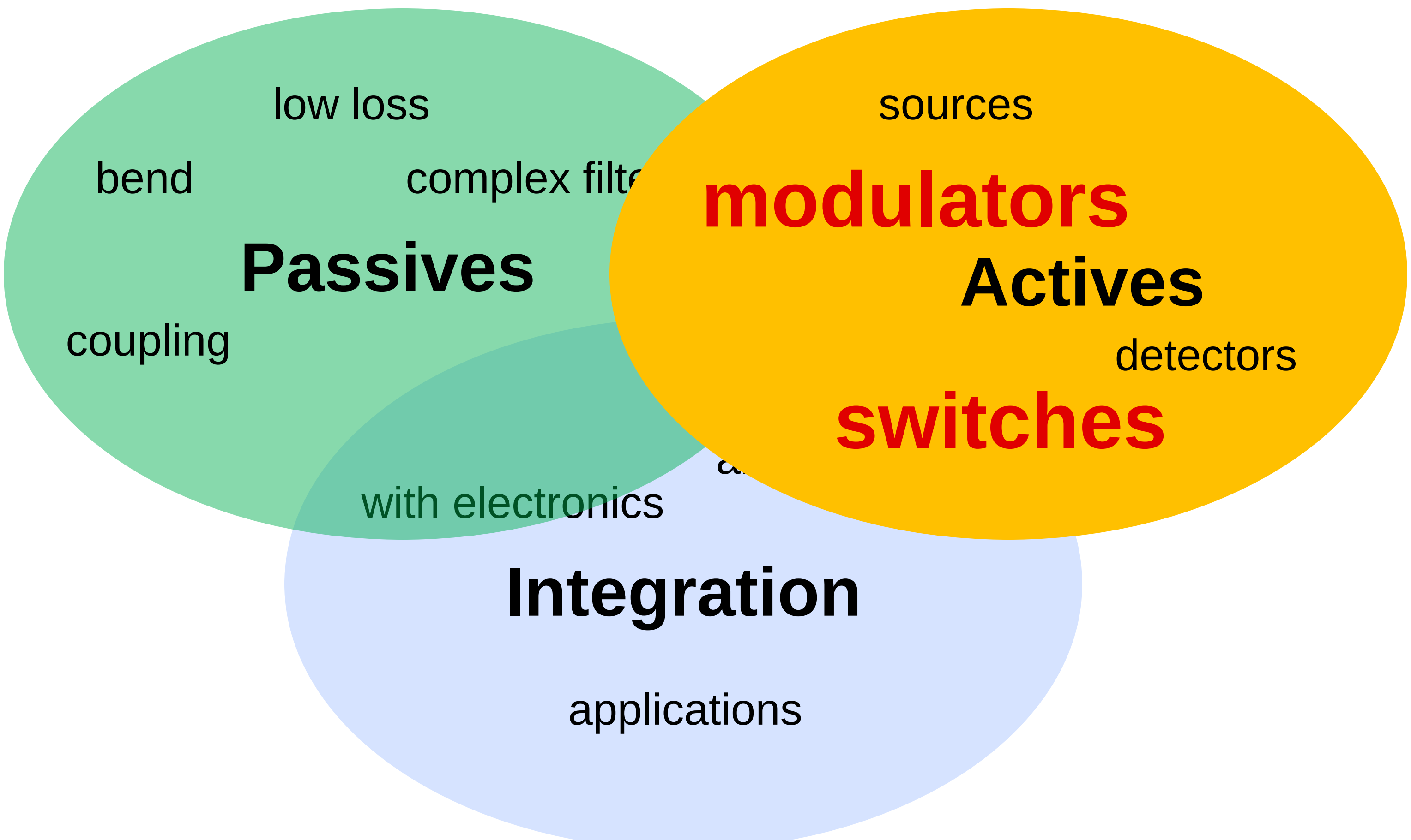
	Ge-on-Si photodetectors					III-V-on-Si photodetectors			
	 LUXTERA	 MIT	 INTEL	 UPS-IEF & LETI	 UPS-IEF & LETI	 EU- PICMOS project	 INTEL	 IMEC	 EU- PICMOS project
Year	~ 2007	2007	2007	2008	2009	2006	2007	2007-09	2009
structure	PIN	PIN	PIN	PIN	PIN	PIN	PIN	MSM	PIN
Dark current at -1V	~10 µA	~1 µA	~170 nA	~ 20 nA	~ 1 µA	~1 nA	~50 nA	~1 nA	~1 nA
Responsivity	~ 0.85 A/W	~1.08 A/W	~0.9 A/W	~ 1 A/W	~0.8 A/W	~0.45 A/W	~0.31 A/W	~1 A/W	~0.7 A/W
Bandwidth	20 GHz	7.2 GHz	31 GHz	42 GHz	~ 90 GHz	33 GHz	0.5 GHz	-	25 GHz

Table compiled by L. Vivien e.a. (IEF) for EU HELIOS project
Extracted from D003 "Silicon Photonics State-of-the-Art", public deliverable (http://www.helios-project.eu/)

Outline


low loss
bend
complex filte
Passives
coupling
sources
modulators
Actives
detectors
switches
with electronics
Integration
applications

Modulation of light

How to make a modulator in silicon

- Silicon has no intrinsic EO-effect
- But:
  - Free carriers induce absorption
  - And index modulation …

Plasma dispersion effect

Empiric relations determined

Soref , JQE 23, (1987).

$$\Delta n = -8{,}8.10^{-22}\Delta N - 8{,}5.10^{-18}\Delta P^{0{,}8}$$

$$\Delta \alpha = 8{,}5.10^{-18}\Delta N + 6{,}0.10^{-18}\Delta P$$

(in silicon at 1550nm – carrier densities in cm^{-3})

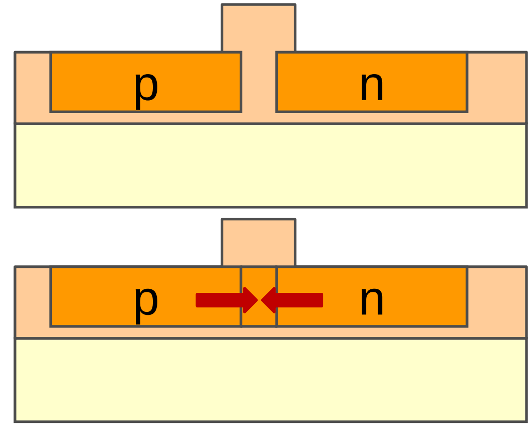
Change carrier densities by

- Doping
- Injection/extraction of carriers

Injection vs. depletion

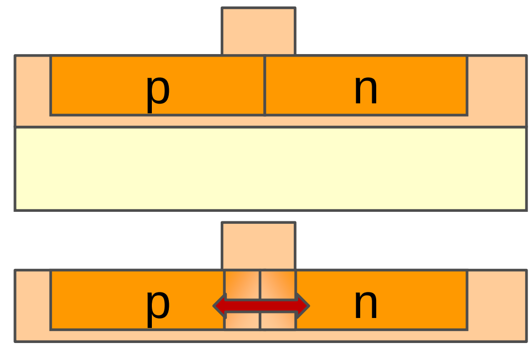
Carrier injection

- p-i-n diode in forward bias
- Inject carriers into waveguides
- Strong effect (many carriers)
- Slow effect (~1GHz)



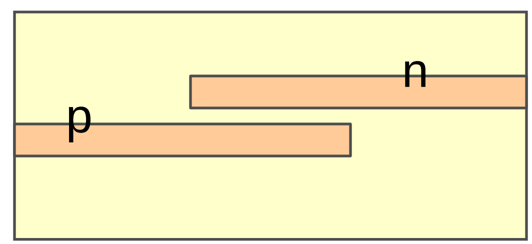
Carrier depletion

- p-n diode in reverse bias
- Extract carriers from waveguide
- Weaker effect
- Fast effect (>40GHz)



Carrier accumulation

- Accumulation at oxide
- Similar to capacitor
- Fast

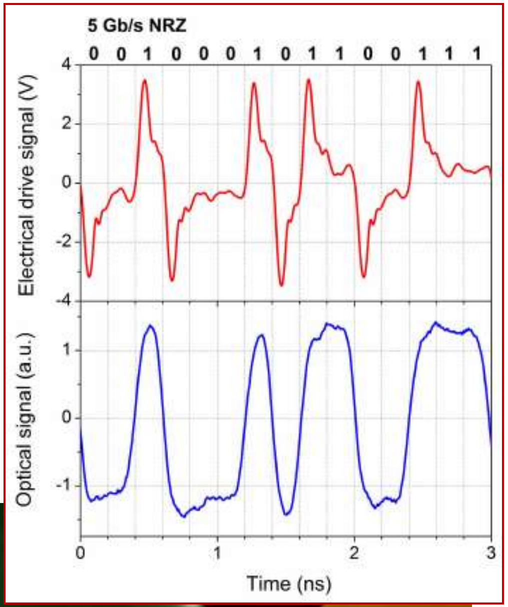


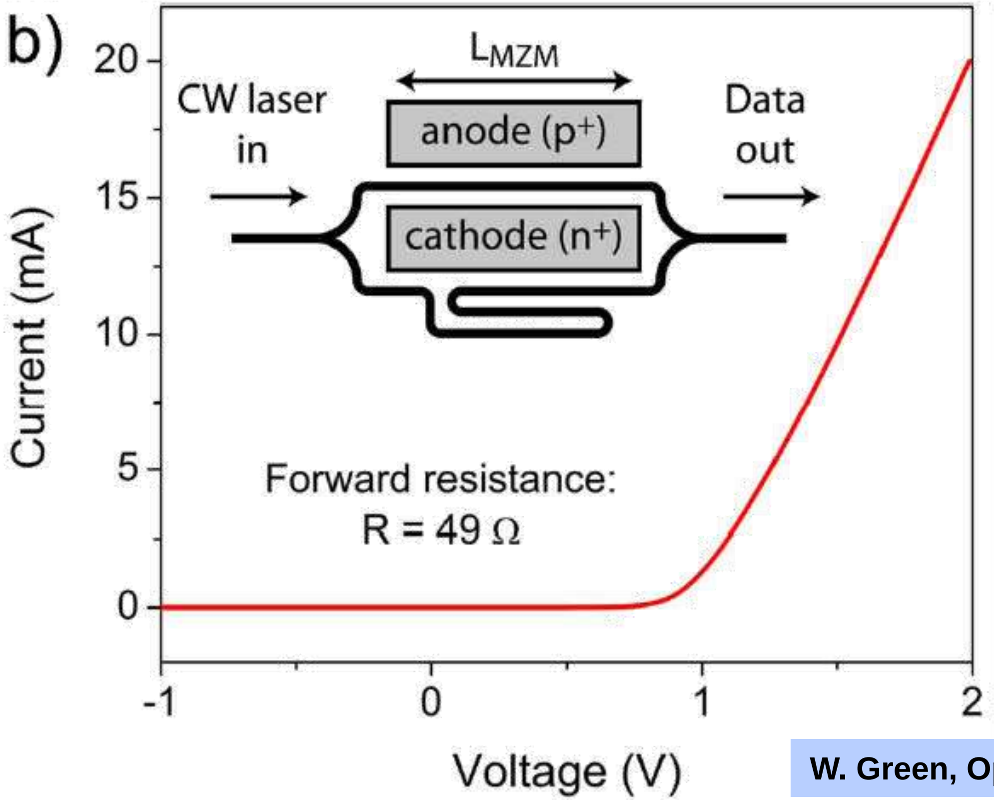
Injection Modulator

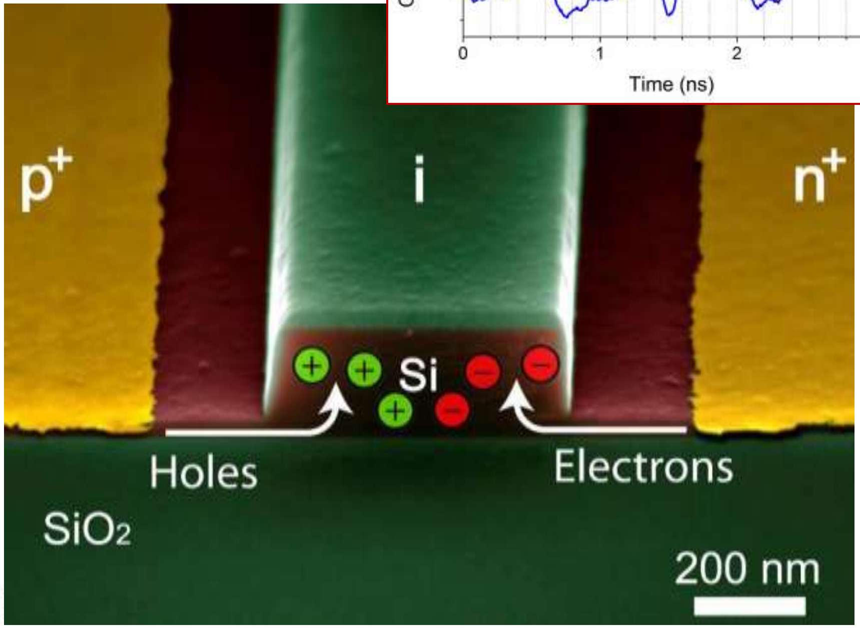
100-200µm length

p-i-n diode

MZI configuration





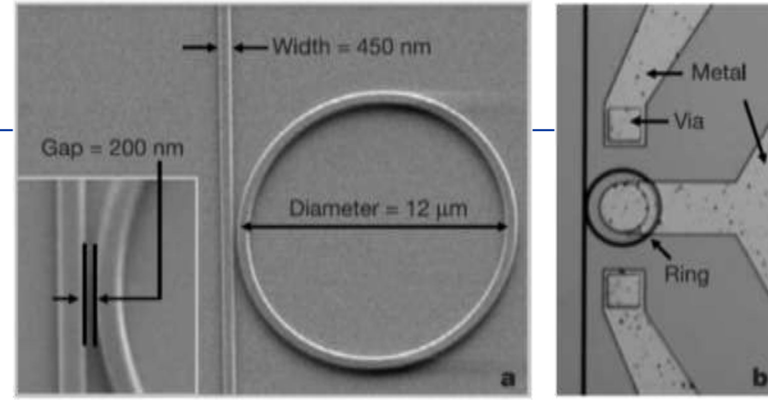


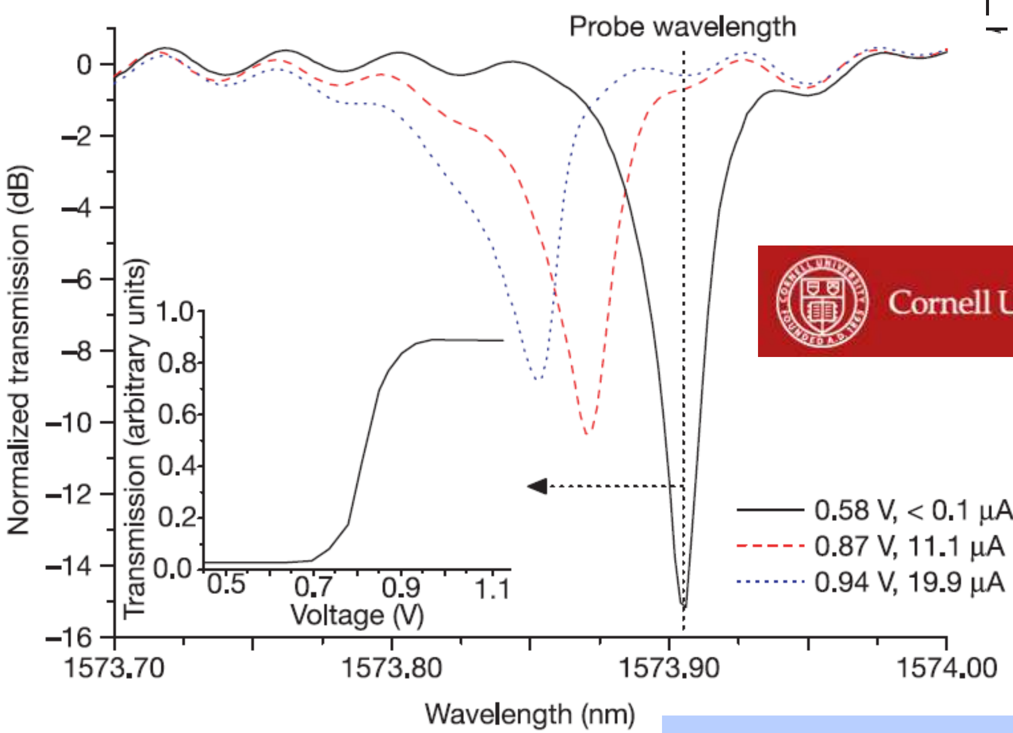
W. Green, OpEx 15, p17106 (2007)

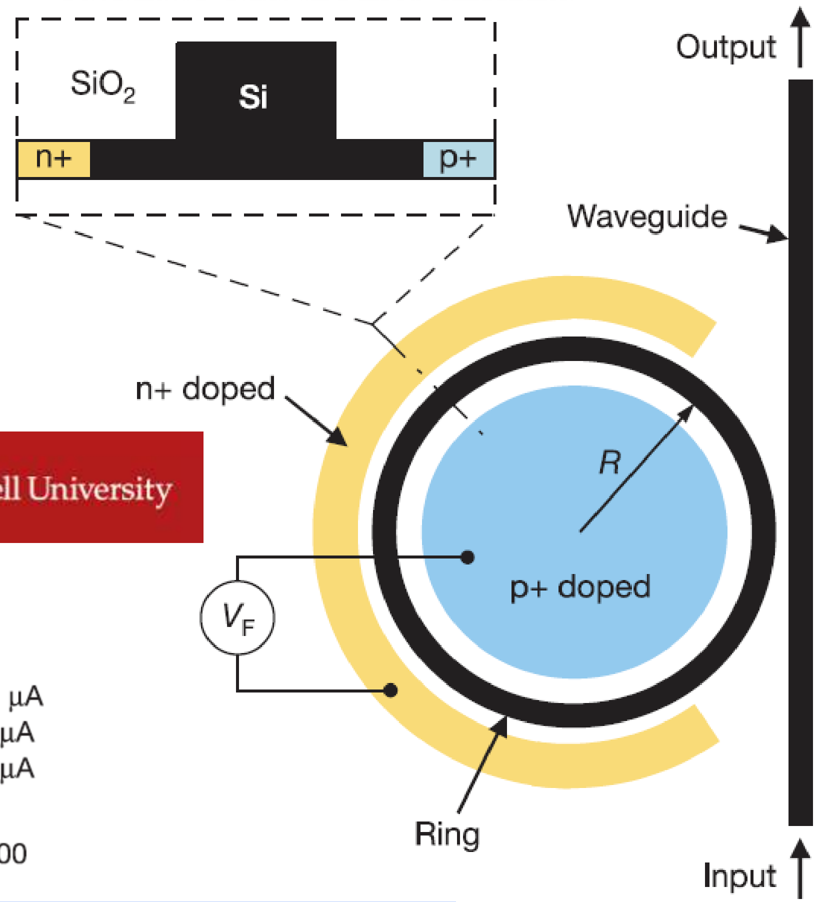
Ring Modulator

Speed ~2GB/s

With preemphasis: >20GB/s







Cornell University

Q. Xu et al, nature 435(19), p03569 (2005)

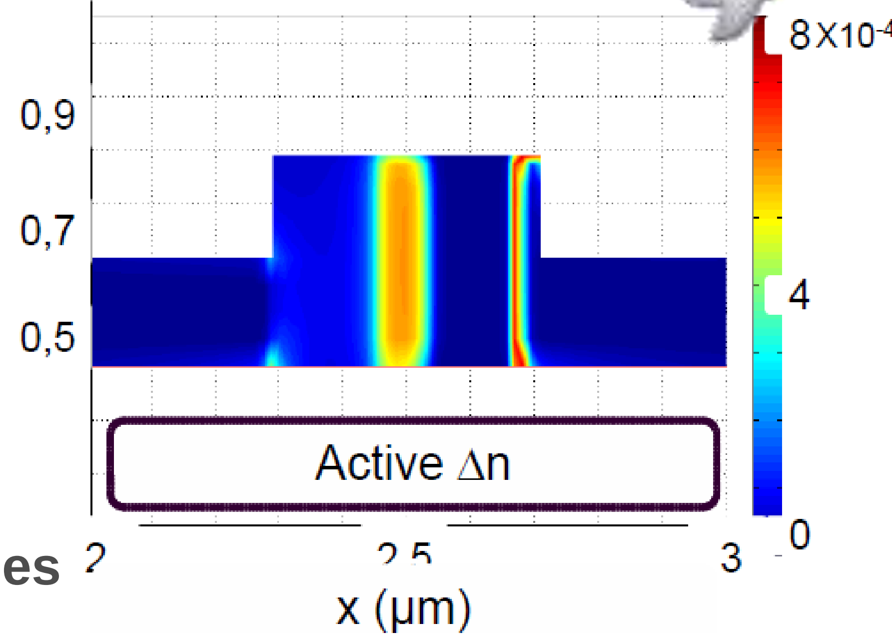
Example: depletion modulator

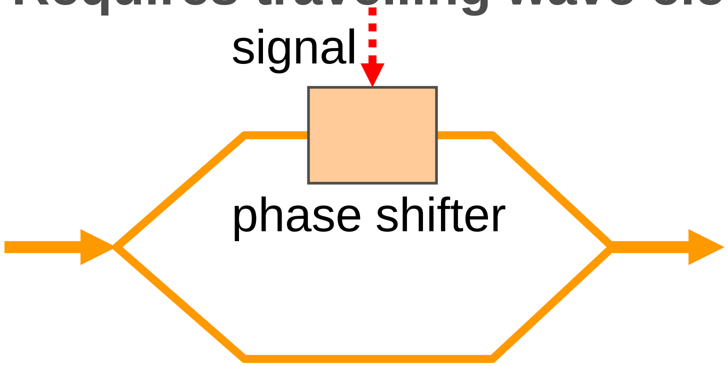
Complex multi-doping profile

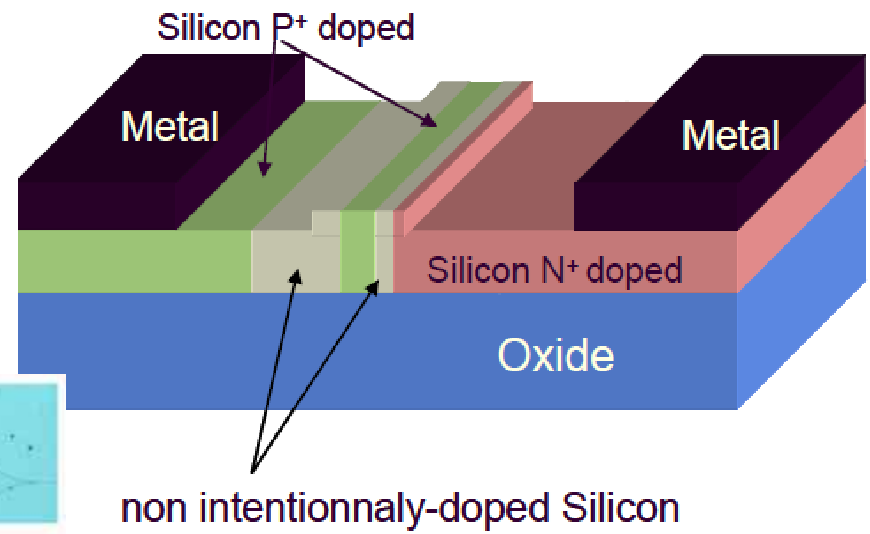
- Larger index change
- Lower RC

But

- Still a long device (4mm)
- Requires travelling wave electrodes







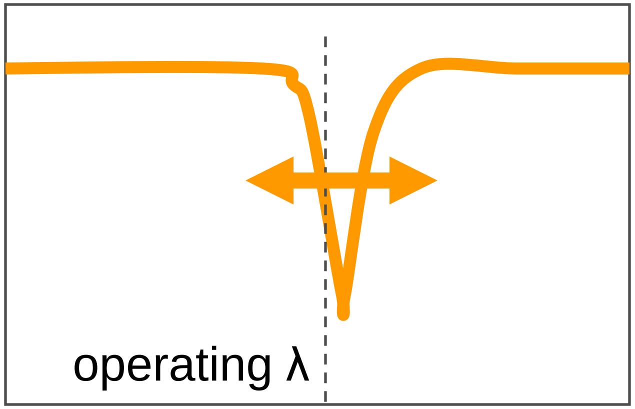
4mm long mach zehnder

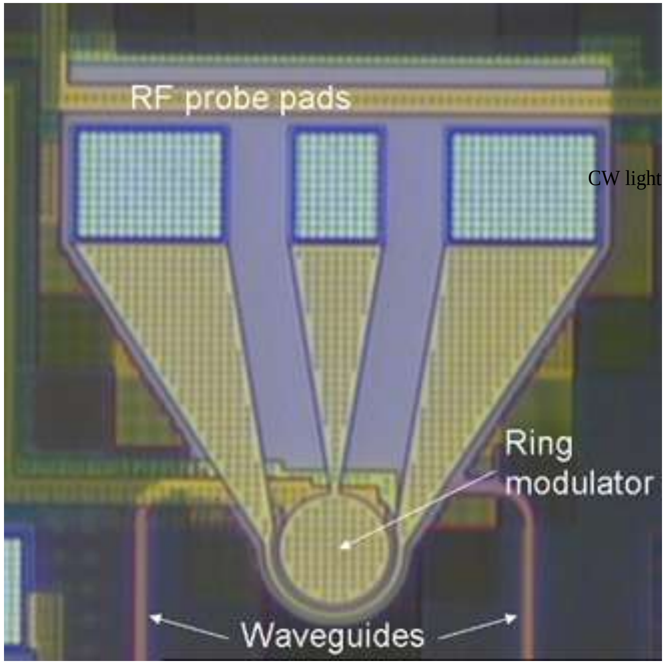
D. Marris-Morini, OpEx 16 (2008)

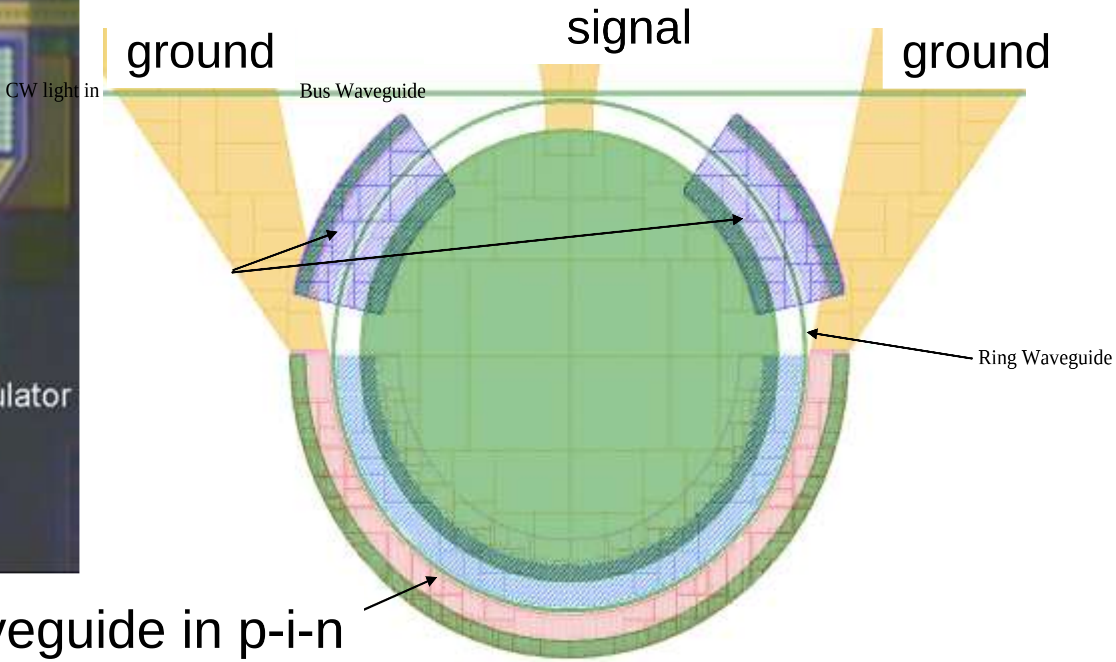
Ring modulator

Ring resonator in p-i-n junction

- Carrier injection
- Change refractive index
- Change resonance







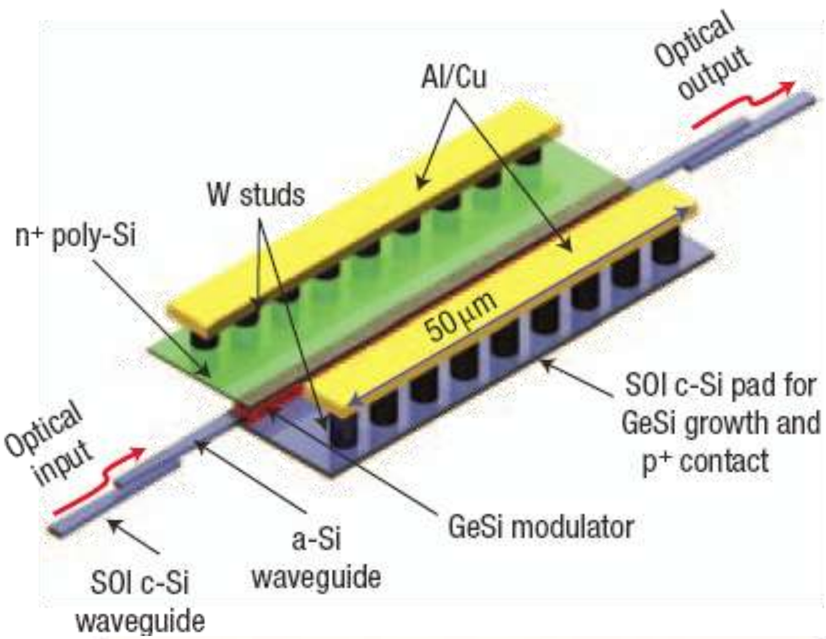
C. Gunn, IEEE Micro, 2006

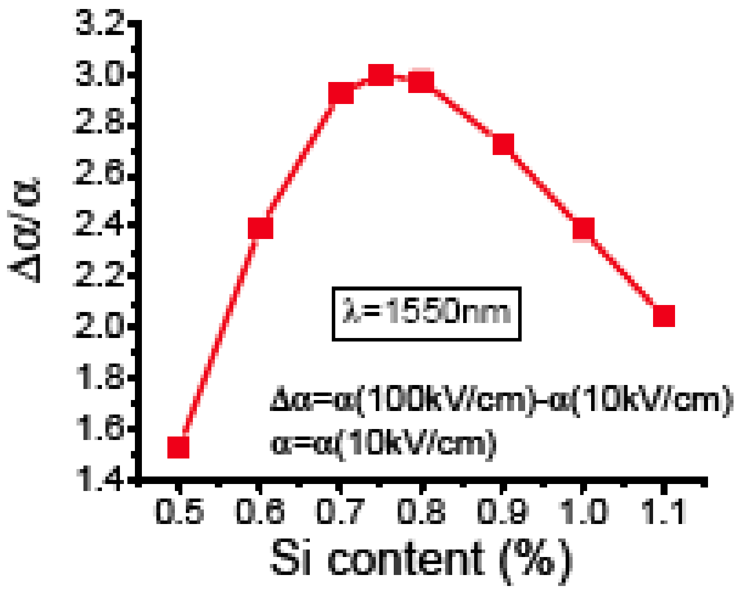
SiGe electroabsorption modulator

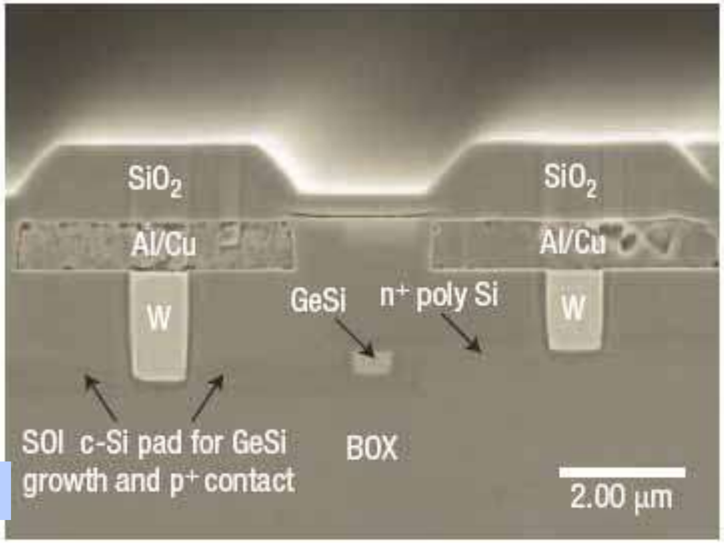
Operation at 1550nm

Compact: 30µm

But: one operation point.

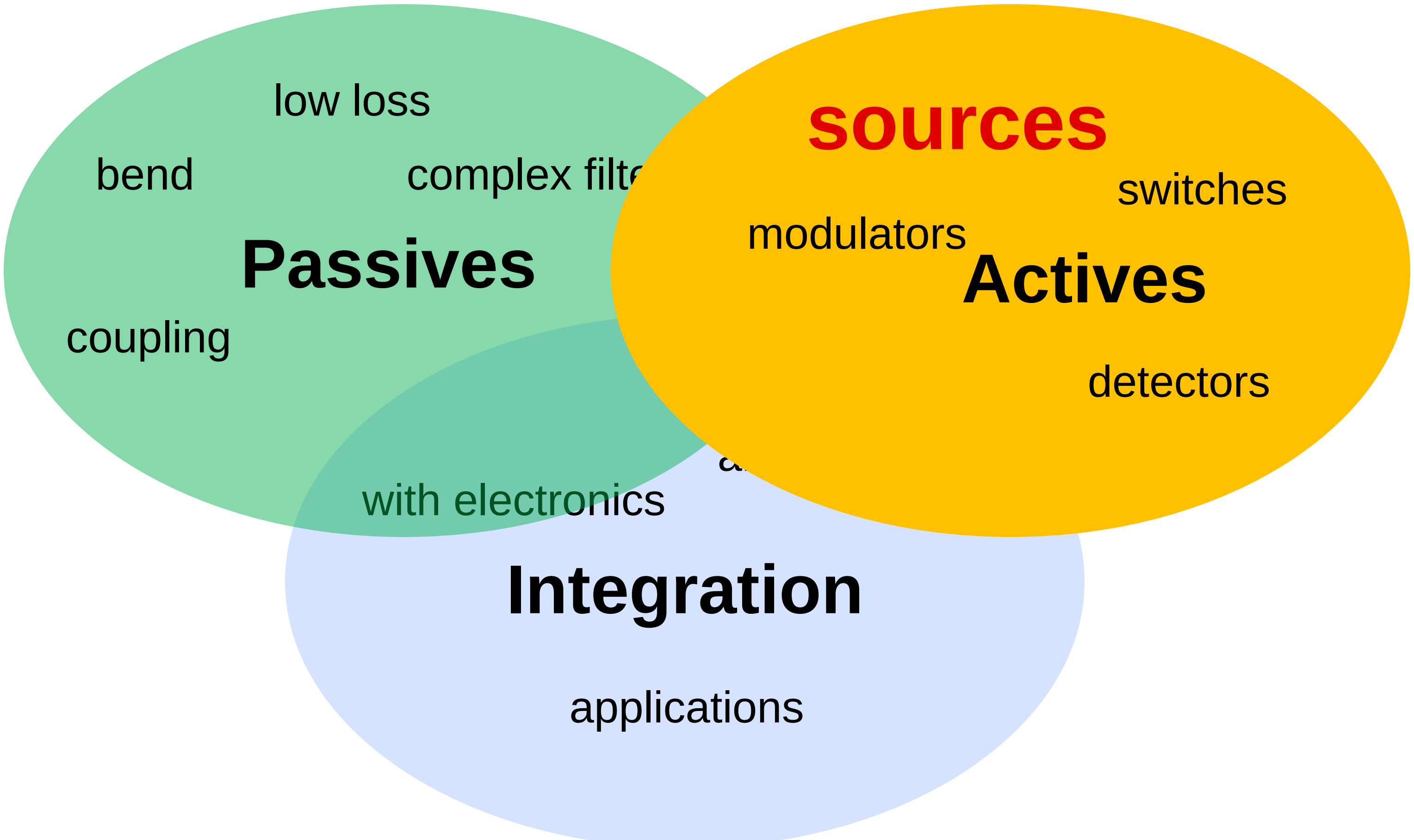






Liu, Nature Photonics 2, p.433 (2008)

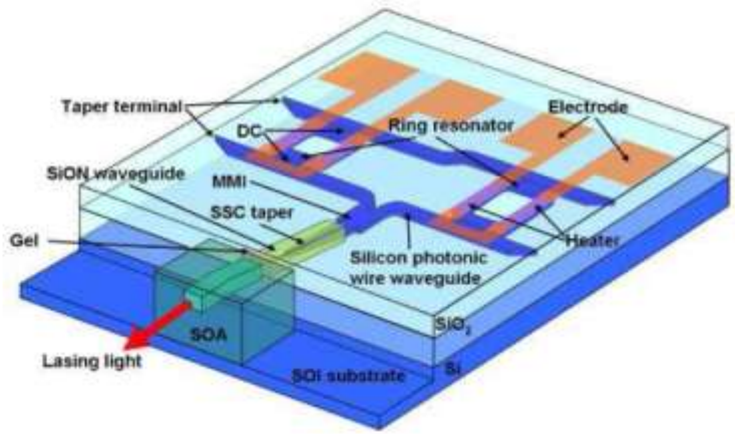
Outline

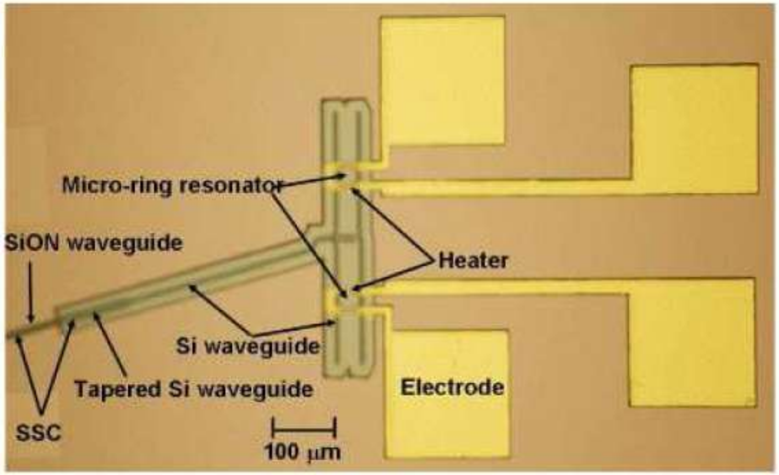


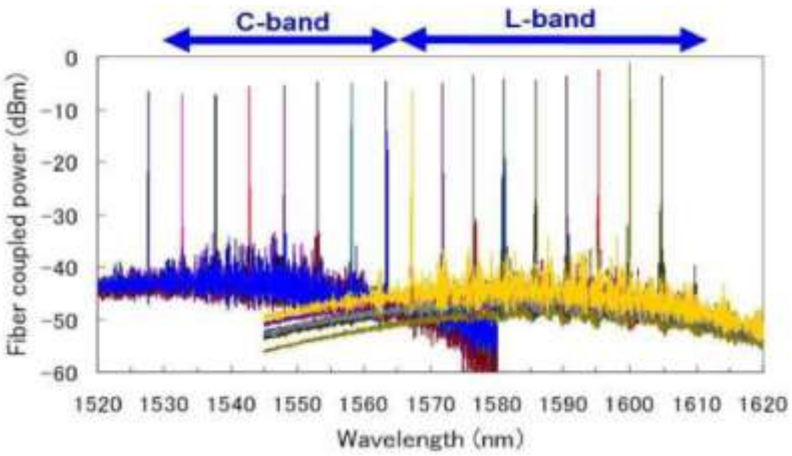
low loss
bend
complex filte
Passives
coupling
sources
switches
modulators
Actives
detectors
with electronics
Integration
applications

Sources on Silicon

1. Hybrid integration





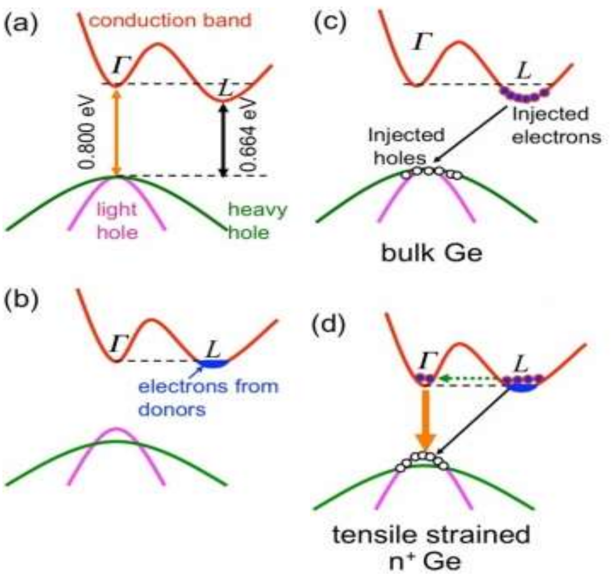


Song e.a. OE 17, 14063-14068 (2009).

Sources on Silicon

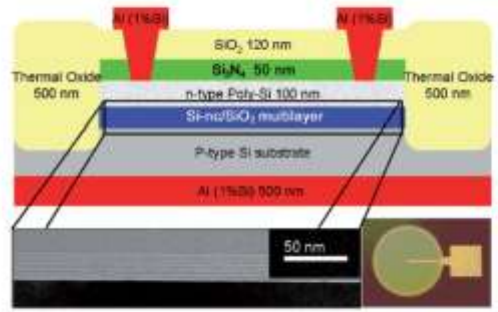
1. **Hybrid integration**
2. **Monolithic integration**

Strained Ge-laser



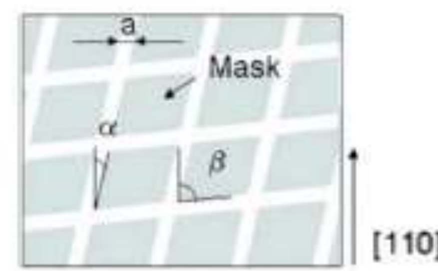
MIT press release

Er-doped Si nanocrystals



Zhizhong, Y. et al. Proc of the IEEE 97, 1250 (2009).

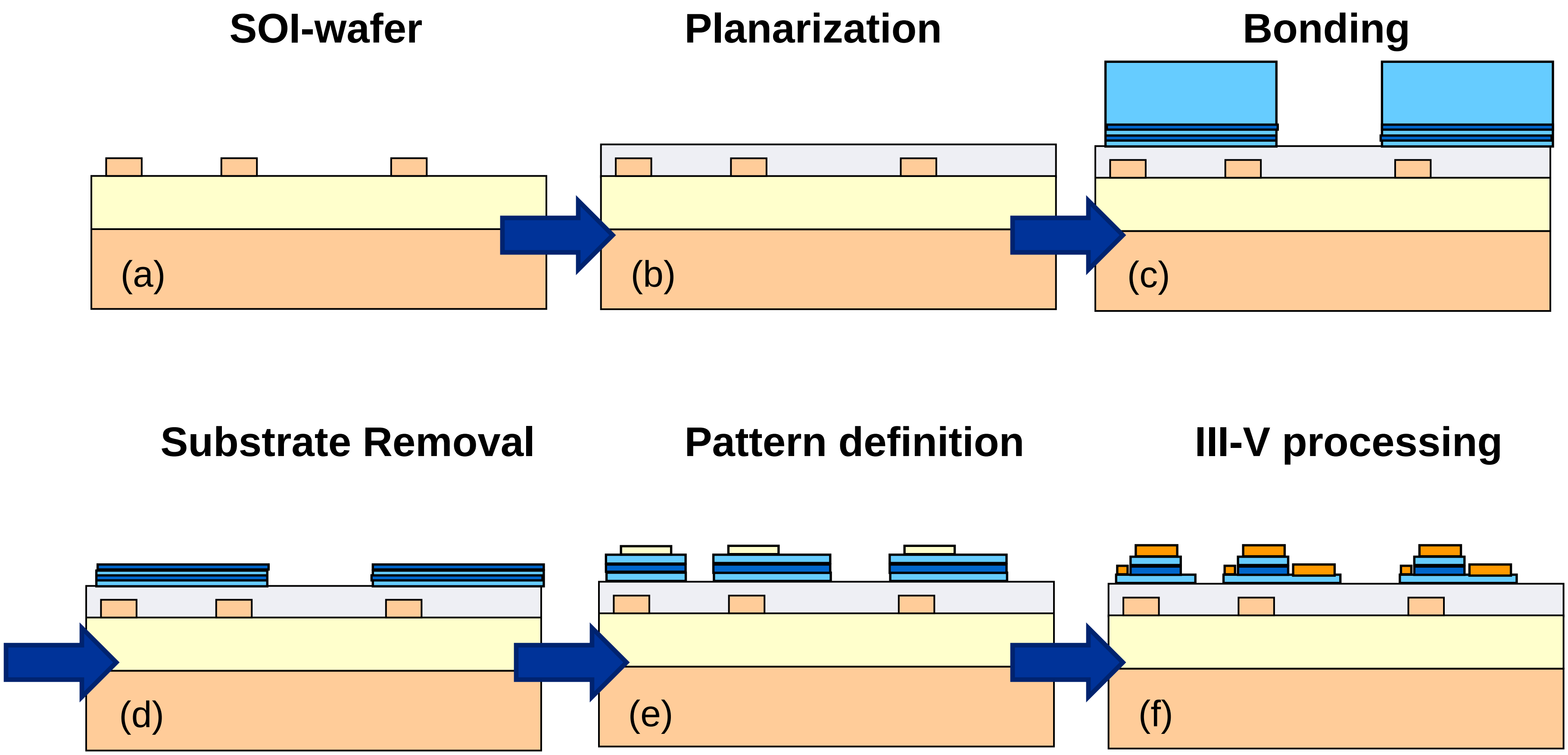
III-V on silicon epitaxy



Junesand e.a., IPRM 2009 pp59

Sources on Silicon

1. Hybrid integration
2. Monolithic integration
3. Integration through waferbonding techniques



III-V/Silicon photonics

Bonding of III-V epitaxial layers

- **Molecular die-to-wafer bonding, direct bonding**
  - Based on van der Waals attraction between wafer surfaces
  - Requires “atomic contact” between both surfaces

    - very sensitive to **particles**

    - very sensitive to **roughness**

    - very sensitive to **contamination of surfaces**

LETI, UCSB+INTEL …

- **Adhesive die-to-wafer bonding**
  - Uses an adhesive layer as a glue to stick both surfaces
  - Requirements are more relaxed compared to Molecular

    - glue compensates for particles (some)

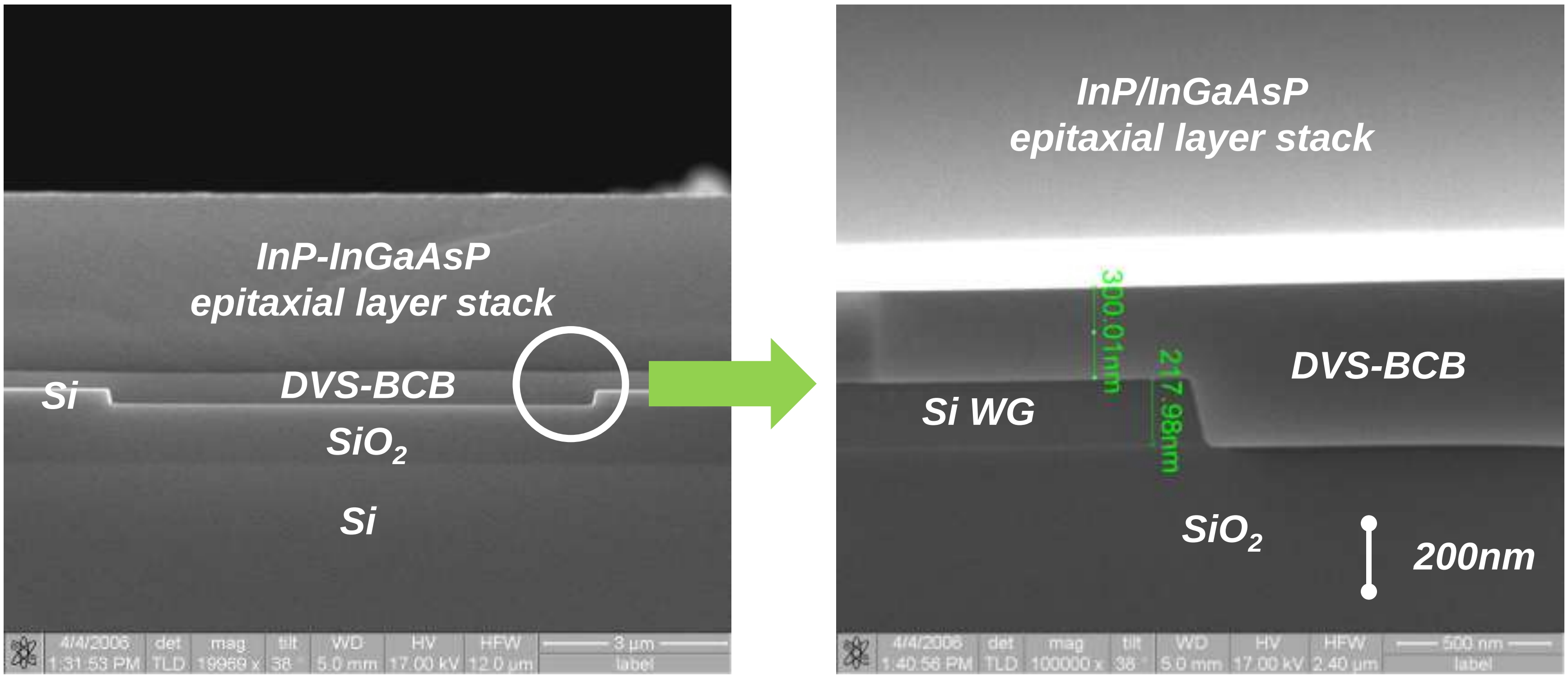
    - glue compensates for roughness (all)

    - glue allows (some) contamination of surfaces

IMEC/Ghent University

Bonding Technology

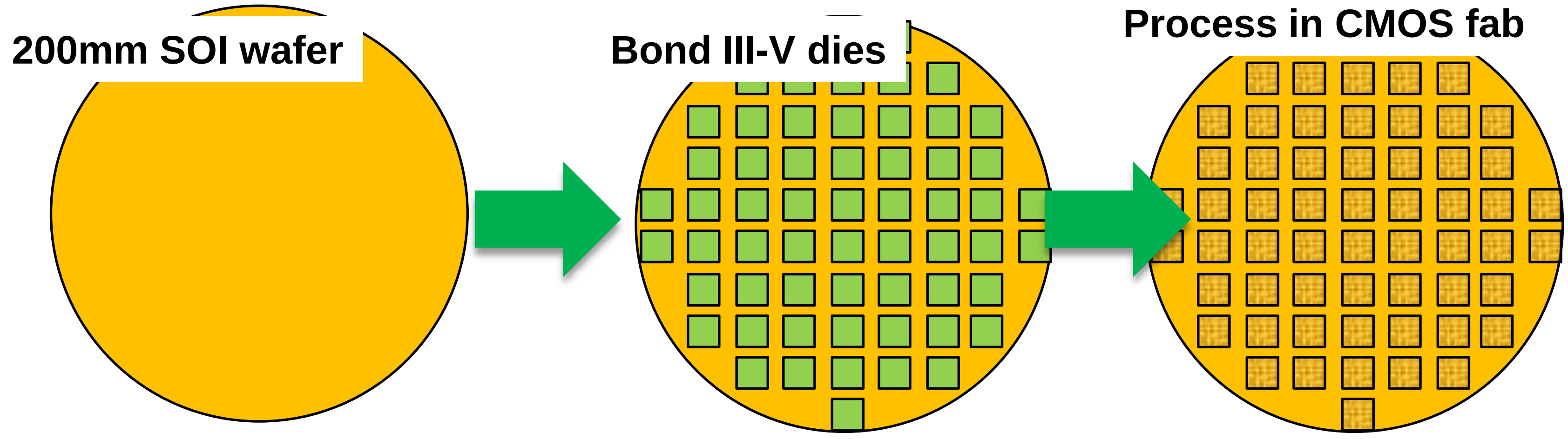
Cross-sectional image of III-V/Silicon substrate



- **200nm bonding layer routinely and reliably obtained**
- **Recently : focus on thin bonding layer develoment (<100nm)**

Business model ?

Option I : all CMOS-fab processing

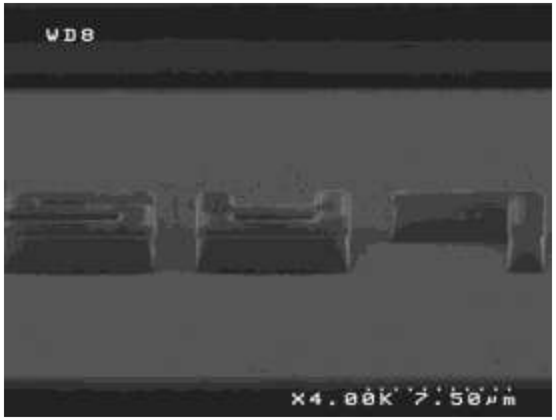


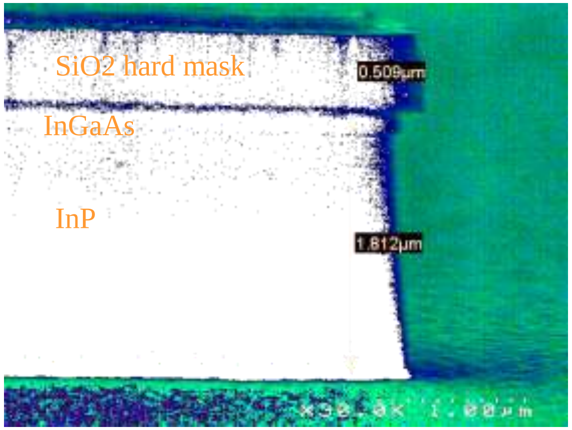
- **Need to cover full 200mm wafer (or 300mm ?)**
- **Need to adapt processes to CMOS fab**
  - **Gold free contacts**
  - **III-V etching**
  - …

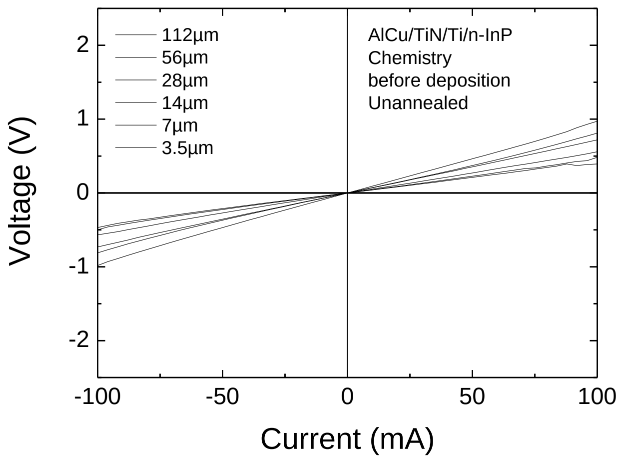
200mm process development

InP processing in CMOS-fab ?   YES !!!

- **CEA/LETI demonstrated full laser processing in CMOS pilot line**
  - CH_4/H_2 RIE process in 200mm reactor
  - Gold free contacts demonstrated (AlCu/TiN/Ti)



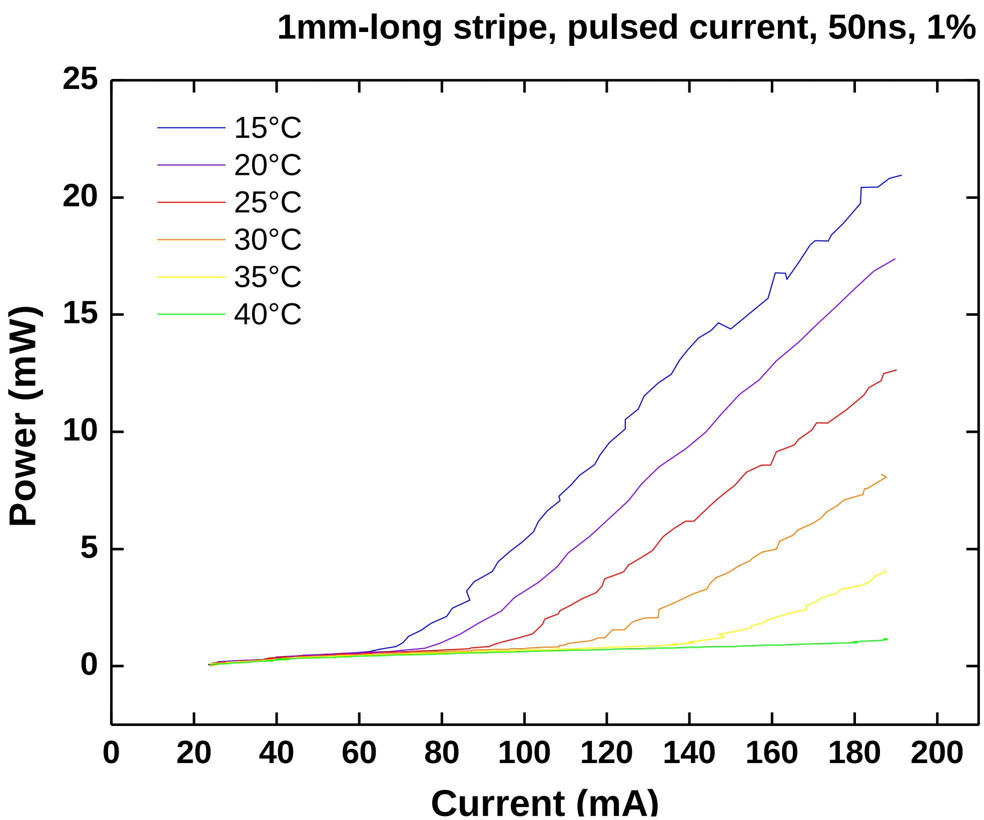




L. Grenouillet e.a., "CMOS compatible contacts and etching for InP-on-silicon active devices", GFP 2009, San Fransisco

FP lasers on silicon

- AlGaInAs active layer – 1.3µm
- individual die processed
  - $CH_4/H_2/O_2$ dry etching
  - metallization + lift off process

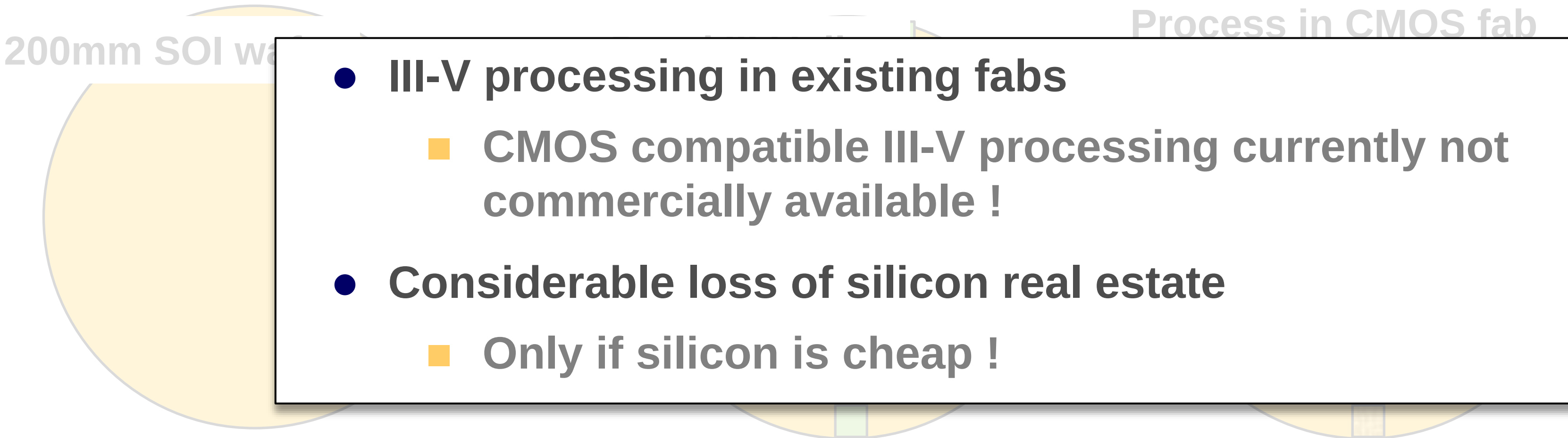


- pulsed operation:
  - L = 1mm
  - λ = 1.3µm
  - P >20 mW
  - max T = 40 C

© CEA 2009. All rights reserved
Any reproduction in whole or in part on any medium or use of the information contained herein
is prohibited without the prior written consent of CEA

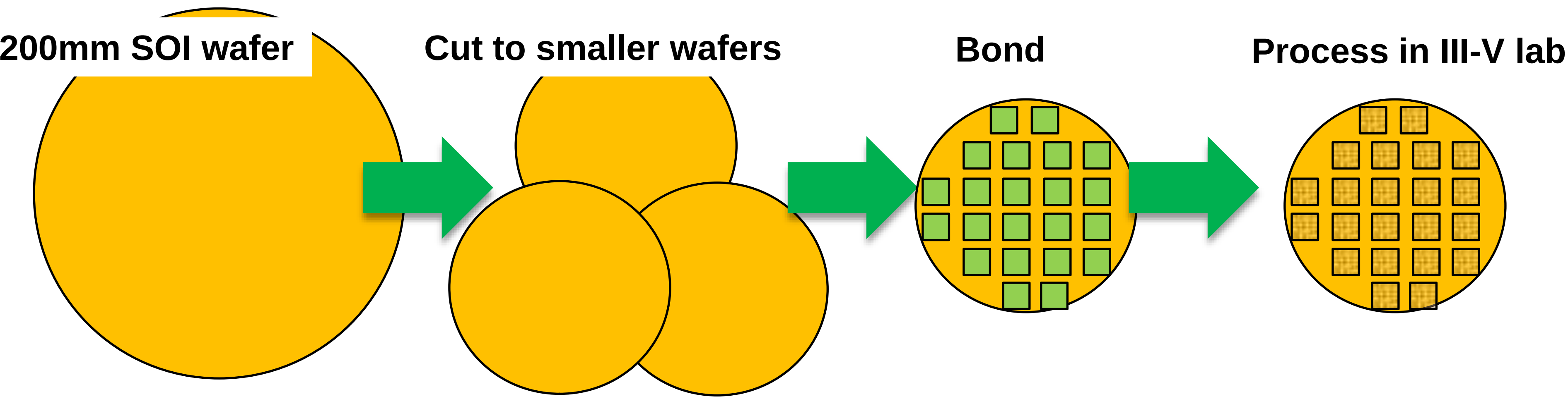
Business model ?

Option I : all CMOS-fab processing



- III-V processing in existing fabs
  - CMOS compatible III-V processing currently not commercially available !
- Considerable loss of silicon real estate
  - Only if silicon is cheap !

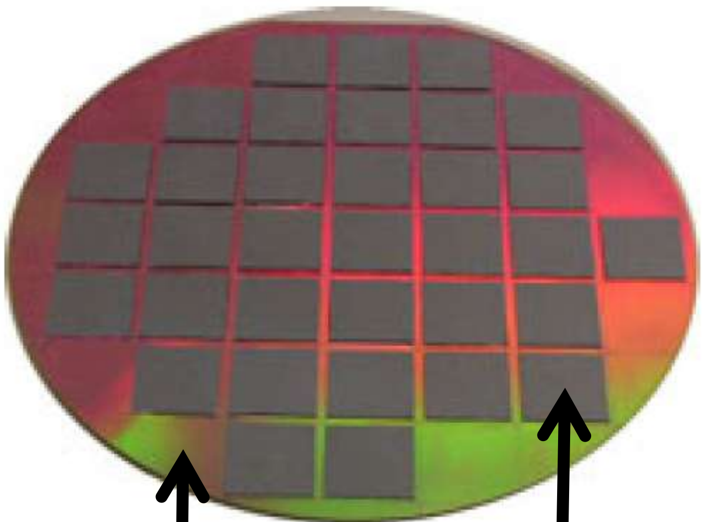
Option II : CMOS-fab + III-V fab processing



Option II: example

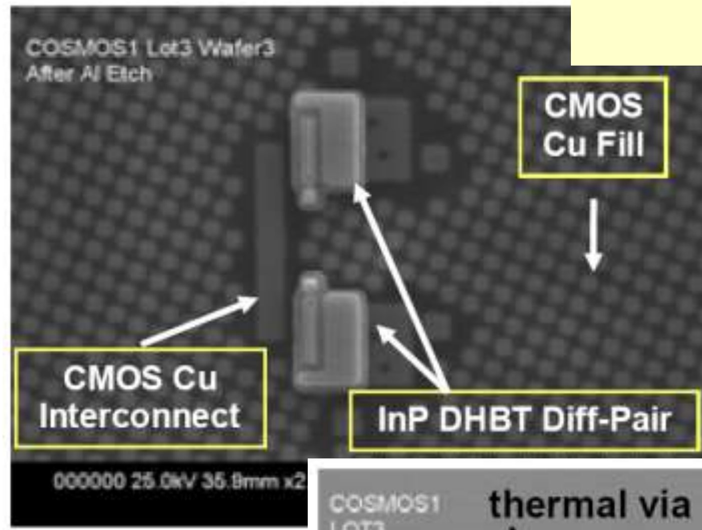
InP HBTs on IBM CMOS (HRL Labs)

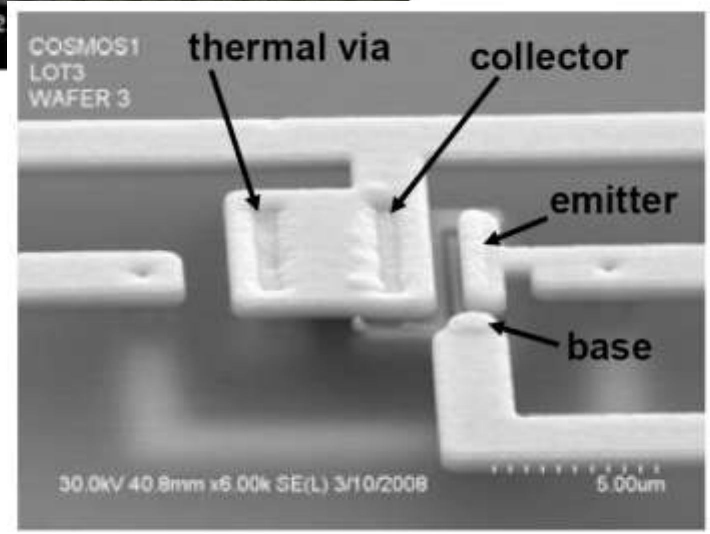
Collective processing after bonding



IBM 130nm RF-CMOS cut to 3 inch wafers

BCB-bonded unprocessed InP dies



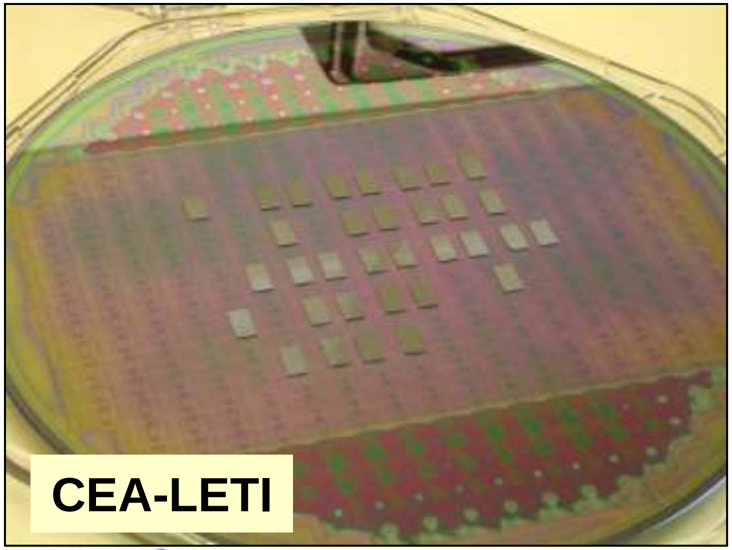


Y. Royter e.a. , "Technology for Dense Heterogeneous Integration of InP HBTs and CMOS," in *CS Mantech*, Tampa, Florida, 2009

Business model

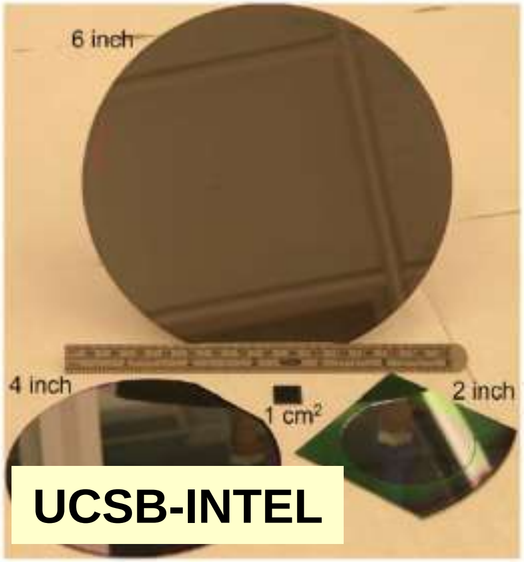
Die bonding … OR

- Edge effects may induce bonding effects
- Independent of size silicon wafer (200mm, 300mm …)
- Total required material may be smaller
- Rapid pick and place process required



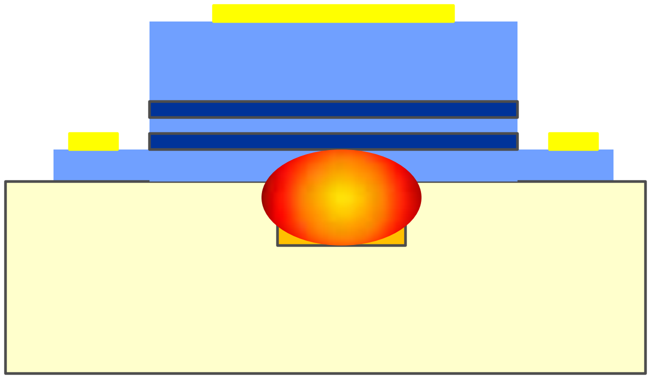
Wafer bonding...

- Currently more reliable process
- Largest wafers now available 150mm, 100mm more standard
- Single step process



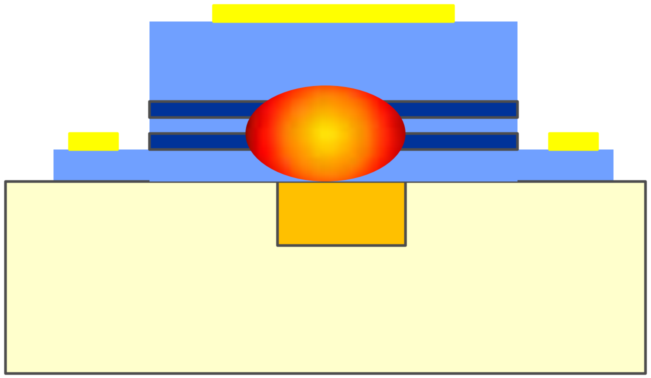
Design options

Light centred in Silicon



- High overlap with silicon:
  - Allows for modal control
  - Easy coupling to waveguide
- Low overlap with III-V : low gain –high saturation threshold
- Not compatible with sub-400nm silicon thickness

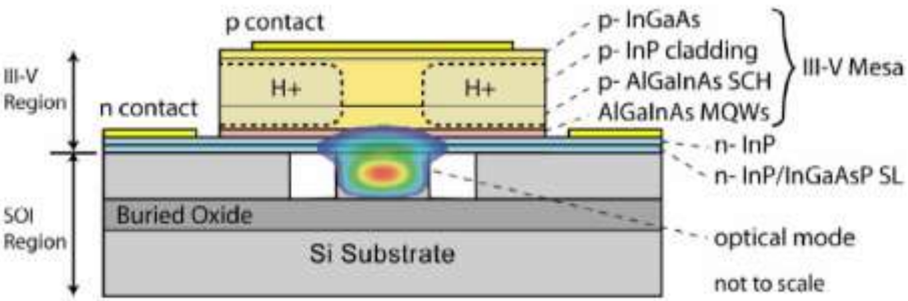
Light centred in III-V



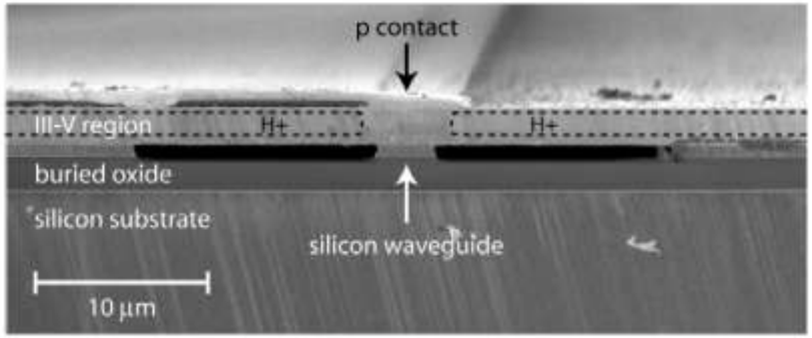
- High gain
- Coupling to silicon may require special structures

Hybrid evanescent laser

Hybrid evanescent laser (UCSB/INTEL)

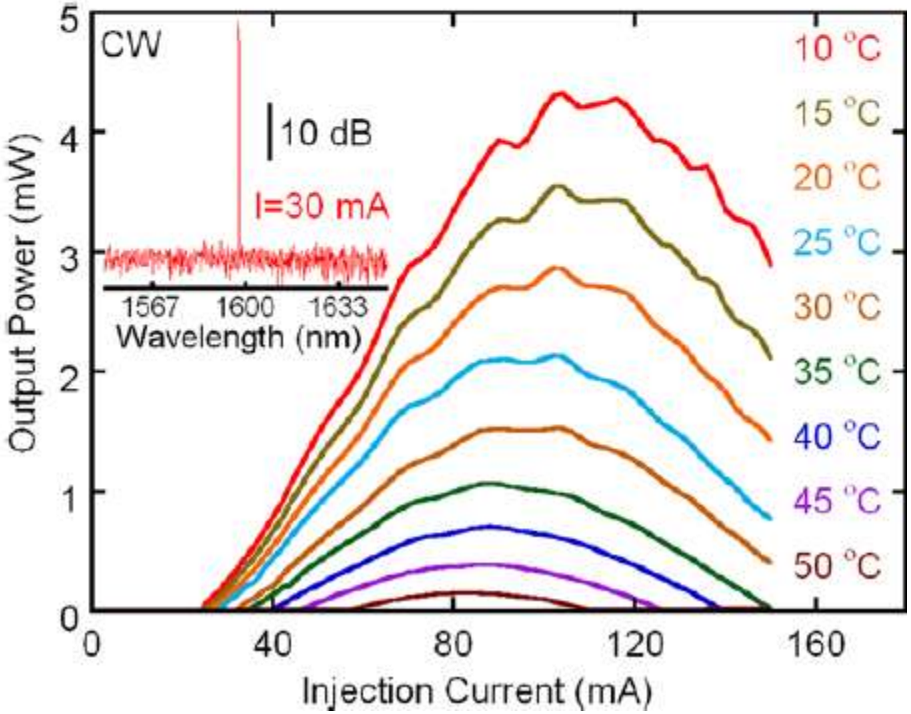


(a)



(b)

DFB-laser

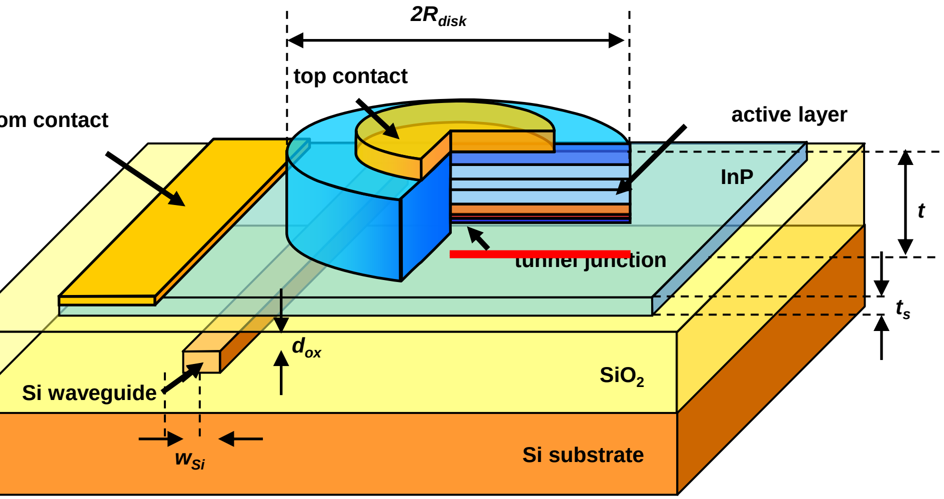


Also:

- DBR-laser, SGDBR-laser, EA-modulator, Detector, Disk laser

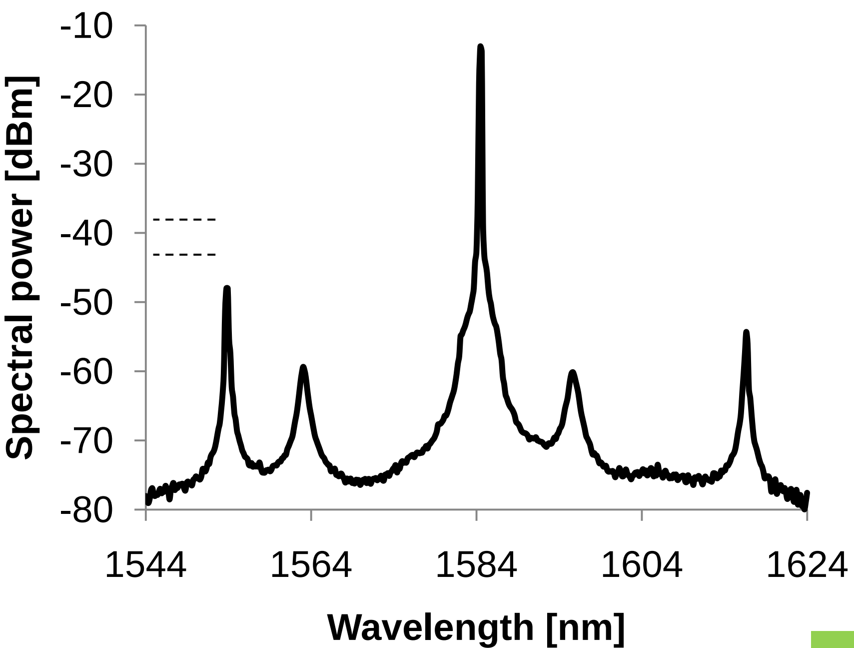
Liang, D. et al. Appl Phys a 95, 1045-1057 (2009).

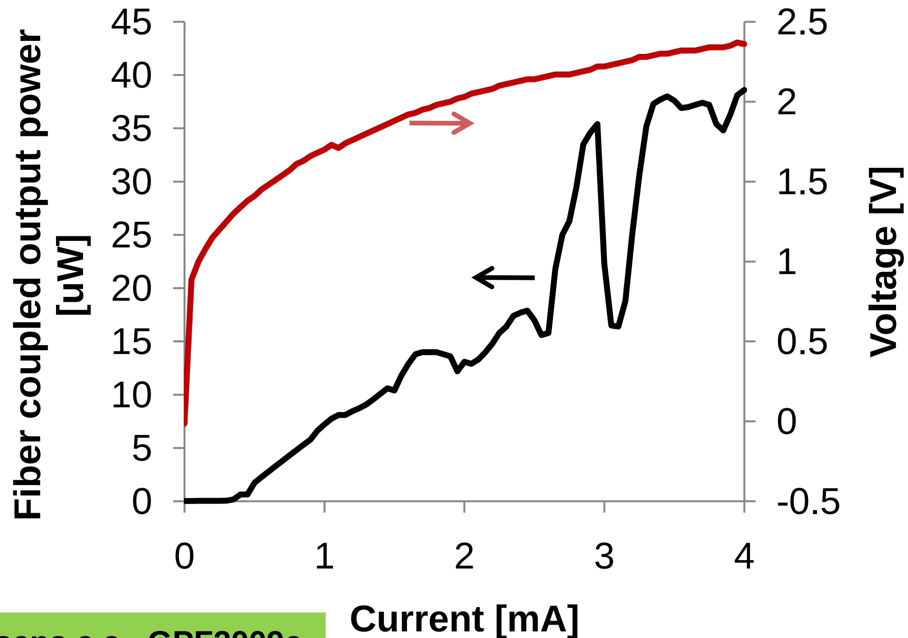
Microdisk laser



Microdisk laser

- Whispering gallery mode
- Evanescent coupling to silicon
- 150-350uA threshold
- 120uW output power (CW)



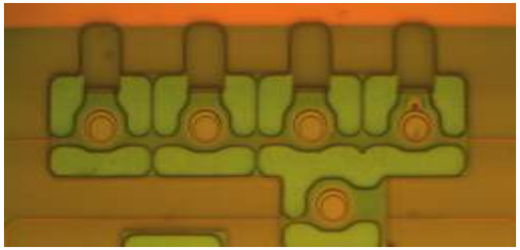


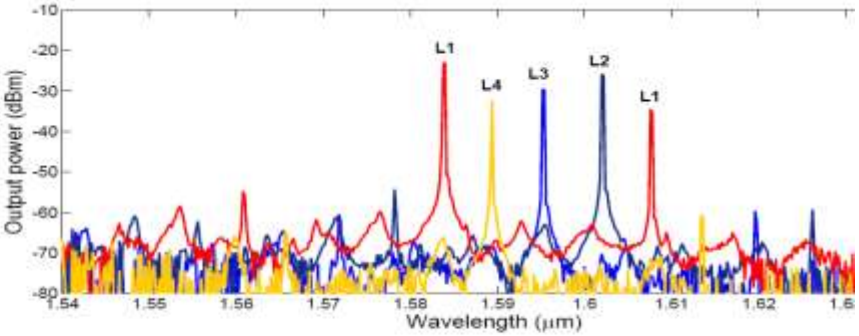
Spuesens e.a. ,GPF2009c

Microdisk device

Very flexible device

- Direct modulation
- Multi-wavelength source



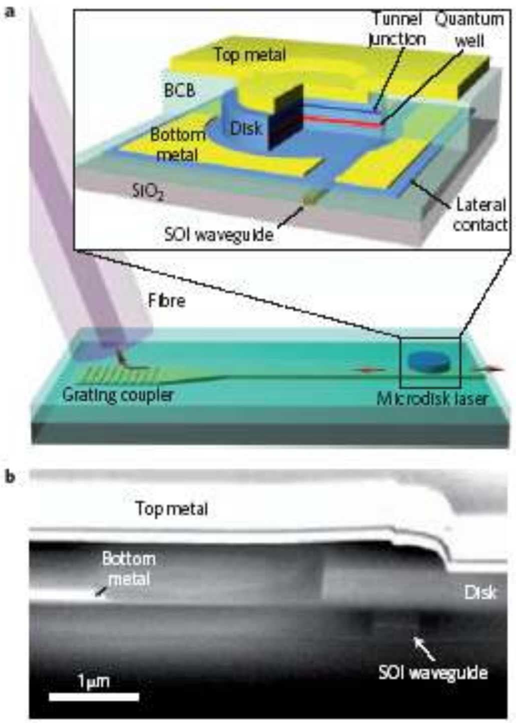


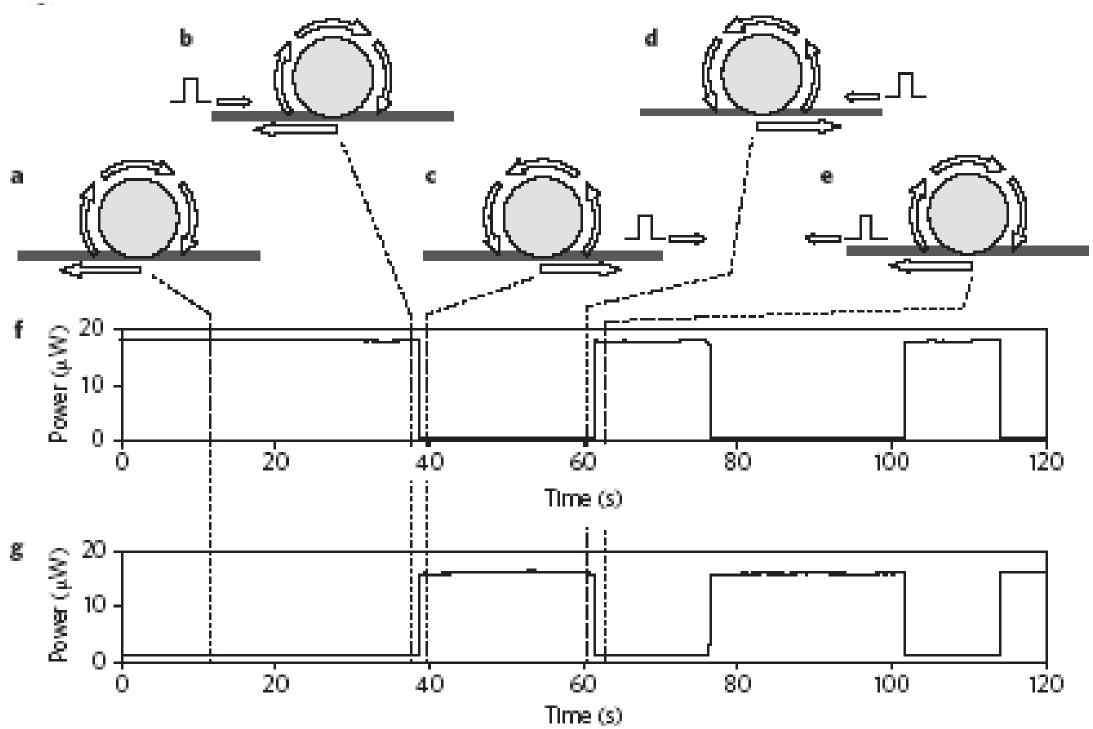
- 20GHz All-optical wavelength conversion — Raz e.a. ,OFC2010, paper OMQ5
- 10GHz All-optical gate — Kumar e.a. ,OFC2010, paper JWA44
- Electro-optic modulation — Liu e.a. , Optics Letters, 33(21), p.2518 (2008)
- All-optical switching
- All-optical flip-flop — Liu e.a. , Nat. Phot 2010 + Kumar e.a. , OFC2010, Tuesday

ARTICLES
PUBLISHED ONLINE: 24 JANUARY 2010 | DOI: 10.1038/NPHOTON.2009.268
nature photonics

An ultra-small, low-power, all-optical flip-flop memory on a silicon chip

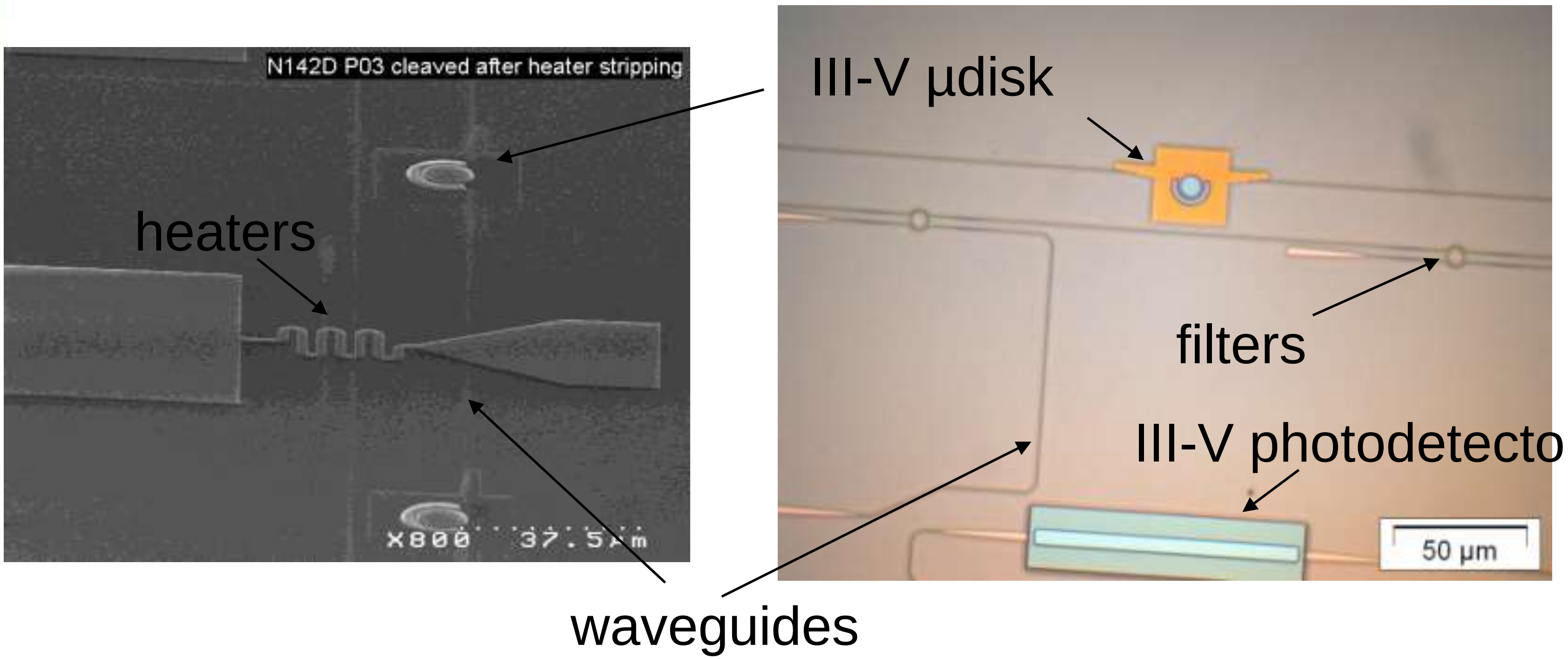
Liu Liu[1†], Rajesh Kumar[1], Koen Huybrechts[1], Thijs Spuesens[1], Günther Roelkens[1], Erik-Jan Geluk[2], Tjibbe de Vries[2], Philippe Regreny[3], Dries Van Thourhout[1], Roel Baets[1] and Geert Morthier[1]*





What's next ?

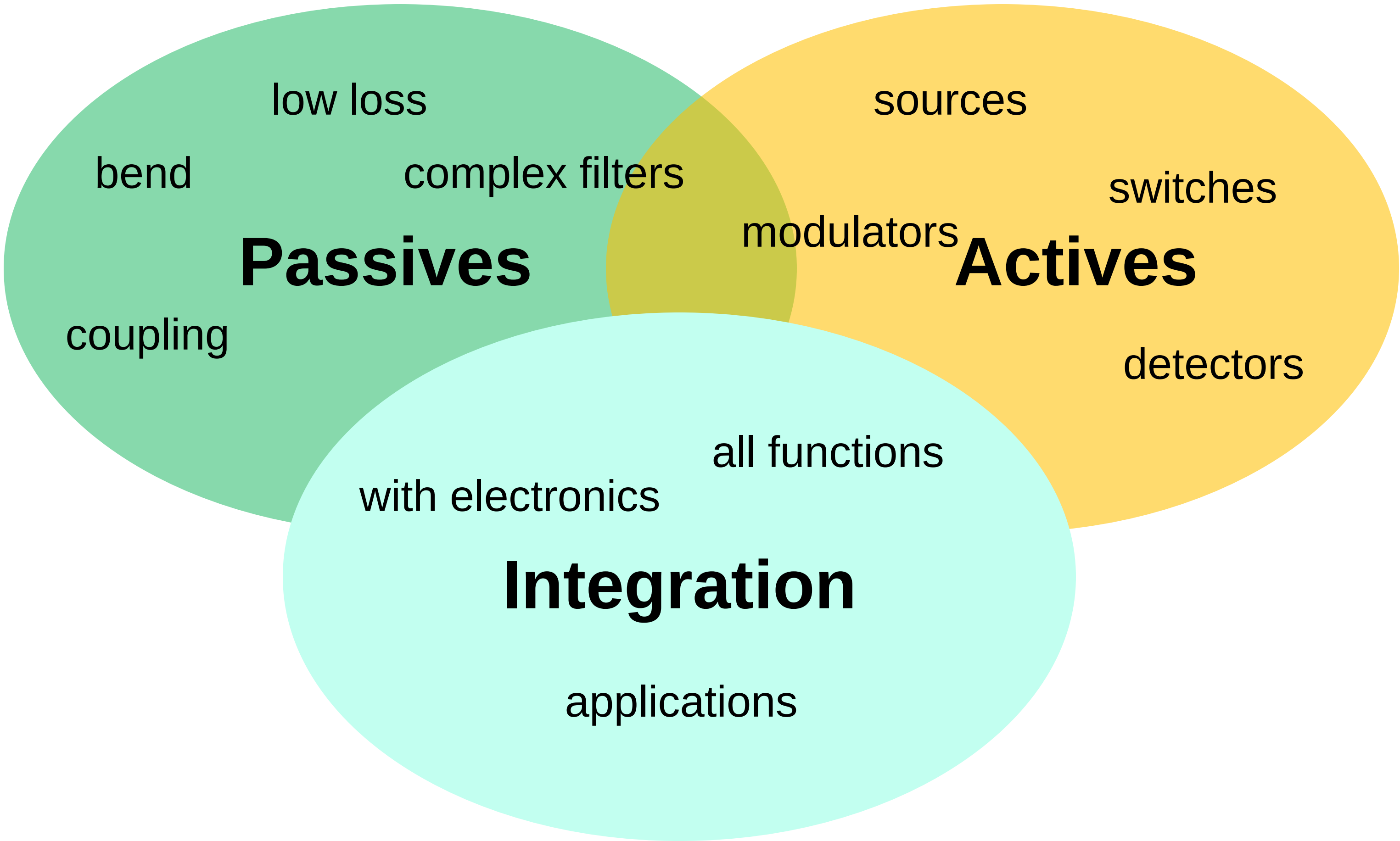
- WDM optical intraconnections on chip with a fully CMOS compatible process
(EU WADIMOS project http://wadimos.intec.ugent.be/)



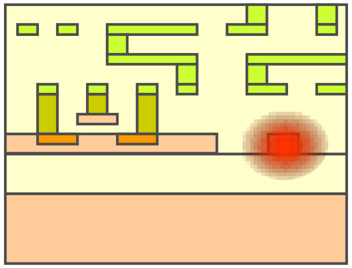
Now lasing !!!!!

© CEA 2009. All rights reserved
Any reproduction in whole or in part on any medium or use of the information contained herein is prohibited without the prior written consent of CEA

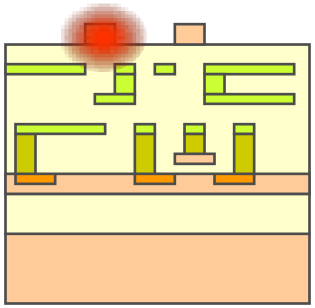
Outline


low loss
sources
bend
complex filters
switches
modulators
Passives
Actives
coupling
detectors
all functions
with electronics
Integration
applications

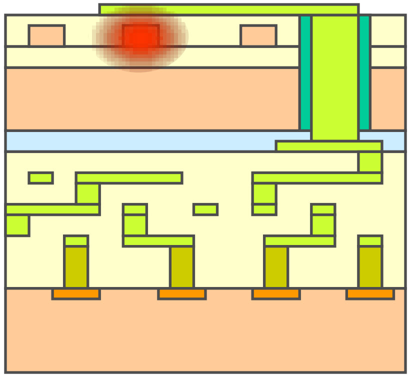
Monolithic vs. 3-D integration



- Front-end: no thermal budget
- Integrated in CMOS flow (on SOI only)
- High process development cost
- Compound yield
- Little flexibility
- Optical layer buried

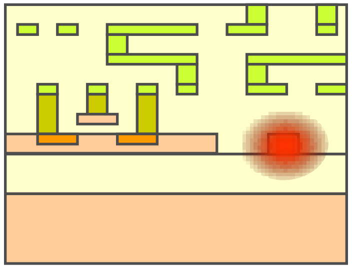


- Back-end: thermal budget < 400C
- On top of CMOS (or in metal layers)
- Serial process
- Compound yield
- Optical on top is possible



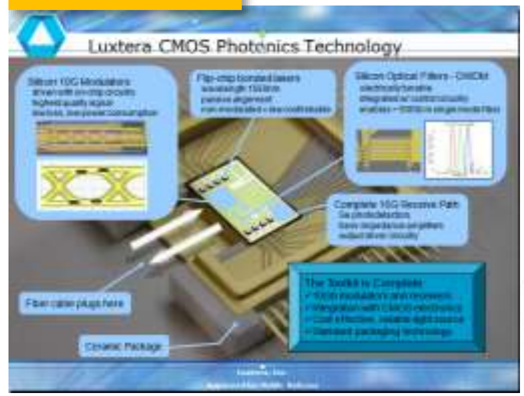
- 3-D: on top of CMOS
- No thermal budget
- Parallel process
- No compound yield problem with die-to- wafer stacking (known good die)
- Flexible choice of electronics and photonics
- Other layers possible: MEMS, antennas
- Optical layer on top is possible

Monolithic vs. 3-D integration

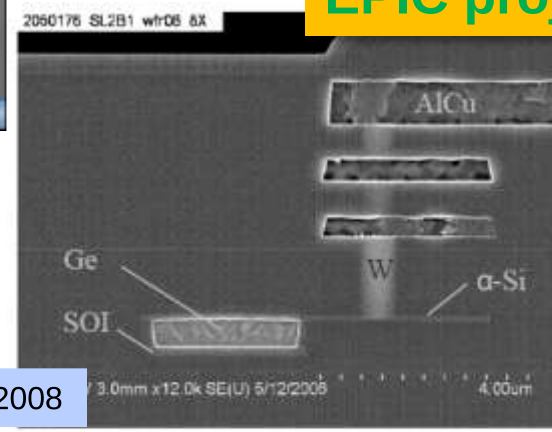


- Front-end: no thermal budget
- Integrated in CMOS flow (on SOI only)
- High process development cost
- Compound yield
- Little flexibility
- Optical layer buried

Luxtera

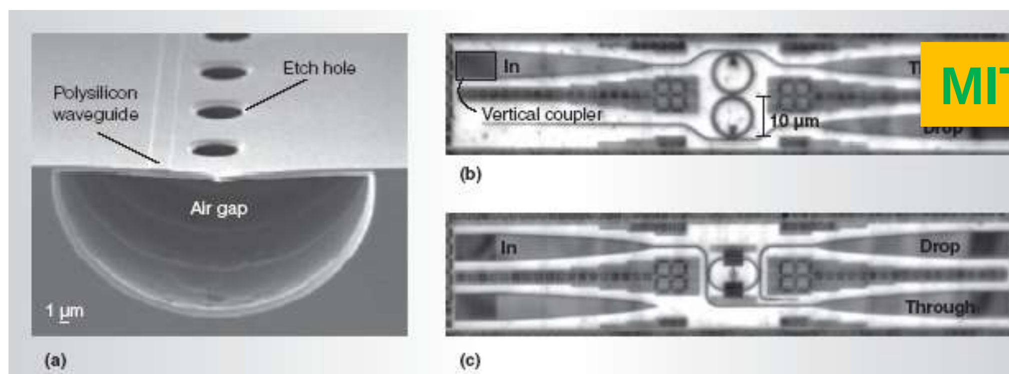


EPIC project



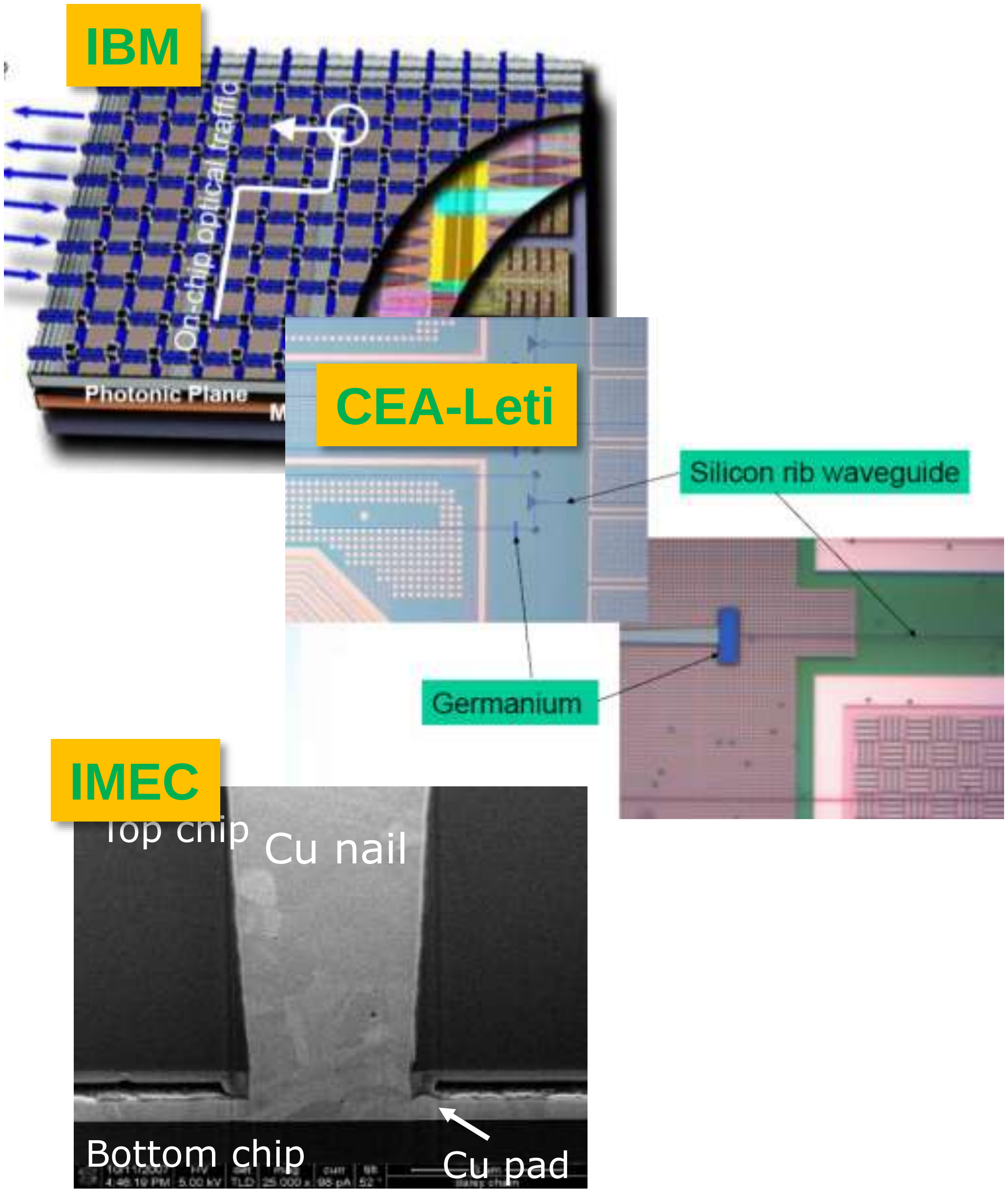
Beals e.a., SPIE Phot West 2008

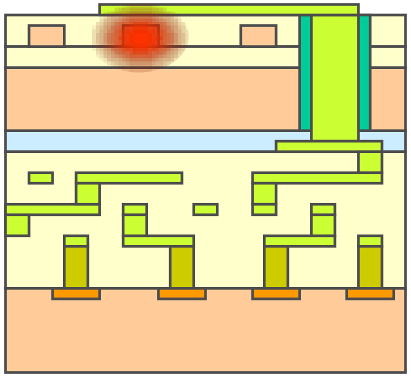
MIT



Batten, C. et al. in *IEEE Symp. on HP Interconnects 21-30Stanford, CA, USA; 2008).*

Monolithic vs. 3-D integration





- 3-D: on top of CMOS
- No thermal budget
- Parallel process
- No compound yield problem with die-to- wafer stacking (known good die)
- Flexible choice of electronics and photonics
- Other layers possible: MEMS, antennas
- Optical layer on top is possible

Comparison of IBM CMOS Nanophotonics with existing Si Photonics

Si CMOS Photonics

Others (Announced)

- ✓ 130nm design rules for CMOS
- ✓ 130nm design rules for Micro-Photonics
- ✓ CMOS FEOL integrated (Ge-last after activation)
- ✓ Large Litho variations - active tuning is required
- ✓ 6mm² per transceiver channel

Si CMOS Nano-Photonics

IBM (Announcing now)

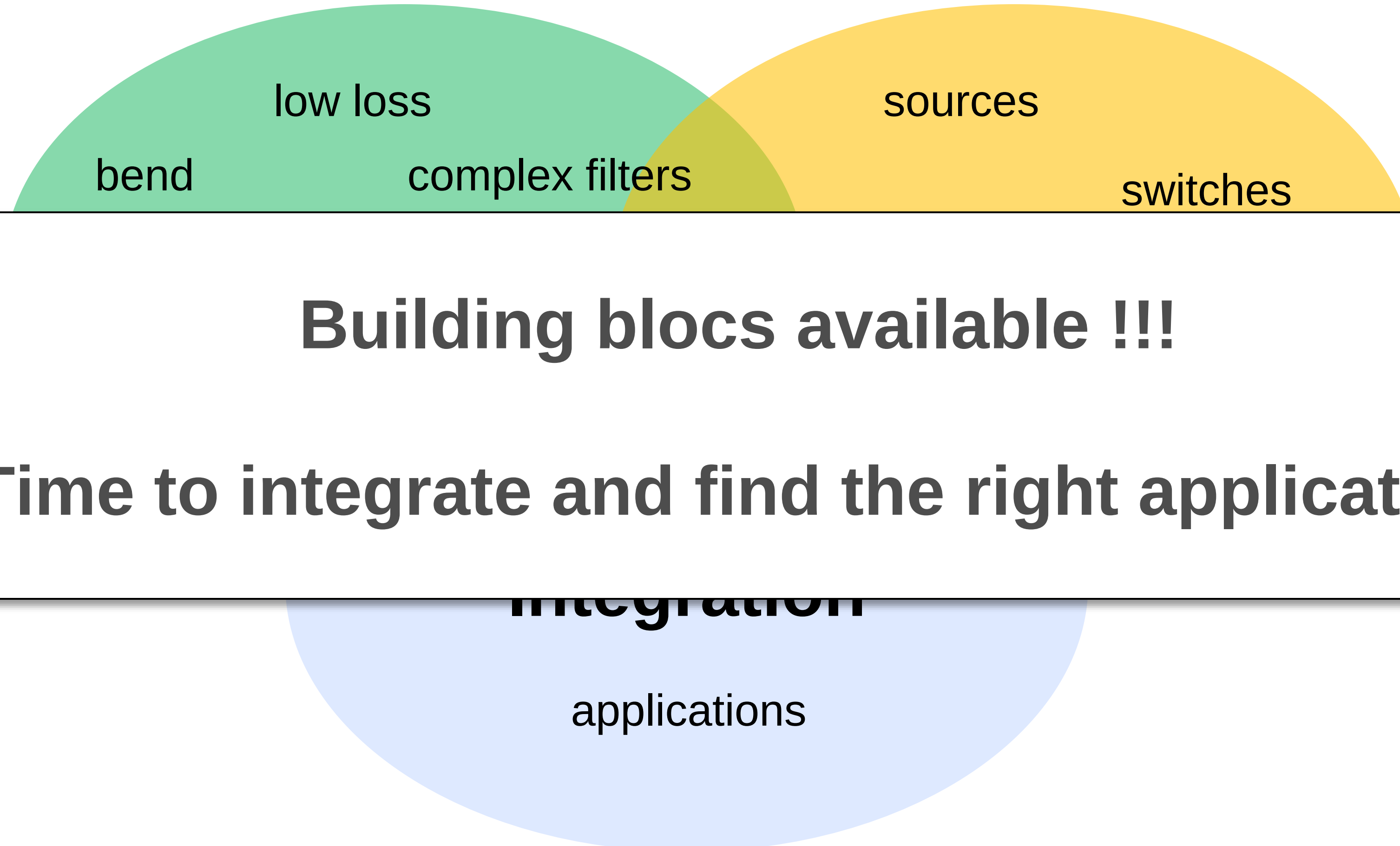
- ✓ 130nm design rules for CMOS
- ✓ 65nm design rules for Nano-Photonics
- ✓ CMOS FEOL integrated (Ge-first prior to activation)
- ✓ Small Litho variations - active tuning not required
- ✓ 0.5mm² per transceiver channel

IBM CMOS Nanophotonics technology:

- ➤ 10x higher integration density
- ➤ The only amenable for Terabit/s-class single-chip CMOS transceivers
- ➤ 50channels x 20Gbps = 1Tbps transceiver occupies only 5x5mm² of a CMOS die
  (can be smaller than 2x2mm² without pad frame and capacitors)

http://www.research.ibm.com/photonics

© 2010 IBM Corporation



Building blocs available !!!

Time to integrate and find the right application

ePIXfab

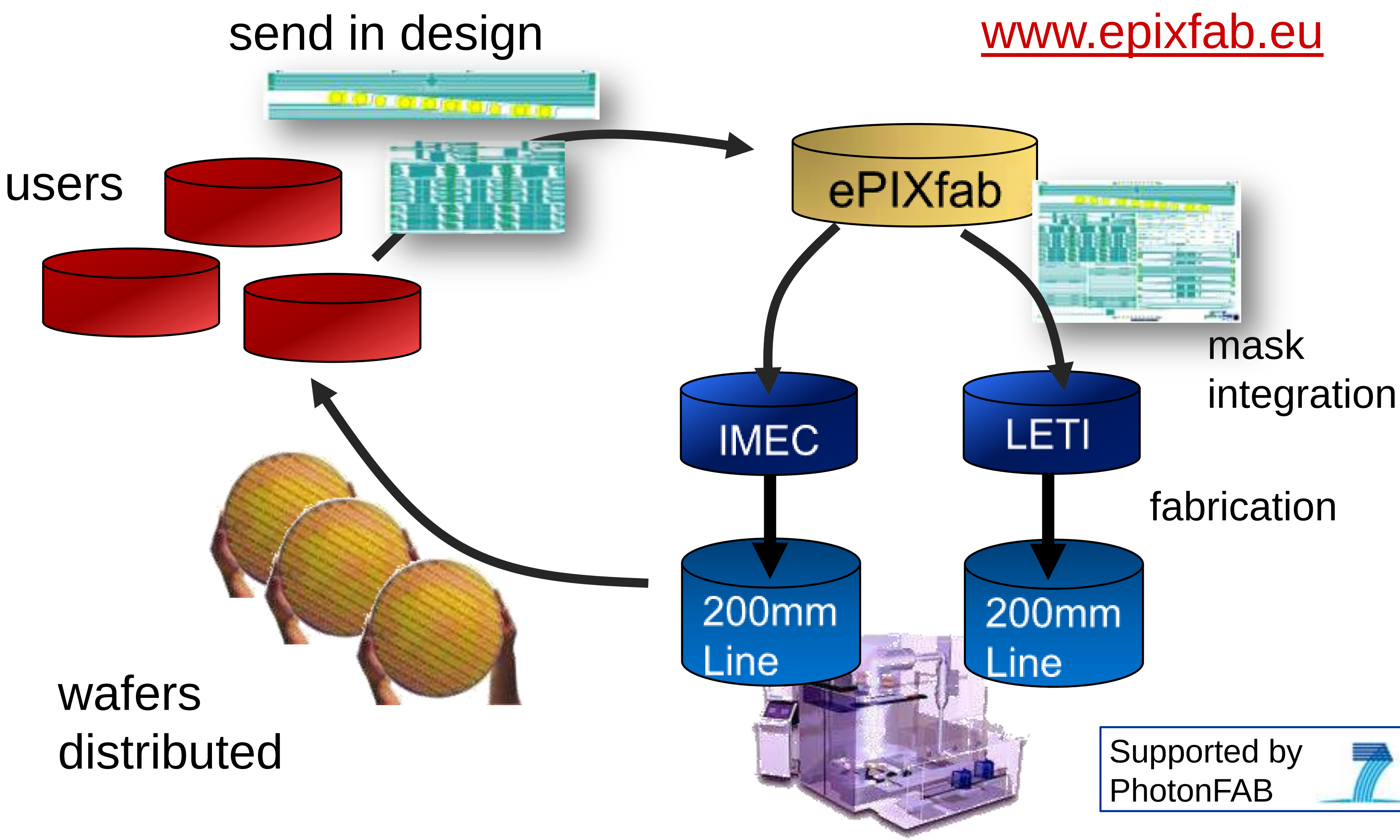
Silicon photonics in CMOS fab

- Cheap for volume production
- Expensive and difficult access for research and prototyping

Solution ? ePIXfab

- Multi-project wafer shuttles allow cost sharing
- Joint initiative of IMEC and LETI
- Supported by EU-commission
- Open for research and prototyping

ePIXfab: serving the research community



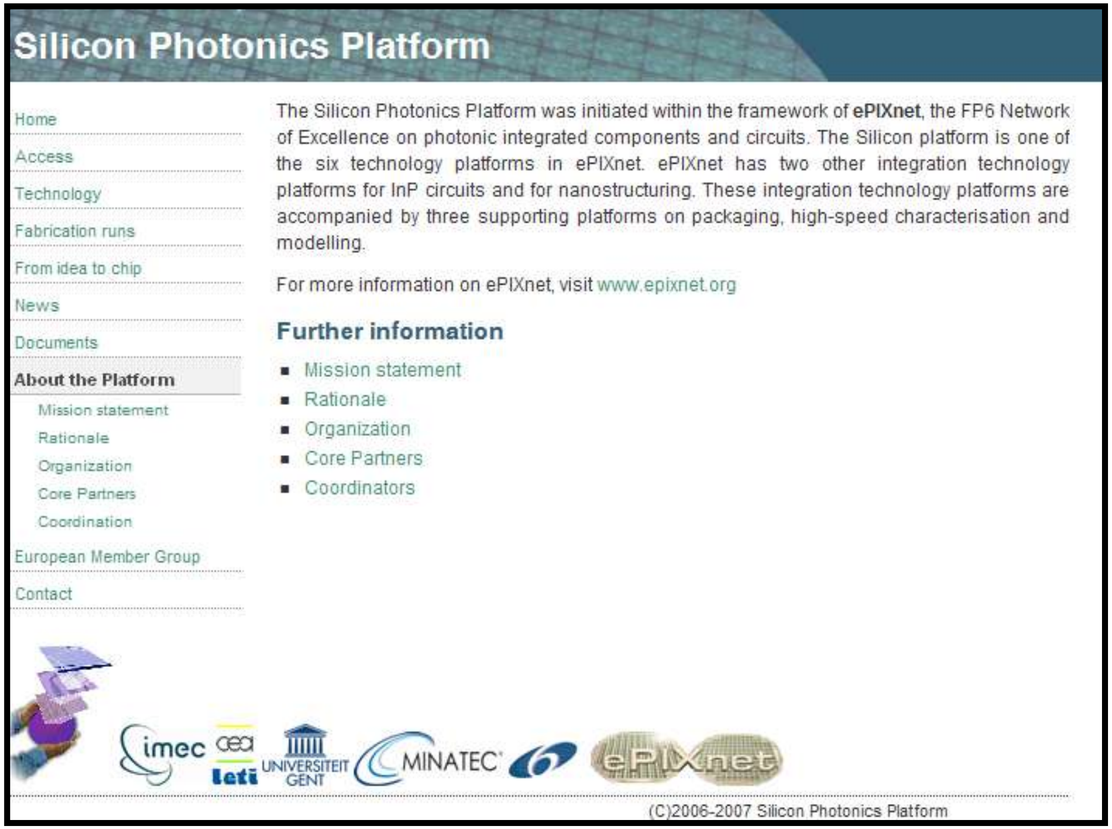
Supported by PhotonFAB

ePIXfab: Practical information

Visit our web site:

www.epixfab.eu or www.siliconphotonics.eu

- Information on calls
- Technical docs



Coordinator:

Pieter Dumon

pieter.dumon@imec.be

Acknowledgements

Thanks to

- Ghent University/IMEC Photonics Research Group
  - (in particular Wim Bogaerts who provided a lot of the slides)

- ePIXfab project for silicon fabrication
  - See www.epixfab.eu : also for YOU!!!
- Funding through national and EU research projects