All-Optical Wavelength Conversion at 160Gb/s Using an SOA and a 3rd Order SOI Nanowire Periodic Filter

C. Stamatiadis (1), K. Vyrsokinos (1), L. Stampoulidis (2), A. Maziotis (1), Z. Sheng (3), D. Van Thourhout (3), J. Bolten (4), M. Karl (4), T. Wahlbrink (4) and H. Avramopoulos (1)

1: National Technical University of Athens, 15773 Zographou, Athens, Greece, e-mail: cstamat@mail.ntua.gr
2: Constelex Technology Enablers, 17 Ikoniou Str, Acharnai, Athens, Greece, 13675
3: Photonics Res. Group, INTEC, Ghent Univ.-IMEC, Belgium
4: AMO GmbH, Aachen, Germany

Abstract: We present 160Gb/s all-optical wavelength conversion using an SOA and a 3rd order racetrack resonator integrated on a SOI nanowire platform. The scheme requires 0.5W of electrical power and the power penalty is <3 dB.

1. Introduction

Silicon-on-insulator has emerged as an integration platform that enables the CMOS compatible fabrication of ultra-compact photonic components. In this context a range of passive photonic structures – including micro-resonators – have been demonstrated implementing filtering and add-drop functionalities for WDM reconfigurable networks. These components are now being further applied to wavelength routing, dynamic, packet-switched networks, where a number of advanced wavelength selective functionalities are involved including all-optical wavelength conversion (AOWC) [1], switching [2] and buffering [3]. In the case of AOWC, the chirp filtering technique that relies on a single non-linear SOA followed by an optical band-pass filter (OBF) is most promising due to the low power consumption and the potential for ultra-fast (>100 Gb/s) operation. So far the scheme has been demonstrated using bulk OBFs, but now the employment of micro-resonators (MRs) to realize chirp filtering, can guarantee compactness and graceful scaling of high-capacity wavelength routing platforms. To this end we have recently demonstrated the first MR-assisted all-optical wavelength converter in a proof-of-concept experiment at 40 Gb/s using a medium index contrast substrate for the integration of ring resonators with a bend radius of ~50 um [1]. In order to reach ultra-fast bit rates, higher order resonators with very small bend sections would be required in order to obtain sharp filter profiles as well as round-trip times comparable to the ultra-short data pulse duration within the resonant cavity. In this rationale we demonstrate for the first time error-free AOWC at 160 Gb/s using a high order micro-resonator structure integrated on a high-index contrast SOI nanowire substrate. The SOI chip features a 3rd order racetrack resonator with each resonator having a bending section of 5 um and a total footprint of only 0.51 mm^2. We demonstrate effective recovery time acceleration of a 40 Gb/s SOA and measured a maximum power penalty of 3 dB for the 160 Gb/s converted signals. The electrical power consumption is limited to 500 mW.

2. Experimental setup

Figure 1(a) presents the experimental setup. The 160Gb/s transmitter consists of a 40 GHz Mode Locked Laser (MLL) emitting 2.2 ps sech pulses at 1553 nm modulated via a Ti:$LiNbO_3$ modulator at 40 Gb/s with a 2^7-1 PRBS. After multiplication at 160 Gb/s, this pulsetrain is combined with a CW signal provided by a tunable laser. The AOWC consists of an SOA and the third order SOI racetrack resonator. The SOA is a commercially available 40 Gb/s device with an 1/*e* nominal recovery time of 80 ps. The third order racetrack has been fabricated by Electro

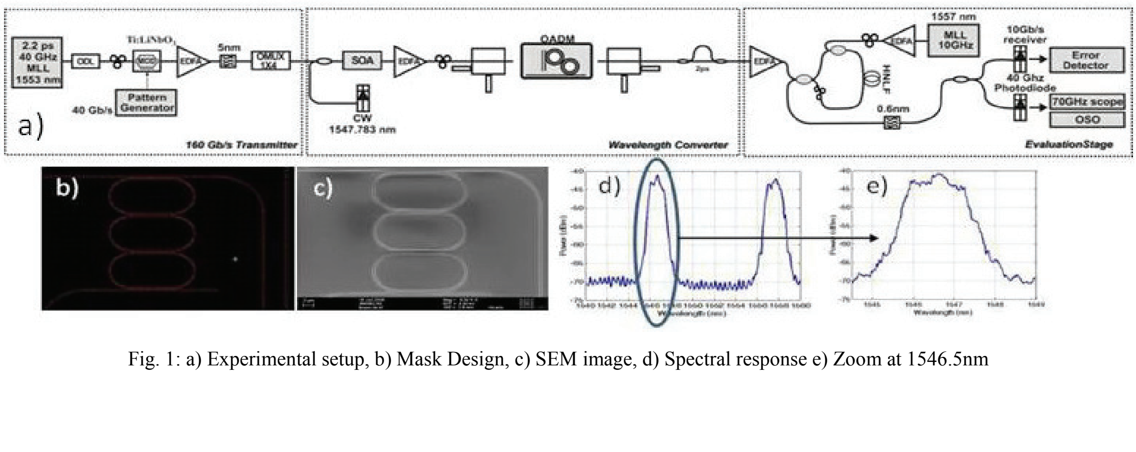


Fig. 1: a) Experimental setup, b) Mask Design, c) SEM image, d) Spectral response e) Zoom at 1546.5nm

978-1-4244-5369-6/10/$26.00

Beam Lithography and consists of three coupled resonators. The radius of the bending section of each racetrack was 5μm, while the length of the straight section was 8.5μm resulting to a total footprint of 0.51mm^2 and Free Spectral Range of 11.44nm. The dimension of the waveguides were 220nm x 450nm and the gaps between bus-racetrack and racetrack-racetrack were 156nm and 254nm. The peak that was chosen for blue chirp filtering was at 1546.5nm with 35dB out of band rejection and 1.3nm 3dB bandwidth. The CW detuning for the inverted signal was 1.2nm while for polarity inversion a Delay Interformeter (DI) with 2ps differential delay was employed. The high-rate wavelength converted signal was demultiplexed at 10Gb/s using a Sagnac interferometer. For the control signal a 10GHz MLL was utilized emitting 1.5ps pulses at 1557nm.

3. Results and discussion

Figure 2(a) depicts the eye diagram of the incoming 160Gb/s signal. Fig. 2(b) illustrates the 160Gb/s inverted wavelength converted signal recorded with an Optical Sampling Oscilloscope at the output of the racetrack resonator when the CW wavelength is detuned to 1547.783nm. The open eye diagram and the absence of intersymbol interference reveals the ability of the resonator to reject the red-chirp “slow” spectral components and accelerate the effective recovery time of the 40 Gb/s SOA within the 160 Gb/s bit-slot. A non-inverted 160 Gb/s waveform is obtained at the output of the DI. The eye diagram of the demultiplexed wavelength converted signal is shown in Fig. 2(d). Figure 2(e) illustrates the spectrum of the inverted signal at the output of the periodic filter, while Figure 2(f) shows the spectrum of the non-inverted signal after the DI where carrier suppression has been achieved. Error free operation has been demonstrated for all 16 channels with 3dB power penalty, as shown in Fig. 2(g). The optical power requirements were 3.75dBm for the CW and -0.65dBm for the data signal. The AOWC requires approximately 0.5W of electrical power to operate, including both SOA bias and TEC.

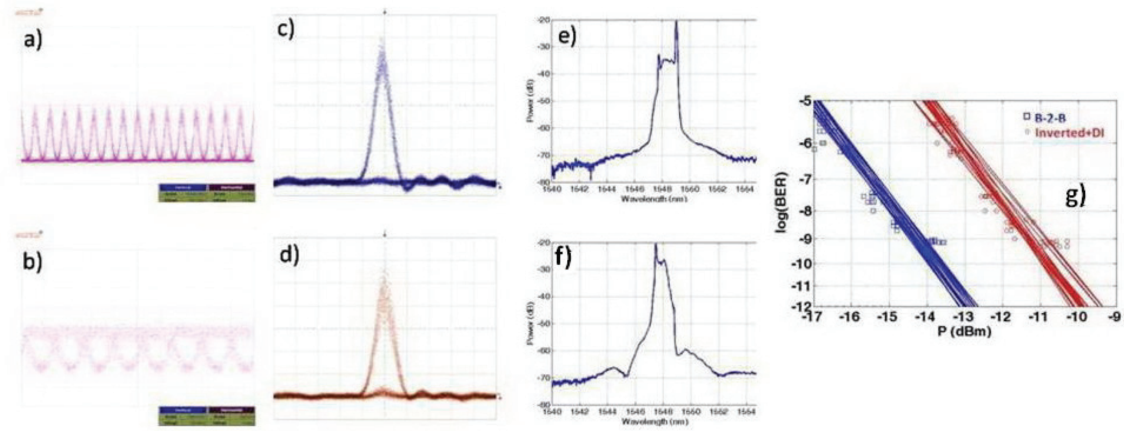


Fig. 2: Eye diagram of a) Input 160Gb/s, b) Inverted 160Gb/s WC signal, c) B2B 10Gb/s demultiplexed signal, d) Non-Inverted 10Gb/s demultiplexed WC signal after DI. Spectrum of e) Inverted Signal, f) Non-Inverted Signal after DI. g) BER Measurements. Time scale: a)10ps/div, b) 5ps/div, c),d) 10ps/div

4. Conclusions

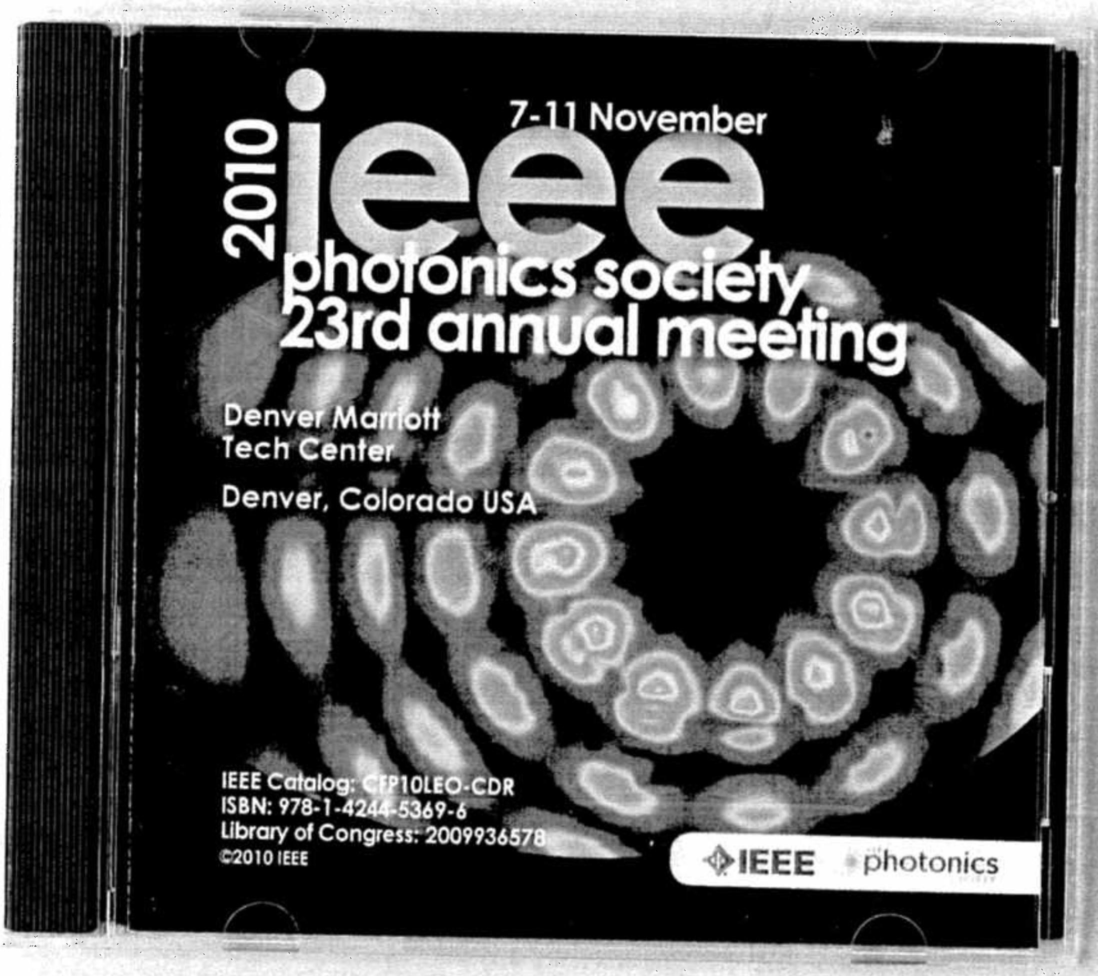
We have demonstrated 160 Gb/s all-optical wavelength conversion with power penalties of less than 3dB utilizing a single SOA and an integrated SOI periodic filter. The filter is implemented as a 3rd order racetrack resonator and consumes only 0.51mm^2 of a SOI wafer. The scheme requires 0.5W of electrical power which is decreased by a factor of three with respect to the power consumption of 40 Gb/s commercial all-optical wavelength converters.

Acknowledgement

This work was supported by the European Commission through ICT-BOOM project. The authors would also like to acknowledge PhoeniX BV for providing the simulation tools used for the design of the resonators.

References

[1] L. Stampoulidis et al, J. Lightwave Technol., **28**, 4, 476- 483 (2010)
[2] B. G. Lee et al., J. Sel. Topics. In Quantum Electron., 16, 1, 6-22 (2010)
[3] F. Xia et. al., *Nature Photonics* **1**, 65 - 71 (2007)


2010
ieee
7-11 November
photonics society
23rd annual meeting
Denver Marriott
Tech Center
Denver, Colorado USA
IEEE Catalog: CFP10LEO-CDR
ISBN: 978-1-4244-5369-6
Library of Congress: 2009936578
©2010 IEEE
IEEE
photonics