

## Heterogeneous integration of GaSb based photodetector on Silicon-on Insulator waveguide circuits for shortwave-infrared sensing applications

N. Hattasan<sup>1</sup>, L. Cerutti<sup>2</sup>, J.B. Rodriguez<sup>2</sup>, E. Tournié<sup>2</sup>, D. Van Thourhout<sup>1</sup>, G. Roelkens<sup>1</sup>

<sup>1</sup>Photonics Research Group-UGentimec, Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

<sup>2</sup>Université Montpellier 2 - CNRS, UMR 5214, Place Bataillon, 34095 Montpellier, France

*We report our work on the heterogeneous integration of GaSb-based epitaxy on silicon-on-insulator (SOI) waveguide circuits for shortwave-infrared sensing applications. We demonstrate the integration of p-i-n GaSb photodetectors on SOI waveguides. We use an evanescent coupling approach to couple light from the SOI waveguide to photodetector. The integration of active material onto SOI is based on die-to-wafer adhesive bonding using DVS-BCB as the bonding agent. Here, we present design, simulation results and fabrication details. The measurement results are also discussed.*

### Introduction

Spectroscopy is a well-known technique to examine composition and concentration of the substances by measuring and analyzing the transmission/absorption spectra. Several sensing applications in environment and biomedical field are realized by using this technique, where the system is used to detect bio-molecules or gases with their characteristic absorption lines in near and mid-infrared wavelength region. Nevertheless, such a system consists of source, detector and passive components that are bulky, expensive and unsuitable for many applications e.g. implantable sensors. Photonic integration offers an attractive economic solution with significant miniaturization.

Photonic integrated circuits with silicon-on-insulator (SOI) platform provide compact and cost effective solution due to the access to CMOS fabrication technology, which has steadily matured over the last decades. Hence, high quality SOI passive circuits can be easily designed and fabricated in wafer scale. Moreover, its high omni-direction refractive index contrast allows realization of the miniaturized photonic integrated circuits. Although SOI have several advantages, light generation is difficult due to its indirect bandgap transition. Heterogeneous integration of active devices and SOI integrated circuit is therefore needed to realize fully functional integrated circuit and speed up the development process. There are several techniques for integration, such as molecular bonding, metal bonding and adhesive bonding. In our work, we employ adhesive bonding technique using divinylsiloxane-benzocyclobutene (DVS-BCB) as a bonding agent [1]. This technique provides several advantages. For example, it does not require an ultra clean surface unlike the molecular bonding technique. Moreover, the DVS-BCB maintains good adhesion with some topography on both epitaxy and SOI wafer.

In this paper, we present our work on heterogeneous integration of p-i-n GaSb p-i-n photodetector on SOI waveguide circuit. The design of the device and fabrication process is described. The measurement results are also presented.

### Device designs

Figure 1a shows schematic of the integrated device. It consists of SOI waveguide and photodetector on top of the SOI waveguide. Light from SOI waveguide is evanescently coupled into photodetector waveguide when the phase matching occurs. Figure 1b shows simulation results of absorbed power dependence on the intrinsic region thickness of the photodiode. Clearly, the absorption efficiency is strongly dependent on the bonding thickness, i.e. on the phase matching condition. The simulation is done via CAMFR [2] which is based on frequency-domain eigenmode expansion techniques.

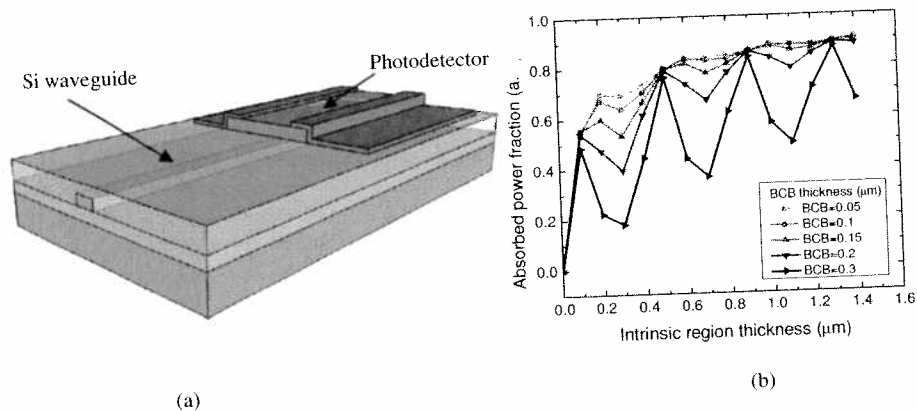


Figure 1: a) Schematic of the device b) Simulation results of the device where the absorbed power depends on intrinsic region thickness and BCB thickness.

### Fabrication process

The fabrication process starts with cleaning of both SOI and GaSb epitaxy. SOI is cleaned with standard clean-1 solution containing  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ . GaSb epitaxy is cleaned with acetone and IPA. For the heterogeneous integration, DVS-BCB is first diluted with mesitylene in 2:3 v/v. The SOI substrate then is spin-coated with DVS-BCB diluted solution at 3 krpm for 40s to obtain ~200nm bonded thickness. The sample is then baked at 150°C on a hotplate for 3 minutes to let mesitylene evaporate before transferring the GaSb die onto the SOI substrate. Bonding is performed at the same temperature, after which the sample is cured at 250°C for 1 hour. After the bonding process, the complete GaSb substrate is removed by using the combination of mechanical grinding and chemical etching using a mixture of  $\text{CrO}_3$ , HF and  $\text{H}_2\text{O}$  in 1:1:3 v/v at room temperature. InAsSb is used as an etch stop layer. This layer is later removed by selective wet etching with a 2:1 v/v citric acid and hydrogen peroxide mixture. The etching rate is ~100nm/minute [3]. The photodiode mesa is formed by using ICP-RIE (inductively coupled plasma reactive ion etching) with  $\text{CH}_4$  and  $\text{H}_2$  gas mixture. The etch rate is ~3.6 nm/minute. Figure 2 shows etching results of a dummy sample (GaSb substrate) with Ti as a hard mask. The sidewall roughness is relatively high, as seen in Fig. 2a. The etching profile is also shown in Fig. 2b. The slope is

estimated to be 101 degree. Ti/Au and NiGe/Au are used to form ohmic contact on both p and n-type GaSb, respectively. The photodiode island is defined by using wet etching in tartaric solution (tartaric acid/HCl/ $\text{H}_2\text{O}_2/\text{H}_2\text{O}$ ) with 0.5 $\mu\text{m}/\text{minute}$  etching rate [3]. DVS-BCB is used for device passivation. Figure 3a shows cross section diagram of the realized device with the detector on top of the SOI waveguide. Figure 3b is the SEM cross section image of the fabricated device. The etching profile is found to be similar to that of the dummy sample (Figure 2a). The bonding thickness of the device is estimated to be 265 nm

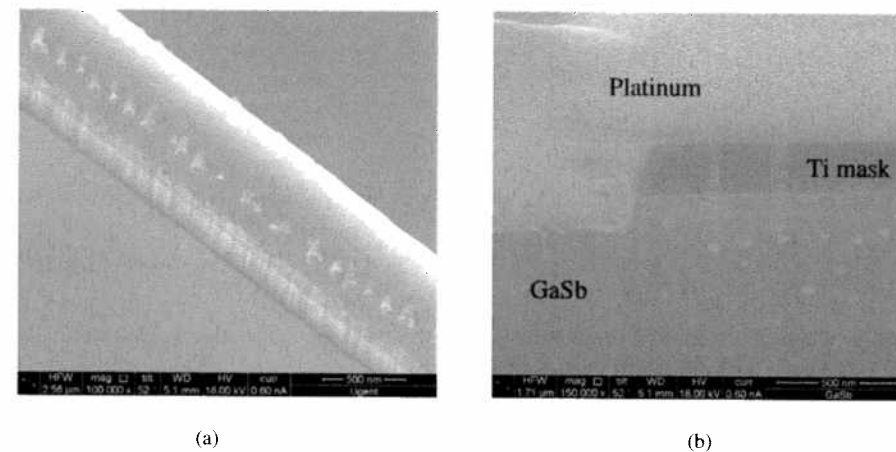


Figure 2 SEM image of dummy sample (GaSb substrate) (a) showing side wall roughness (b) showing etching profile

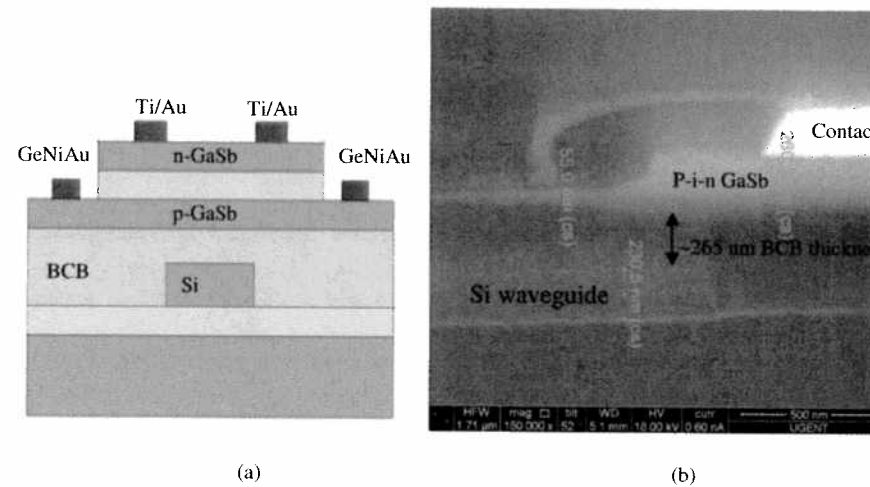


Figure 3 a) Cross section diagram of the realized device b) SEM image of the device

### Measurement Results

Figure 4 shows V-I characteristic measured at room temperature. The high leakage current is attributed to ICP etching which results in high roughness on the mesa sidewall. Light with varied input powers at wavelength  $1.57\mu\text{m}$  is coupled into the device via grating coupler to measure photoresponse. As depicted in Fig. 3, the device illustrates good photoresponse ( $\sim 0.4\text{A/W}$ ) as a function of the applied voltage.

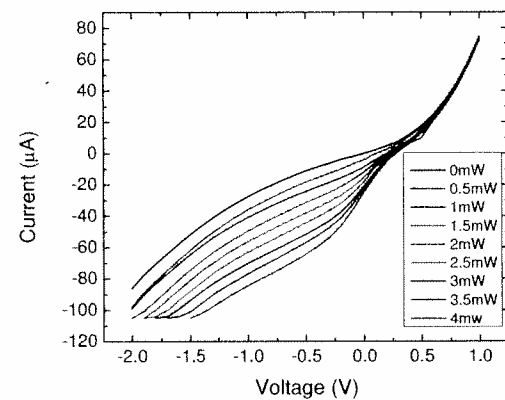


Figure 4 V-I characteristic of the device at different light input powers. The power level indicates output power from tunable laser.

In conclusion, we demonstrate the first generation of integrated p-i-n GaSb on SOI waveguide. It shows good responsivity of  $\sim 0.4\text{A/W}$ . Lower dark current can be obtained by optimizing the fabrication process such as chemical passivation. The successful demonstration of this device yields significant step toward shortwave-infrared integrated circuit.

### References

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## Lateral arrangements of size and number controlled $1.55\text{-}\mu\text{m}$ InAs quantum dots on InP nanopylramids

Jiayue Yuan, Hao Wang, René P. J. van Veldhoven, and Richard Nötzel

COBRA Research Institute, Department of Applied Physics, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands

*Lateral arrangements of size and number controlled InAs quantum dots (QDs) on truncated InP (100) nanopylramids grown by selective area metalorganic vapor-phase epitaxy (MOVPE) are reported. The QDs nucleate on high-index facets on pyramids top allowing precise position and distribution control. The size and shape of QDs are related to As/P exchange determined by the growth temperature, as demonstrated for circular-based pyramids. The QD number is controlled by both the size of the high-index facets (governed by pyramids top area) and As/P exchange (governed by growth temperature). Sharp emission peaks from individual QDs are observed around  $1.55\mu\text{m}$ .*

### Introduction

Self-assembled semiconductor quantum dots (QDs) represent a particularly intriguing and challenging class of quantum nanostructures for novel optoelectronic device applications [1, 2]. For advanced quantum functional devices, however, precise position and number control of QDs is required. The site-controlled QDs can be realized by pre-defined nucleation on truncated nanopylramids formed by selective area epitaxy [3, 4]. Here, we report the lateral arrangements of size and number controlled InAs QDs on truncated InP (100) nanopylramids grown by selective area metalorganic vapor-phase epitaxy (MOVPE). The QDs nucleate on high-index facets on the pyramids top allowing precise position and distribution control [3]. The size of the QDs is related to As/P exchange determined by the growth temperature, as demonstrated for circular-based pyramids. The QD shape transition from round to elongate is due to the increasing adatom surface migration length at the elevated growth temperature. The QD number is controlled by both the size of the high-index facets (governed by the pyramids top area) and As/P exchange (governed by the growth temperature). The sharp emission peaks from individual QDs are observed around  $1.55\mu\text{m}$ .

### Experimental procedure

A 100 nm thick  $\text{SiN}_x$  mask layer was deposited on the semi-insulating InP (100) substrates,  $2^\circ$  misorientated towards (110), by plasma-enhanced chemical-vapor deposition (PECVD). The openings in the  $\text{SiN}_x$  layer were created by electron beam lithography (EBL) and reactive ion etching (RIE). Figure 1 (a) shows the scheme of the  $\text{SiN}_x$  mask patterns for various pyramid base shapes: (I) diamond, (II) square, (III) circular, and (IV) elliptical. The openings were arranged in a square lattice with center-to-center distance of  $10\mu\text{m}$ . The side lengths or diameters of the openings were varied between 500 nm and  $1.5\mu\text{m}$ . Figure 1 (b) depicts the scheme of a square-based InP nanopylramid containing InAs QDs grown by selective area MOVPE. Trimethyl-indium (TMI), trimethyl-gallium (TMG), tertiarybutyl-phosphine (TBP), and tertiarybutyl-arsine (TBA), diluted in  $\text{H}_2$ , were used as source materials. The InP nanopylramids were grown at  $610^\circ\text{C}$  with a growth rate of  $18.39\text{ nm/min}$  in unmasked areas [4]. Three