HELIOS: pHotonics ELectronics functional Integration on CMOS

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ABSTRACT

Silicon photonics have generated an increasing interest in the recent year, mainly for optical telecommunications or for optical interconnects in microelectronic circuits. The rationale of silicon photonics is the reduction of the cost of photonic systems through the integration of photonic components and an IC on a

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common chip, or in the longer term, the enhancement of IC performance with the introduction of optics inside a high performance chip.
In order to build a Opto-Electronic Integrated circuit (OEIC), a large European project HELIOS has been launched two years ago. The objective is to combine a photonic layer with a CMOS circuit by different innovative means, using microelectronics fabrication processes. High performance generic building blocks that can be used for a broad range of applications are developed such as WDM sources by III-V/Si heterogeneous integration, fast Si modulators and Ge or InGaAs detectors, Si passive circuits and specific packaging. Different scenari for integrating photonic with an electronic chip and the recent advances on the building blocks of the Helios project are presented.

INTRODUCTION

Pioneered by Soref, silicon photonics has been developed since the beginning of the nineties. In Europe, early works were conducted both in France at IEF and in UK at the University of Surrey. Submicron silicon photonics have generated an increasing interest in the recent years, mainly for optical telecommunications or for optical interconnects in microelectronic circuits. At the beginning of the century, the focus was given on optical clock distribution for future microprocessor in order to break the red wall on clock distribution versus power. In about five years time, more European coordinated efforts has been launched but still with universities and research centers. The rationale of silicon photonics is the reduction of the cost of photonic systems through the integration of photonic components and an IC on a common chip (telecommunications applications), or the enhancement of IC performance with the introduction of optics inside a high performance chip (core to core communications), or low cost sensors (sensing applications). So different types of projects have been sponsored by the European commission and they addressed different devices demonstrations sharing the silicon photonics technology. In order to facilitate the use of the technology for research institutes and SME, an open silicon photonics platform named ePIXfab (http://www.epixfab.eu) was launched and it runs with fabrication calls alternatively in IMEC or in CEA-LETI. The HELIOS project (pHotonics ELectronics functional Integration on CMOS) was launched in May 2008 under the 7th Framework Programme (FP7) of the European commission. It gathers 19 European partners and aims at combining a photonic layer with a CMOS circuit by different innovative means. This 4-year project is coordinated by CEA-LETI and has been awarded a grant valued at 8.5 Million Euros (http://www.helios-project.eu).

HELIOS PROJECT DESCRIPTION

By co-integrating optics and electronics on the same chip, high- functionality, high-performance and highly integrated devices can be fabricated, while using a well-mastered microelectronics fabrication process. In addition, advances in CMOS photonics will move the emphasis from device component to architecture. Industrial and RTD efforts then could be focused on new products or new functionalities rather than on the technology level.
HELIOS will allow to combine a photonic layer with a CMOS circuit by using microelectronics fabrication processes. It will make CMOS photonics accessible to a broad circle of users in a foundry-like, fabless way. The objectives of the project are manifold:

- Development of high performance generic building blocks for a broad range of applications: WDM sources by III-V/Si heterogeneous integration, fast modulators and detectors, passive circuits and packaging
- The building and optimization of a complete production chain for complex functional devices. Integration of electronics and photonics in a single chip will be addressed not only at process level but also through the development of an adequate design environment
- Demonstrating the power of this CMOS photonics production chain through several complex photonic IC's that address different industrial needs. These include a 40Gb/s modulator, a 10x10 Gb/s transceiver, a Photonic QAM-10Gb/s wireless transmission system and a mixed analog and digital transceiver module for multifunction antennas.

• Investigating also some more promising but more challenging alternative approaches, such as silicon lasers and amorphous silicon modulators. These concepts offer clear advantages in terms of integration on CMOS for the next generation of Photonic IC's

• Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

One of the main challenging tasks of HELIOS is to analyze and compare the figures of merits of different full integration options as sketched in the Figure 1.

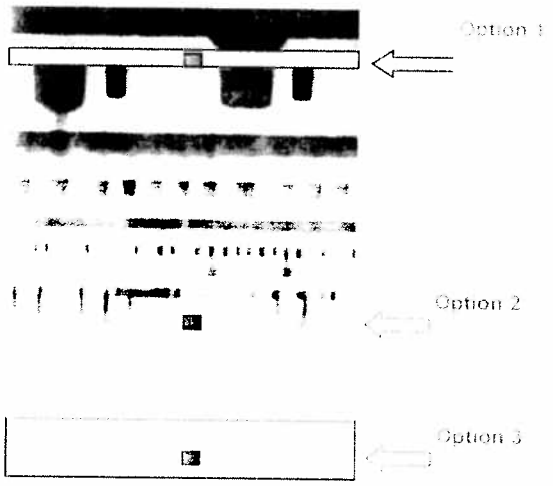

Figure 1: Different options for integrating the photonic layer addressed by the Helios project

Option 1: The photonic layer is build on top of the EIC at the last levels of metallization. Thus high integration density due to AboveIC approach can be performed. Contrary to Option 2, multilevel process for silicon waveguide can be considered. It is open to any standard FE electronic technologies and full heterogeneous integration of III-V on Si is available. Depending on the devices to be processed two sub-options are considered:

• Option 1A consists in building the photonic layers with only low temperature processes <400°C. For example, low temperature deposition of amorphous layer or die-to-wafer bonding can be used.

• Option 1B consists in fabricating the photonic functions on a separate wafer, and then to bond it on the electronic wafer. In this approach, high temperature processes can be used for the fabrication of photonic functions (eg Si-based modulators, Ge-based photodiodes).

Option 2: A specific front-end technology which combines the processing steps for electronic devices and photonic devices is developed with a specific design library. III-V components can only be hybridized with Flip-Chip technology. Areas for electronics and photonics are separated which leads to moderate integration density. Metallizations are performed for both electronics and photonics devices.

Option 3: The use of the rear side of the Electronic Integrated wafer leads to high integration density as for option 1. However through substrate connections are mandatory. Same characteristics can be listed as for option 2 with a sub_option 3A with only BE technology and 3B with a wafer bonding step.

The combined fabrication corresponding to option 2 have already been successfully demonstrated at 10G by Luxtera using 130nm modified SOI technology form Freescale. The aim of the Helios project is to extend this option to 40G applications using a different IC technology.

Since the beginning of this century CEA-LETI and IMEC developed building blocks for the option 1. The technologies developed are either pure SiGe or heterogeneous with InP die bonding. The PICMOS project consortium demonstrated the first full optical link on a silicon wafer, but it could be easily replaced by a

electronic wafer. Very recently under the Wadimos project, we have demonstrated the lasing of InP laser coupled to SOI waveguide which were fabricated in a microelectronics environment see Figure 2.

For option 1B, on SOITEC optical SOI, we have processed a silicon rib network with cavities filled with Ge. Before etching openings in the oxide for electrical contact to the germanium photodetector, the optical wafer was carefully polished and bonded to a dummy CMOS wafer before substrate removal (Figure3). After this step, vias and metallization process steps can be performed with regular technologies.

Figure 2: IR image of lasing of Φ40μm μdisk laser coupled to a waveguide. The light is output via a surface grating coupler.

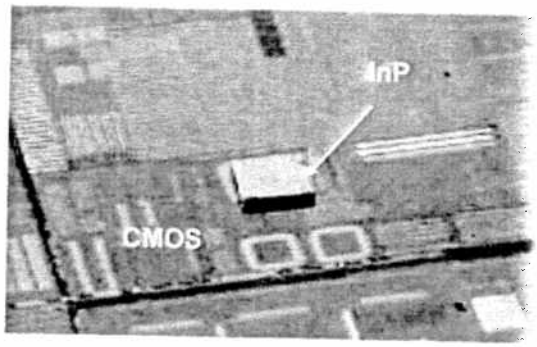

Figure 3: 1.2 x 1.2 mm², 200 μm thick InP die bonded on an optical layer on a dummy CMOS wafer

For option 1A, as long as temperature is constrained so that it must not exceed 400°C, a photonic layer can be defined above the transistors and the dielectric/metallic levels. The obvious way to introduce such a photonic layer is to treat it as an additional metallic layer on top of most of the layers that have been used for the electrical interconnect. For the passive parts, hydrogenated amorphous silicon waveguiding exhibited similar performances to monocristalline silicon with low temperature process. For the active parts, such as the introduction of copper for electrical interconnect, new materials like low temperature III-V compounds have be introduced on the wafers using decontamination procedures. After a CMP planarisation operation, MQW layers on InP die are mounted on top of the waveguides. The InP substrate of these die is then removed by chemical etching and further processing steps are performed which lead to sources and detectors connected to the metallic interconnects of the integrated circuit.

HELIOS TRANSMITTER BUILDING BLOCKS

The basic building blocks of a transmitter consist of a CW laser, a high speed modulator and a highly efficient coupler to a fiber. The results on modulation are described in paper 7719-2 on the proceedings of this conference. Main results are operation up to 15GHz with a high extinction ratio.

The heterogeneous integration of III-V materials by bonding consists in the transfer an III-V heterostructure from its original growth substrate to a silica surface. The III-V components are next fabricated on 200mm wafer using wafer-scale processing. This technique allows a high density of integration, collective processing and the use of high-quality III-V layers. The light can be directly coupled into a silicon waveguide underneath the III-V epitaxy. Most of the laser functions can be moved into the silicon part by designing the III-V layer only as a gain material while the cavity lies in the silicon region.
The III-V heterostructure (InP stack) are placed only at specific point by die-to-wafer bonding. The strong point is that it reduces the cost of the integration process since expensive III-V stacks can be bonded only where they are needed. Two main types of bonding are used in the literature: BCB and molecular bonding.

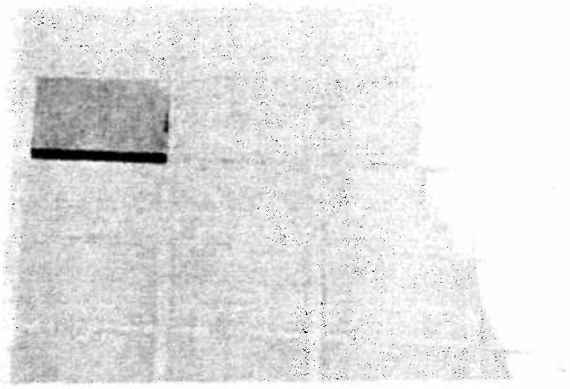

Figure 4: Image of an InP die on silicon photonics circuit with SiO2 molecular bonding

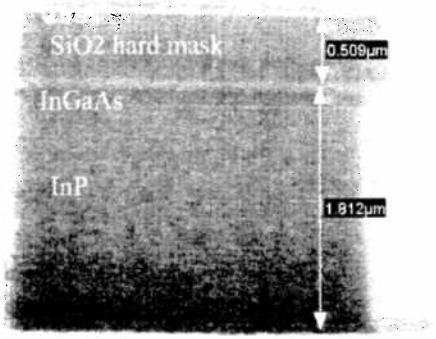

Figure 5: Etching profiles obtained on InP die bonded on 200mm Si wafer after a 15 min CH4/H2 plasma under RIE mode.

After molecular bonding seen on figure 2, mechanical grinding and InP chemical etching are performed in order to leave the thin heterostructure on the waveguide layer with a controlled SiO2 separation layer.

Decontamination steps of the rear side of the wafers are required before the introduction of the wafers in a microlectronics fab at the back-end level. With DUV lithography, fine patterns can be defined with high alignment (less than ±125nm) with the waveguide layer. Then etching of InP in 200mm format is performed using reactive ion etching (RIE) with CH4/H2 gases as the thin thickness of the hetrostructure requires low etching speed. Steep profiles with no trenching were observed, as illustrated in Figure 3. The plasma conditions also allow for the etching of InGaAs. InGaAsP, and AlGaInAs alloys.
The defined InP structures for SOA or laser are then cladded with a thick silica and the wafers are chemically polished in order to leave a thin layer of silica on top the laser diodes.
By opening the silica layers at different positions and different levels, contact with all the semiconductor layers and the last metallizations layers of the electronic circuit can be performed.

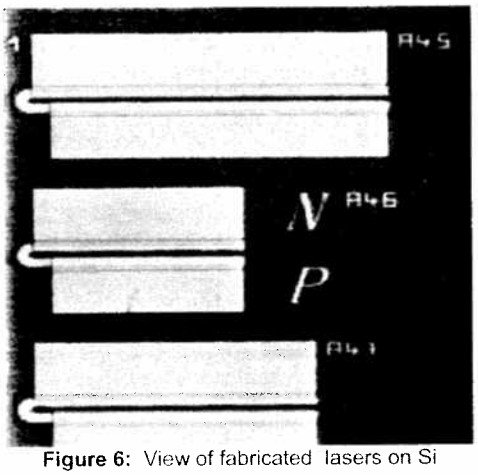

Figure 6: View of fabricated lasers on Si

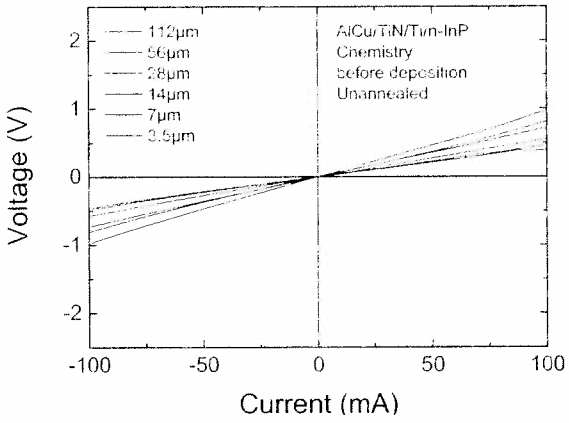

Figure 7: Voltage-current curves measured on the Ti/TiN/AlCu contacts deposited on n-InP dice on silicon Values correspond to the distance between TLM pads

CMOS compatible contacts on InP were developed as gold is forbidden is 200mm microelectronics clean room. Ti/TiN/AlCu stack was full sheet deposited at 200°C maximum temperature. After lithography step, the metal stack was dry etched with a chlorine-based chemistry down to the oxide which acts as a stop layer. No annealing was performed on the wafers.

The dies upper doped layer consists of either a 5x1018 cm-3 n-doped 500nm thick InP layer or a 3x1019 cm-3 p-doped 500nm thick InGaAs layer.
The specific contact resistance derived is 1x10-4 Ω.cm2 on n-InP and 6x10-5 Ω.cm2 on p-InGaAs. These values compare favourably with the gold-based stacks without annealing, and are sufficiently low to allow for

device fabrication. However in order to reduce heating, more efficient contacts are desired. With the same metallization, the electrical contacts are performed to take the contacts on the implanted area for modulators and on doped area for the Germanium PIN photodiodes. High performance lasers are obtained and are described in the paper 7719-50 of this proceeding.

Most grating couplers demonstrated over the last years have shown coupling efficiencies below 50%m (-3dB), or required complex fabrication techniques. In the framework of the HELIOS project, IMEC demonstrated a new grating coupler design with coupling efficiencies of nearly 70%, using an amorphous or poly-crystalline silicon overlay to create thicker grating teeth (Figure 8). The process can also be integrated with existing waveguide circuits, but requires additional processing steps. For relevant demonstrators, these fiber couplers will be used instead of the traditional couplers, and we aim to improve the coupling efficiency further by optimizing the design parameters (simulations show up to 85% is possible). This high-efficiency grating coupler showed a coupling efficiency of -1.6dB and a 3dB bandwidth of 80nm. The results have been published as post-deadline paper at Group IV Photonics, San Francisco, USA, 9-11 September 2009

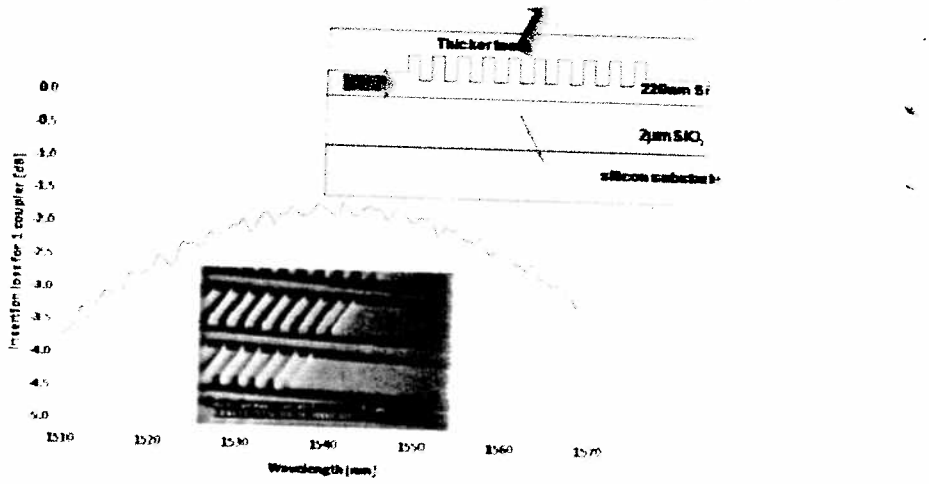

Figure 8: Schematic of improved 1D grating coupler

HELIOS RECEIVER BUILDING BLOCKS

On the receiver side, the main building blocks are a polarization insensitive coupler, a polarization diversity passive circuitry and high speed photodetectors. The passive circuitry has been extensively developed by the IMEC group at Ghent University and largely published [3,4]

Integrated photodetector is one of the main building blocks for silicon photonic applications for either monitoring or high speed detection. For this purpose, germanium (Ge) is exploited thanks to its strong absorption coefficient. A vertical pin Ge photodetector integrated in submicron SOI rib waveguide has been developed. As butt coupling configuration is considered, the detector length to totally absorb incident light at the wavelength of 1.55 µm, is reduced down to 15 µm (figure 9a). Such a waveguide detector, reported in figure 9b uses a process fully compatible with CMOS technology. The responsivity as high as 1 A/W under -4V and a dark current density as low as 60 mA/cm^2 has been obtained. An open eye diagram at 40 Gb/s under -4V is presented in figure 9c. For more information see reference [2].

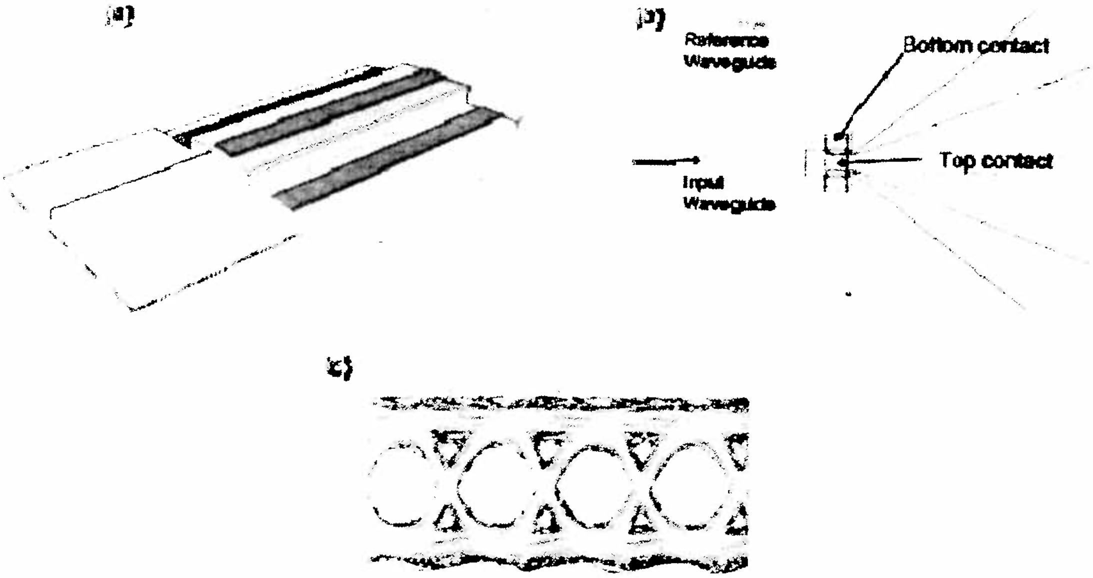

Figure 9: (a) Schematic view of vertical pin Ge-on-Si diode integrated in rib waveguide. (b) Top view of waveguide Ge photodetector. (c) Open eye diagram at 40Gbit/s.

To achieve a dense and efficient integration, light has to be strongly confined in submicrometer-size waveguides that exhibit a large refractive index contrast (typically $\Delta n \sim 2$) between the silicon-core and the cladding silica. As a consequence, light coupling from the outside world into photonic circuits is made somewhat difficult because of the poor overlap between the waveguide and fiber modes. Another drawback is the polarization management: in their topology, silicon waveguides are generally highly birefringent, and in the other hand, polarization in fiber-based networks is unpredictable and varies randomly with time. The design of an interface building-block which enhances light-coupling for all polarization states is therefore a critical issue.

Grating couplers are obviously good candidates to transfer the power flow from fibers into waveguides, but they still suffer from a low optical bandwidth and high polarization dependence. To overcome this polarization dependence a two-dimensional approach has been proposed [4]. The 2D-grating consists of a square-lattice of air holes partially etched into the top silicon membrane of a SOI wafer. This photonic-crystal like coupler also acts as a polarization splitter and it has recently been implemented in polarization-diversity devices [3]. Although this type of device still presents a low coupling efficiency (~20%), further improvements are expected under HELIOS development.

An alternative approach, already extensively discussed in the literature, is to use a spot-size converter that gradually transforms a highly confined waveguide mode into a wider mode supported by a low-index-contrast waveguide (such as polymers, or oxides) and that properly matches a tapered or cleaved lensed fiber [5-6].

The design [7] consists of a tapered nano-wire collector embedded in a low index contrast injector that adiabatically transforms the (lensed-) fiber mode into a highly confined mode. The coupling mechanism is based on a phase-matching condition between the fundamental modes of the SOI waveguide and of the SiOx injector.

The fabrication is based on microelectronics technology. A silicon strip waveguide having a width of 500 nm and a thickness of 220 nm is tapered down to 80nm by means of DUV-193nm lithography and RIE etching techniques. The linear variation of the waveguide widths is carried out on a length ranging between 200μm and 300μm, depending on the device designs. A 3.5μm-thick layer of silicon-rich oxide (SiOx) is then deposited. The amount of silicon nano-crystals is tailored to obtain a refractive index around 1.6, i.e. close to that of the fiber cores. Then, the thick layer is partially etched (1.5μm) to form a rib-waveguide shaped injector. The unit is finally encapsulated with a 1μm-thick silica layer.

Optical characterizations are performed with two single-mode tapered lense fibers with a mode field diameter of 3μm use for the injection and collection of the optical signal that propagates in a device composed by a Si strip waveguide with inverted taper couplers on both extremities. The transmission characteristic includes the losses at the facets between the fiber and the SiOx injector, the mode-conversion losses toward the silicon wire, and the waveguide propagation losses which are negligible in our study. The coupling efficiency of one coupler is obtained from this measurement, assuming that the input and output couplers are identical. Additionally, a tunable polarizer has been implemented in the optical setup to investigate the polarization behavior of the couplers. The experimental results are shown on Fig. 10. The coupling efficiency remains high in a broad spectral range: the bandwidth at 1dB is around 100nm (> 300nm at 3dB) for both TE/TM polarization states. The increase of the cross-section of the injectors was performed in order to achieve an efficient coupling with cleaved single-mode fibers (MFD~10μm). First results showed low insertion losses around 4dB.

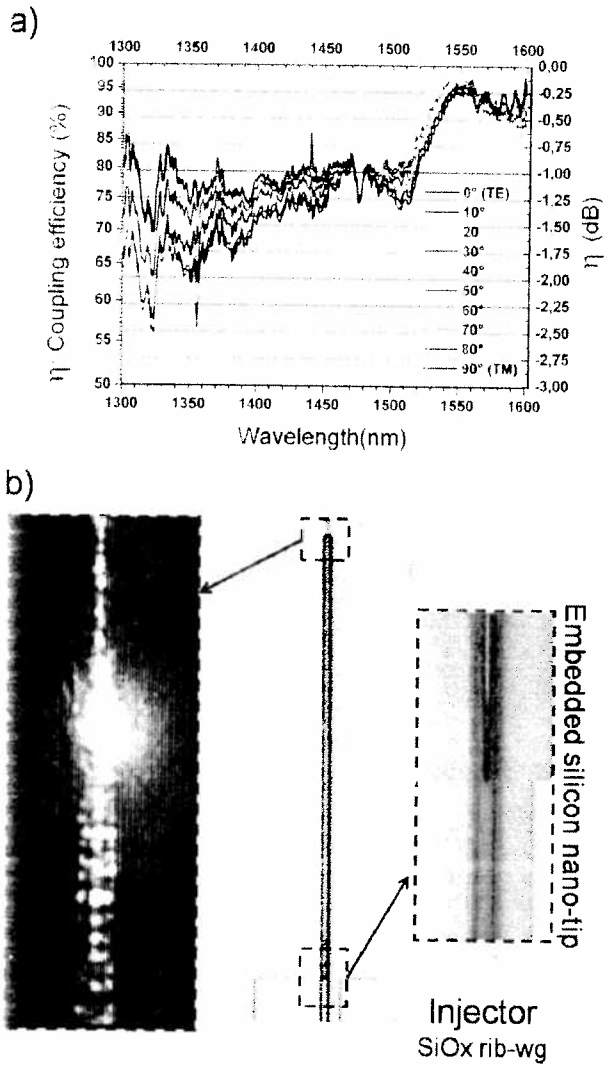

Figure 10: a) Coupling efficiency measured as a function of the injection angle. b) Optical images of the couplers associated with an infrared picture (taken at 1300nm) showing the end of the coupling transition

CONCLUSION

A photonics electronics integration [1,7] was sketched and some of the key process highlighted. The building blocks developed in the Helios project will be assembled in order to achieve the different foreseen demonstrators (high speed modulator, WDM transceiver, QAM system). Already 15GHz modulator and 40G Ge photodetector have been achieved and less than 2dB loss couplers have been demonstrated either with 1D surface grating or inverted taper coupler have been demonstrated. Moreover InP on Si laser fabrication with 200mm processing in microelectronics clean room have been achieved for applications with embedded laser.

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REFERENCES

[1] J. M. Fedeli, L. Di Cioccio, D. Marris-Morini, et al., "Development of Silicon Photonics Devices Using Microelectronic Tools for the Integration on Top of a CMOS Wafer," Advances in Optical Technologies, vol. 2008, Article ID 412518, 15 pages, 2008. doi:10.1155/2008/412518 (2008)

[2] L.Vivien & al, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide" Optics Express 17 (8), 6252-6257 (2009)

[3] W. Bogaerts, D. Taillaert, P. Dumon, D. Van Thourhout, R. Baets, E. Pluk, "A polarization-diversity wavelength duplexer circuit in silicon-on-insulator photonic wires, " Opt. Express, vol. 15, no 4, pp. 1567-1578, 2007

[4] D. Taillaert, H. Chong, P. Borel, L. Frandsen, R. M. De La Rue, and R. Baets, "A compact two-dimensional grating coupler used as a polarisation splitter," IEEE Photon. Technol. Lett., vol. 15, no. 9, pp. 1249–1251, 2003.

[5] V. R. Almeida, R. Panepucci and M. Lipson, "Nanotaper for Compact Mode Conversion", Opt. Lett., vol. 28, no. 15, pp. 1302-1304, 2003.

[6] T. Shoji, T. Tsuchizawa, T. Watanabe, K. Yamada and H. Morita, "Spot-size converter for low-loss coupling between 0.3um square Si wire waveguides and single mode fibers", in Proc. 15th Annu. Meeting IEEE LEOS , vol. 1, pp. 289-290, 2002.

[7] B. Ben Bakir, A. Vazquez de Gyves, R. Orobtchouk, P. Lyan, C. Porzier, A. Roman, and J-M. Fedeli ," Low loss (<1dB) and Polarization-Insensitive Edge Fiber Couplers fabricated on 200 mm Silicon-on-Insulator wafers", to appear in PTL.

[8] Silicon photonics II edited by D. Lockwood and L. Pavesi Topics in Applied Physics (Springer Verlag 2010)

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