# Photonics-CMOS 3D integration: copper through-silicon-via approach

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*Three-dimensional (3D) Integration using copper through-silicon-vias (TSV) is an emerging approach for heterogeneous integration of different technologies (MEMS, memory etc) with standard CMOS. This approach, which involves vertical interconnections with TSVs, is especially relevant for powering and controlling active optical devices (electrical and thermal tuning, modulators, switches, photodetectors etc) for silicon based photonic integrated circuits. We compare this integration approach with available alternative methods and describe our progress in developing a generic process for Photonics-CMOS 3D Integration using Copper TSVs.*

## Introduction

Recent growth in silicon photonics is mainly fueled by the capabilities of the electronic chip industry to fabricate inexpensive silicon photonics components using standard CMOS fabrication infrastructure [1]. Physical limitations of metallic interconnects is seen as the next critical problem in the development of modern information systems. One of the proposed solutions is the merger of electronics and photonics into an integrated multifunctional platform fabricated using the existing CMOS fabrication infrastructure [2].

3D Integration is an emerging, system level integration in electronics industry where many layers of planar devices are stacked and interconnected using TSVs [3]. 3D integration facilitates the heterogeneous integration of different technologies (like MEMS, memory etc) with electronics [4].

We are adopting IMEC's expertise in 3D Integration processing technologies for performing 3D integration of a photonics layer with an electronics layer. This paper briefly sums up the concept of 3D integration for photonics, and our latest progress in the development of a generic 3D integration process for photonics-CMOS integration.

## 3D Integration vs Other Approaches

There are many different approaches for photonics-CMOS integration. Most of the integration approaches can be divided into two broad categories: monolithic integration and hybrid integration [5].

The monolithic approach involves fabricating electronic and photonic devices on a single wafer, with "2 Dimensional" interconnections. This allows for close integration and facilitates the inclusion of doping and electrical contacting. However, this approach requires integration of photonics and electronics processing capabilities in the same fabrication facility, and often demands modifications in the FEOL (Front End of Line; steps to form active devices) processes of CMOS and that makes it less generic. It also makes a shift to a newer technology costly, and limits the combination of a photonic

layer with different classes of electronics (low-power, high-voltage, high-speed etc). It has an adverse effect on density as photonics and electronics devices compete for die space. Compound yield due to special photonics processing is another major drawback. The other approach is heterogeneous integration where the photonic layer and CMOS layer can be fabricated separately, and then they can be integrated and packaged. This gives freedom to fabricate and optimize photonic and electronics devices independently before integration. Compound yield is not an issue as only known-good photonic dies are used in die-to-wafer stacking. However, this advantage is void when wafer-to-wafer stacking is used. A 3D integration approach, where Copper through-silicon-vias (TSV) are used as "3D Interconnects", includes all the advantages of heterogeneous integration. Furthermore, IMEC has gained substantial expertise in 3D integration processes, which can be utilized for photonics-CMOS integration.

## 3D Integration for Photonics

One of the most important potential benefits of the 3D integration approach is the possibility of heterogeneous integration of different technologies. Such heterogeneous integration gives multi-functionalities in a single integrated chip with reduced cost [6]. Taking cue from this, it can be deduced that 3D heterogeneous integration of a photonics layer with a CMOS layer can be looked upon as a solution for Photonic-CMOS integration.

The 3D integration approach at IMEC makes use of Cu TSV acting as interconnects between the two different layers stacked over one another. The FEOL and BEOL (Back End of Line; steps to connect active devices by multiple layers of metal) of the two layers are processed using the standard CMOS processes. The top metal layer of the bottom wafer is connected to metal pads. Cu TSVs are fabricated in the top layer during the BEOL process. It is followed by backside thinning where the bottom tips of the Cu TSVs are exposed. The top layer is then integrated with the bottom layer using a tacky polymer film in a way that the TSV bottom tips can be fused with the landing pads of bottom layer. Thermo compression method is used to integrate Cu TSVs with the landing pads. The further process is dicing and packaging of the 3D integrated chip.

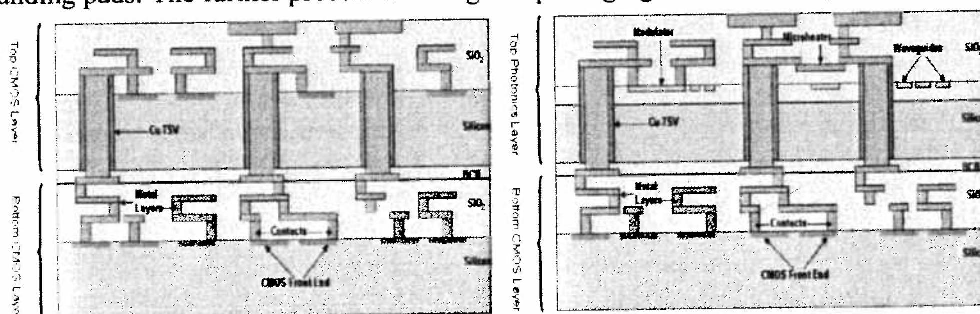


**Figure 1: Cross sectional diagram of 3D Integration of CMOS-CMOS and Photonics-CMOS**

Figure 1 shows the cross section of CMOS-CMOS and photonics-CMOS integration using TSV based 3D integration. For smooth adaption of this process for photonics-CMOS integration, the stack for the photonics must be similar to the CMOS. A generic process for fabricating SOI (silicon-on-insulator) photonic devices using standard CMOS processes has already been mastered by the Photonics Group at Ghent

University [7]. That ensures that a photonic layer with very similar layer stack as in the standard CMOS stack can be fabricated for smooth integration with CMOS layer.
The second image in Figure 1 shows integration of a photonics layer, with very few changes in stack, integrated with the CMOS layer at the bottom. Hence, the progress made in 3D integration can be easily adapted for photonics-CMOS integration.

## Fabrication Process

The first step in the 3D integration of photonics with CMOS is the finalization of standard layer stack composition for the photonics layer. In standard CMOS layers, the active devices are fabricated on a silicon substrate. It is then covered by a 50 nm liner of SiON through Plasma Enhanced Chemical Vapor Deposition (PE-CVD). This step is followed by deposition of Phospho-Silicate Glass (PSG) through High Density Plasma (HDP) CVD. PSG is a binary glass consisting of amorphous $SiO_2$ and $P_2O_5$. After deposition of PSG, Chemical Mechanical Polishing (CMP) polishes PSG layer to a uniform thickness above the active area. It is followed by PE-CVD deposition of a thin Oxide layer. After that, contacts and metallization layers are fabricated. A photonics layer differs from a CMOS layer in many respects. First of all, the photonics devices are fabricated on SOI, and not directly on a silicon substrate. In the CMOS layer, the building unit of all devices, the transistor, is made by doping and must be protected from mobile ions using special oxides like PSG. But most of the photonics devices are largely indifferent to mobile ions. Even optical modulators, which have doped regions, are not much prone to threats from mobile ions. That gives us the liberty to try different oxides available to us and chose the one which is best suited for optical purposes. To select the best oxide for optical purposes, optical tests were performed on several oxides, using propagation loss measurements with straight and spiral waveguides. Three different oxides which were tested were:

1. Shallow Trench Isolation (STI) Oxide (which is mainly used in FEOL processes)
2. Phospho-Silicate Glass (PSG)
3. Inter-Metallic Dielectric (IMD) Oxide (which electrically isolates the metal interconnect layers from each other)

The propagation loss in waveguides was characterized by coupling light from SLED into the waveguides and measuring the output power through grating fiber couplers. The optical losses for STI Oxide, PSG and IMD were found to be 4.48 dB/cm, 9.57 dB/cm and 2.79 dB/cm respectively at 1550 nm wavelength. The results clearly indicate IMD as the best oxide for optical purposes.
After choosing the oxide for the overlay layer, other stack layers were finalized. To accommodate SOI photonic structures and thermal tuning devices, some changes were made into the standard stack. To develop the etch recipe for TSVs with dimensions of about 5μm in diameter and 25μm deep, a dummy SOI was fabricated with the stack structure as shown in the first picture of Figure 2. The nitride ($Si_3N_4$) layer of 30 nm was included to accommodate the thermal tuner device which might be included in the device lots in the future. The thermal tuner will be in a 200nm IMD layer between nitride and silicon carbide (SiC). The silicon carbide layer will act as a stop layer for CMP during BEOL processes. This dummy SOI was then etched using plasma etching for Cu TSVs. The SEM image of the cross-section is shown in the second picture of Figure 2.

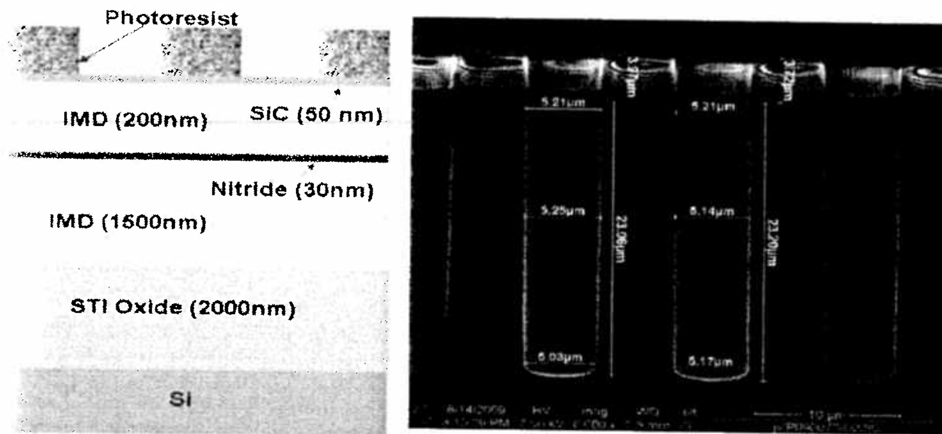


**Figure 2: Stack Structure for Photonics Layer; TSV Etches**

The etching looks satisfactory and similar to the standard TSV etch for standard CMOS stack. The walls are vertical and depth is uniform, which is a good sign for Cu TSVs which will form upon deposition of copper.

## Conclusions

The initial results for the 3D integration fabrication processes look encouraging. The modified stack did not pose any problem during the etching for TSVs and gave good results. Next step will be the deposition of Cu in TSV etched holes, which will be followed by the backside thinning and integration. The electrical and optical tests after the integration will allow to reach conclusive results about the success of the 3D integration approach for photonics-CMOS integration.

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