InP/InGaAs Photodetector on SOI Circuitry

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***Abstract*—We present the design, fabrication and characterization of an InP-based membrane photodetector on an SOI wafer containing a Si-wiring photonic circuit. Measured detector responsivity and 3 dB bandwidth are 0.45 A/W and 33 GHz, respectively. The photonic device fabrication is compatible with wafer scale processing steps, guaranteeing compatibility towards future generation electronic IC processing.**

***Index Terms*—Optical Interconnects, InGaAs/InP, Photodetector.**

I. Introduction

GOING towards smaller device dimension, higher signal switching frequency and higher bandwidth requirements, Si electronic integrated circuits (ICs) are expected to suffer a bottleneck at the interconnect level. Electrical interconnects (EIs) are predicted to limit the maximum bandwidth that can be achieved for both on-chip and off-chip links in future Si ICs [1]. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution, providing bandwidth increase, immunity to electromagnetic noise and reduction in power consumption [2], [3], [4]. A migration from EIs to optical interconnects (OIs) is currently underway for short-reach off-chip applications, such as server backplanes and multirack machines interconnects [5], and recent studies demonstrate the benefits of photonic ICs for on-chip applications as well [6].

In this paper, we present an InP/InGaAs photodetector (PD) suitable for OIs on electronic ICs. The photonic device is processed on an InP-based layer stack flip-chip bonded on a silicon-on-insulator (SOI) wafer containing Si photonic waveguides. The PD fabrication steps are compatible with wafer scale processing steps, to guarantee compatibility with the manufacture of electronic ICs. Photodetector design, fabrication and characterization are presented in this paper.

II. Design and Fabrication

The PD structure is defined on top of the bonding layer, as shown in Fig. 1, and consists of two parts: an InP membrane input waveguide meant to couple the light out of the Si photonic wire on the SOI wafer, and a p-i-n junction, where the optical power is absorbed. The InP and the Si waveguides act as a synchronous coupler: the light is coupled from the Si wire into the transparent InP waveguide and it is then guided to the absorbing detector region stacked on top of the transparent layer. The PD structure is built as an n.i.d. 700 nm InGaAs absorption layer sandwiched between a highly p-doped 50 nm InGaAs contact layer and a highly n-doped 250 nm InP layer, which is also used for realizing the membrane waveguide, and has a footprint of 5×10 μm^2. We chose a total detector thickness of 1 μm in order to meet a trade-off between device efficiency and speed. Due to the type of PD illumination and the compact device geometry, the bandwidth is mostly limited by the photocarrier transit time in the diode depletion region: an expected 3 dB cut-off frequency response of around 30 GHz is expected for this device [7]. Concerning the internal quantum efficiency, simulations show that all the optical power is absorbed within 7 μm. However, about 20% of the power is absorbed in the contact layers and in the metal stack. The light absorbed in this region is lost, as it does not contribute to the generated photocurrent. Therefore, an efficiency around 80% is expected.

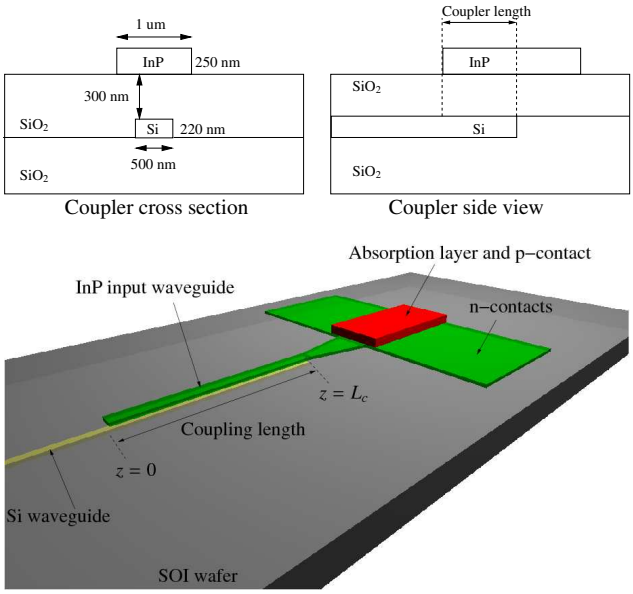

Fig. 1. Photodetector structure. The coupling from the Si photonic waveguide layer to the PD is realized by means of the InP membrane input waveguide, on top of which the detector is stacked. Front and side cross sections of the coupler are shown in the insets.

The detector input InP coupler was designed to achieve mode matching with the Si photonic waveguide, which is 500 nm wide and 220 nm thick (see Fig. 1). We fixed the InP waveguide thickness to 250 nm, which leads to a predicted optimum waveguide width and length of 1 and 14 μm,

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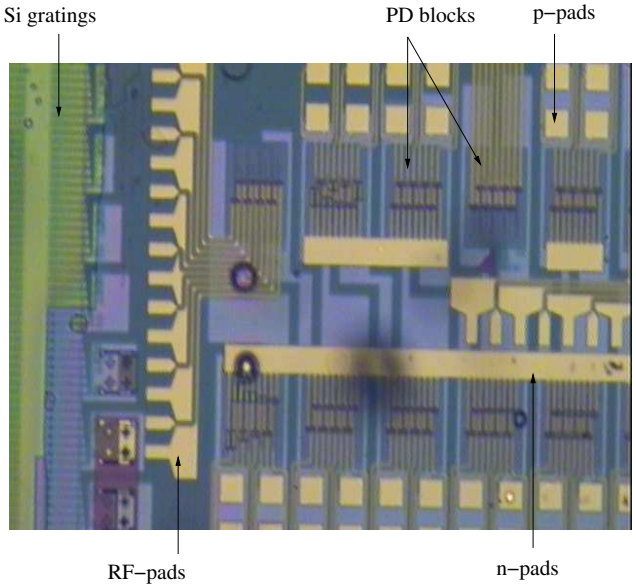

Fig. 2. Picture of the fabricated chip. The photodetectors are grouped in blocks of 8 devices. Metal coplanar waveguides interconnect the RF pads to the diode contact layers. Some of the PDs are contacted with DC pads, also indicated in the figure. On the left side, the Si FGCs used for fiber-to-waveguide light coupling are indicated.

respectively, for which simulations show that 100% coupling efficiency is achieved. For further details on the InP membrane coupler design, fabrication and characterization, we refer to our previously published work [8]. The PD structure shown in Fig. 1 allows the fabrication of laterally tapered membrane waveguides, which provide an increase of the alignment tolerance between the waveguides without additional processing steps. Details about design and fabrication of the Si photonic waveguides were presented in [9].

The PD layer stack described in the previous section was grown on a 2" InP wafer. It was sawn in dies that were then bonded upside down on a processed SOI wafer, containing the Si waveguide structures, by means of SiO_2 direct molecular bonding [10]. The photodetectors were defined via a combination of wet-etching and dry-etching steps, as we describe in [7]. Fiber grating couplers (FGCs) were also integrated in the Si photonic waveguide layer for fiber-to-waveguide light coupling, necessary for the characterization of detectors. Such gratings can be seen in the left part of Fig. 2, which shows a picture of the fabricated devices, and a more detailed description can be found in [11].

III. Measurement Results

The device DC characterization was performed by using a tunable laser source (TLS) to illuminate the detector and a Keithley 2400 current/voltage source-meter unit to reversely bias the PD and to read out the generated photocurrent. First, the detector dark current at different applied bias voltages was measured. Dark currents around 1.6 nA were registered at -4 V. A TLS and a polarization controller were used to couple the light into the Si waveguide via the Si FGC, which is designed to work with TE-polarized light [12].

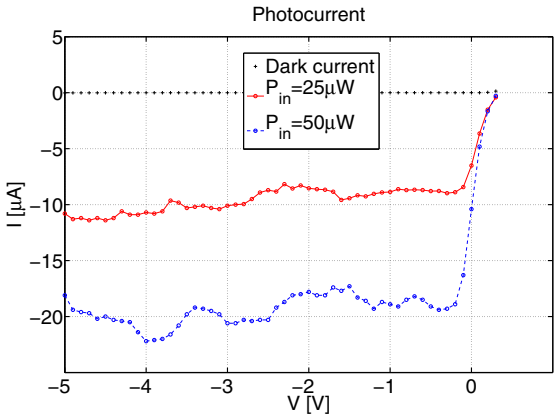

Fig. 3. Measured photocurrent for 0 μW, 25 μW and 50 μW optical input power as a function of the detector applied bias voltage.

The photodiode generated photocurrent as a function of the applied bias voltage was measured for the following TLS output powers: 0 mW, 0.2 mW and 0.4 mW. To evaluate the detector efficiency, the following factors were considered. Firstly, the fiber connections from the laser source to the polarization controller and to the coupling input fiber cause a loss of 0.7 dB. Secondly, the Si FGC is wavelength dependent and has 20% optimum coupling efficiency at $\lambda = 1575$ nm. Lastly, Si waveguide measured losses are 4-5 dB/cm, for TE-polarized light [9]. That leads to a loss of 1.3 dB along the Si waveguide length of 3.2 mm, from the grating coupler to the detector input. Taking those loss sources into account, the detector optical input powers corresponding to the TLS intensities mentioned above are 0 μW, 25 μW and 50 μW. The responsivity of the PD structure was thus calculated to be $R = 0.45$ A/W, which is a conservative value, as the grating coupler maximum efficiency was assumed. Such responsivity corresponds to a quantum efficiency $\eta = 35\%$, which includes the efficiency of the InP membrane coupler and the internal quantum efficiency of the pin-detector itself. Measurement results are shown in Fig. 3, which also demonstrates the linear behaviour of the PD response to the incoming input power.

Optical-to-Electrical dynamic measurements of the PDs were performed in the range of 100 MHz to 40 GHz with an Agilent HPN4373B 67 GHz lightwave component analyzer (LCA). The LCA optical module was used for modulating the optical power from the 1550 nm laser source integrated in the LCA. The modulated optical signal was amplified with an erbium-doped fiber amplifier and a 1.5 nm pass-band filter was employed to improve the signal-to-noise ratio. The electrical input port of the LCA was used for reading out the RF photogenerated electrical signal, while the average photocurrent was monitored with a Keithley 2400 unit, also employed for fiber-to-waveguide alignment and photodiode reverse DC biasing. The frequency response of the RF cables, RF adaptors, bias-tee and RF probe were deembedded through the LCA calibration. The detector structures shown in Fig. 2 showed a frequency response 3 dB cut-off point below 15 GHz, limited by the parasitic capacitance of the 1-1.5 mm long metal coplanar waveguide structure interconnecting the RF pads to the diode

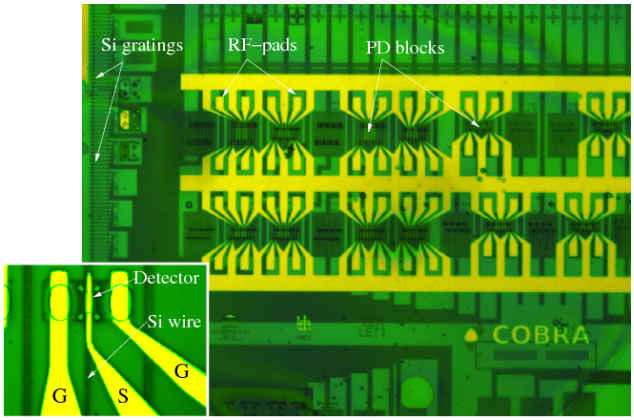

Fig. 4. Picture of the fabricated detectors with improved metallization pattern. A close-up of a detector is shown in the inset.

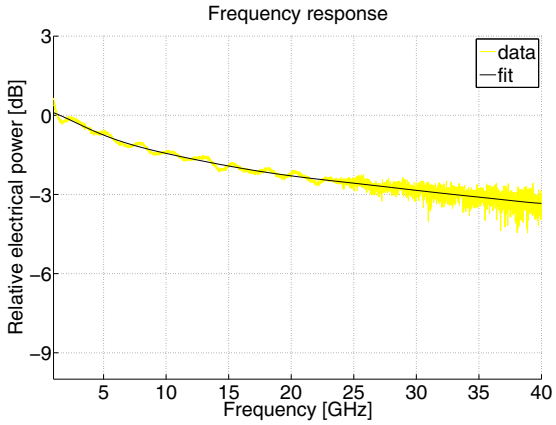

Fig. 5. Detector RF frequency response: normalized transmission parameter S_{21}.

contact layers. This issue was tackled in a following chip run, in which the RF pads were defined close to the devices and connected to the contact layers by means of 100 µm long tapers, as shown in Fig. 4. Results are presented in Fig. 5: a 3 dB cut-off frequency response of about 33 GHz was measured, which quite well matches the expectations.

IV. Conclusion

We presented an InP-based photodetector fabricated on a bonded SOI wafer containing Si waveguides, suitable for an optical interconnect layer on top of CMOS ICs. The PD footprint is 5×10 µm^2 and an InP membrane input waveguide is used to couple the optical signal out of the interconnect layer. Measurements recorded a detector responsivity and 3 dB bandwidth of 0.45 A/W and 33 GHz, respectively.

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