

Effect of device density on the uniformity of silicon nano-photonic waveguide devices.

Shankar Kumar Selvaraja, *Student Member, IEEE*, Katrien De Vos, *Student Member, IEEE*,
Wim Bogaerts, *Member, IEEE, OSA*, Peter Bienstman, *Member, IEEE*, Dries Van Thourhout, *Member, IEEE*,
and Roel Baets, *Fellow, IEEE*

Abstract—We report wavelength selective device nonuniformity of 1 nm over a 200 mm SOI wafer using CMOS fabrication technology. We also report correlation between device density and nonuniformity.

Index Terms—Silicon-on-Insulator, 193nm optical lithography, CMOS photonics,

I. INTRODUCTION

Silicon nano-photonic devices are very sensitive to small dimensional variation and operating environment. Though the devices were designed to function at a certain operating environment (e.g. at certain temperature), the variations originating from fabrication imperfections results in shift in spectral response of the devices. There are two way to tackle this issue, improved fabrication process to achieve high uniformity or compensate for variations through tuning or trimming the device. Though tuning is an option, the amount of tuning is dictated by the level of fabrication imperfections. Apart from the device thickness variation, which is decided by the wafer fabrication process, the width of the device depends on the patterning process, namely optical lithography and dry etch process.

Dry etching is an important step in the fabrication process, where the unwanted material is removed by exposing to a plasma containing chemically reactive radicals and neutrals. The height and the profile of the device is decided by the dry etch process. Loading or device density is an important aspect of dry etching, which affects linewidth uniformity [1], but this can be controlled by adapting device design at the mask level, while other aspects are strongly process related. The term loading is defined in various way in plasma processes, here we refer loading as device density.

In this paper we present our study of device non-uniformity due to etch loading over a 200 mm SOI wafer. The drop response of a 1×4 ring demultiplexer is used as test device for the study. A total of 220 rings were measured using a camera based parallel read-out system. We observe a strong correlation between loading and non-uniformity.

II. TEST DEVICES

We use 1st order ring based 1×4 (de)multiplexer as a wavelength selective device to demonstrate uniformity over a 200 mm wafer and the effect of loading. The ring resonators were designed in a race-track configuration with symmetrical coupling gap (180 nm) and coupling length (2000 nm) between

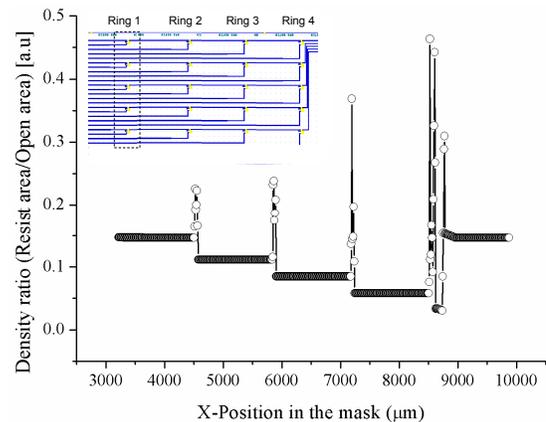


Fig. 1. Loading of different ring resonators. Inset-mask layout showing different rings.

the ring and the bus waveguide. The radius of the four rings were designed to be slightly different (5000 nm, 5010 nm, 5020 nm and 5030 nm), hence they would resonate at different wavelengths. In the mask the 1×4 (de)multiplexer is repeated 4 times with a pitch of 200 μm creating 4 identical (de)multiplexers. The arrange of the (de)multiplexer creates different loading environment for each ring, no special loading structures were added as the access waveguides themselves introduces the variation. Figure 1 shows the ratio of resist to open area along the length of the circuit. The presence of access waveguides along the length of the circuit changes the ratio as much as 50%. Ring1 as designated in fig.1 has a uniformity density environment while Ring4 has a non-uniform density, hence it is expected that the Ring4 would have higher non-uniformity response compared to Ring1.

III. FABRICATION PROCESS

The test devices described in the previous section was fabricated in a 200 mm SOI wafer with 220nm crystalline Si on top of 2000 nm buried silicon dioxide. The fabrication was done in a CMOS pilot line at IMEC, Leuven, Belgium. We used 193nm optical lithography (ASML/1100) and dry etching to define our circuits. The pattern definition process was optimized to yield a highly uniform devices over a single chip and over a 200 mm wafer. Details about the fabrication process can be found here [2].

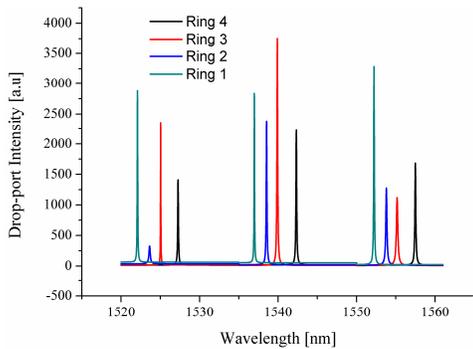


Fig. 2. Drop-port spectrum of 1×4 ring (de)multiplexer.

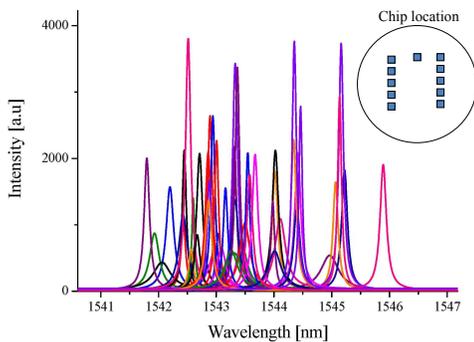


Fig. 3. Drop-port spectrum of 55 ring filters from 11 chips.

IV. MEASUREMENTS AND DISCUSSION

The fabricated devices were optically characterized by coupling in TE polarized light from a tunable laser source and measuring the output from the devices through an IR-camera. Grating fiber couplers were used for in and out coupling of light. The light from the tunable laser is uniformly illuminated over all the grating fiber couplers of the devices in a chip through a lens and the output light is collected with an IR-camera. This enables a simultaneous measurement of 20 ring (de)multiplexers.

The measurement spectrum was limited to the 1550nm telecom wavelength range (1520nm-1600nm) with a resolution of 10pm. Each resonance peak of the resonators were then fitted using lorentzian function. Figure 2 shows the fitted spectral response of 1×4 (de)multiplexers. After fitting, the free spectral range of the rings were 15 nm and a Q factor of 12,000. Since the 4 rings were design with different ring radius they resonate at different wavelengths. Figure 4 shows the shift in the resonance wavelength as a function of perimeter of the ring resonator. We observe a shift of 0.0228 nm/nm shift in the perimeter of the ring resonator. This value aggress with the experiments conducted by Xiao et al in [3].

The drop-port response of the filters is collected from 220 rings from 11 chip from a 200 mm SOI wafer for uniformity analysis. Figure 3 illustrates the resonance wavelength of nominally identical 55 ring filter from 11 chips and the inset shows the location of the chips. The closest and farthest chips

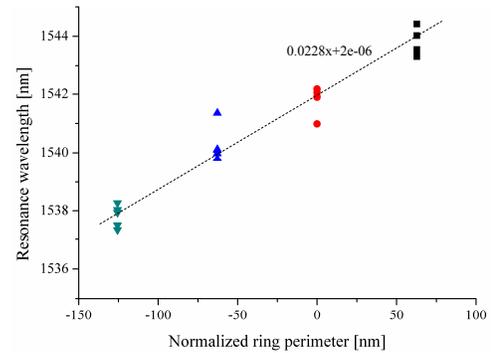


Fig. 4. Resonance wavelength shift as a function of perimeter.

TABLE I
DEVICE UNIFORMITY STATISTICS.

		σ : standard deviation, R : Range ($\lambda_{max} - \lambda_{min}$)				
		Within chip		Within wafer		
Device	Mean	σ nm	R nm	Mean	σ nm	R nm
Ring1	0.3	1	1	1	4.2	
Ring2	0.4	1	1	1.1	5.1	
Ring3	0.4	1	1	1.3	5.9	
Ring4	0.6	1	1	1.5	6.1	

were 20 mm and 120 mm apart respectively. The resonance wavelength of the rings were extracted from the fitted spectrum and the statistics are extracted from them, Table I shows the within chip and wafer statistics.

Within a chip the standard deviation σ increases from ring1 to ring 4. Over a 200 mm wafer, ring1 which has a uniform loading has lower nonuniformity ($\sigma=0.9$ nm, $R=4$) and ring4 has high nonuniformity ($\sigma=1.3$, $R=6$ nm) due to nonuniform loading. The loading control not only help for uniformity control within a chip, but also over the wafer.

V. CONCLUSION

Highly homogeneous ring based filter were demonstrated in high index contrast silicon-on-insulator platform using 200 nm CMOS fabrication tools. We correlate the device uniformity and loading within a chip and over a 200 mm wafer. We observe resonance wavelength nonuniformity of 1 nm with a range of 4 nm over a 200 mm wafer.

ACKNOWLEDGEMENT

We acknowledge the Smartmix Memphis and the ICT WADIMOS projects for supporting this work.

REFERENCES

- [1] D. L. Flamm, V. M. Donnelly, and D. E. Ibbotson, "Basic chemistry and mechanisms of plasma etching," *J. Vac. Sci. Technol. B*, vol. 1, no. 1, pp. 23–30, 1983.
- [2] S. K. Selvaraja, P. Jaenen, S. Beckx, W. Bogaert, P. Dumon, D. Van Thourout, and R. Bates, "Fabrication of photonic wire and crystal circuits in silicon-on-insulator using 193nm optical lithography," *J. Lightw. Technol.*, to be published.
- [3] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for wdm applications," *Opti. Express*, vol. 15, no. 12, pp. 7489–7498, 2007.