

Indium Phosphide based Membrane Photodetector for Optical Interconnects on Silicon

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Abstract—We have designed, fabricated and characterized an InP-based membrane photodetector on an SOI wafer containing a Si-wiring photonic circuit. New results on RF characterization up to 20 GHz are presented. The detector fabrication is compatible with wafer scale processing steps, guaranteeing compatibility towards future generation electronic IC processing.

I. INTRODUCTION

FOR future generation electronic ICs, a bottleneck is expected at the interconnect level. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution, providing bandwidth increase, immunity to EM noise and reduction in power consumption [1]. This solution is investigated within the European project PICMOS¹. In that context, the interconnect layer is built as a passive Si photonic waveguide layer and the InP-based photonic sources and detectors are fabricated in a way compatible with wafer scale processing steps. This approach combines the advantages of high quality Si wires with the excellent properties of InP-based components for light generation and detection. The integration technique that is investigated here assures compatibility towards future generation electronic ICs and is based on a die-to-wafer molecular bonding technology [2]. Experimental results on a full optical link, including lasers and detectors, were reported in [3]. In this paper, we focus on the photodetector (PD): device design, fabrication and measurement results are presented, including device characterization up to 20 GHz.

II. DESIGN

In order to detect the light, it first has to be coupled from the Si wire into the PD structure. In our approach, that is realized by means of an InP membrane input waveguide on top of the SOI wafer containing the Si photonic wiring (see Fig. 1). The two waveguides act as a synchronous coupler that

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¹Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), <http://picmos.intec.ugent.be>

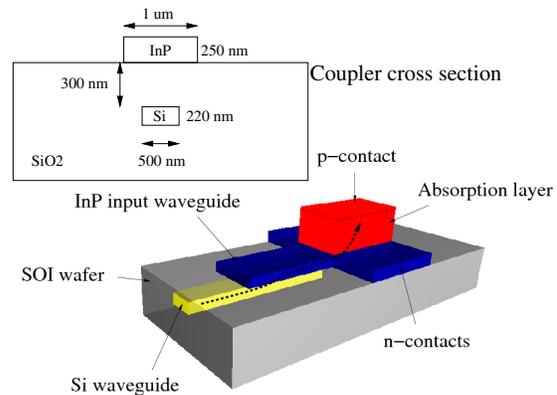


Fig. 1. Photodetector structure. The coupling from the Si waveguide layer to the PD is realized via the InP membrane input waveguide, on top of which the detector is stacked. A cross section of the coupler is schematically shown.

transfers the optical signal from the Si wire into the transparent InP waveguide, which guides it to the PD absorption region stacked on top of the transparent layer. The detector structure is built as an InGaAs absorption layer sandwiched between a highly p-doped InGaAs contact layer and a highly n-doped InP layer, which is also used for realizing the membrane waveguide, and has a footprint of $5 \times 10 \mu\text{m}^2$. We chose a total detector thickness of $1 \mu\text{m}$ in order to ease integration with the μ -disk lasers described in [3]. The thickness also results from a trade-off between device speed and efficiency: simulation results show that with our PD configuration, an internal quantum efficiency of $> 70\%$ and a 3-dB bandwidth of 25 GHz are expected, as we reported in [4]. The detector input InP coupler was designed with a cross section geometry of $0.25 \times 1 \mu\text{m}^2$ and a length of $14 \mu\text{m}$ to achieve mode matching with the Si photonic waveguide, which is $500 \times 220 \text{ nm}^2$ [4]. Details about design, fabrication and characterization of the Si waveguides are extensively presented in [5].

III. FABRICATION

The PD layer stack was grown on a 2" InP wafer. It was sawn in dies that were then molecular-bonded upside down on an SOI wafer, in which the Si waveguides had been defined, and the InP substrate was removed from the dies by a combination of CMP and wet-chemical etching. Afterwards, the PD pattern was aligned on the Si structures by e-beam lithography and transferred to a SiO₂ hard mask.

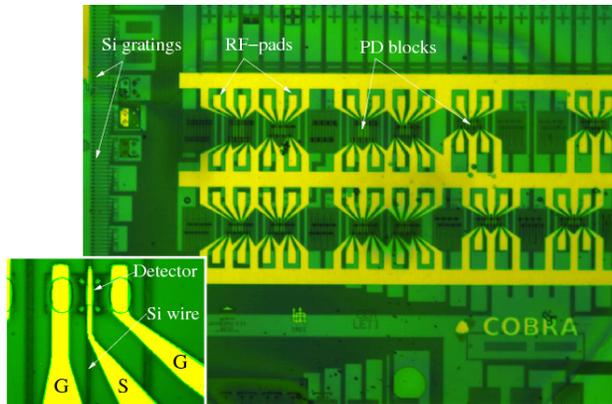


Fig. 2. Picture of the chip. PDs are grouped in blocks (8 devices/block). RF pads and Si grating couplers are indicated. In the close-up box, a PD and the initial part of the Ground-Signal-Ground (GSG) RF metal pads are shown.

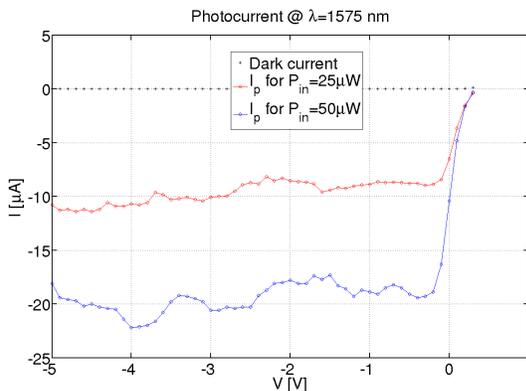


Fig. 3. Measured photocurrent for 0, 25 and 50 μW optical input power as a function of the detector applied bias voltage.

Then, the SOI wafer was sawn into samples, to allow for processing in our clean room. The PD structure was defined using III-V conventional wet- and dry-etching techniques. A polyimide layer was used to planarize the chip and provide electrical isolation and a Ti/Pt/Au metal stack was evaporated and patterned by lift-off. Si grating fiber couplers were also integrated in the Si waveguide layer to allow for on-wafer characterization [6]. Fabricated devices are shown in Fig. 2.

IV. EXPERIMENTAL RESULTS

The detector DC characterization was performed by using a tunable laser source (TLS) and a polarization controller to couple TE-polarized light through the grating coupler into the Si waveguide. A source-meter unit was used to reversely bias the PD and to read out the generated photocurrent. The photodiode generated photocurrent as a function of the applied bias voltage was measured for 0, 25 and 50 μW input powers (see Fig. 3). A dark current around 1.6 nA was registered at -4 V. The PD responsivity was calculated to be $R = 0.45$ A/W, which is a conservative value, as the grating coupler maximum efficiency was assumed (maximum 20% at 1575 nm). Such responsivity corresponds to a quantum efficiency of 35%,

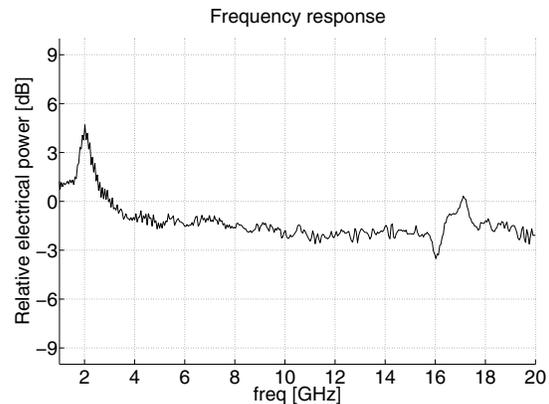


Fig. 4. Detector frequency response.

which includes the efficiency of the InP membrane coupler and the internal quantum efficiency of the pin-detector itself. Dynamic measurements were performed in the range of 130 MHz to 20 GHz with an Agilent HP8703A lightwave component analyzer (LCA), used for small signal modulation of the input optical power from the TLS and for reading out the RF electrical signal generated by the PD. Results are presented in Fig. 4, which shows a rather flat frequency response up to 20 GHz, except for oscillations around 17 GHz, probably due to non-ideal de-embedding of the RF components used in the set-up, and around 2 GHz, caused by the optical module of our LCA, not working properly below that point.

V. CONCLUSION

We presented a $50 \mu\text{m}^2$ InP-based photodetector fabricated on samples bonded to an SOI wafer containing Si waveguides, suitable for an optical interconnect layer on top of CMOS ICs. Measurements recorded a responsivity $R=0.45$ A/W and a rather flat frequency response up to 20 GHz.

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