Low-Loss Amorphous Silicon-On-Insulator Technology for Photonic Integrated Circuitry

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Abstract

We report the fabrication of low-loss amorphous silicon photonic wires deposited by plasma enhanced chemical vapor deposition. Single mode photonic wires were fabricated by 193nm optical lithography and dry etching. Propagation loss measurements show a loss of 3.46dB/cm for photonic wires (480×220nm) and 1.34dB/cm for ridge waveguides.

Key words: Integrated optics, Waveguides, Amorphous silicon
PACS: 42.82.-m, 42.70.Km, 42.82.Et

1 Introduction

With an ever increasing complexity and density of photonic integrated circuits there is an increasing need for multilayer functionality. This could either be the combination of an electronic layer and an optical layer or the combination of several optical layers. In the latter case, the use of optical vias allows avoiding waveguide crossings, which, particularly in high-index contrast waveguiding systems, often lead to high crosstalk and losses [1] . Also the intimate combination with electronics becomes more and more critical as the complexity of the photonic layer increases [2,3].

Monocrystalline Silicon-On-Insulator (SOI) substrates are now widely used for making highly efficient photonic integrated circuits [4–7]. However, despite the superior material quality, these do not allow flexible multilayer stacking. On the other hand, deposited materials provide the freedom for multiple layer

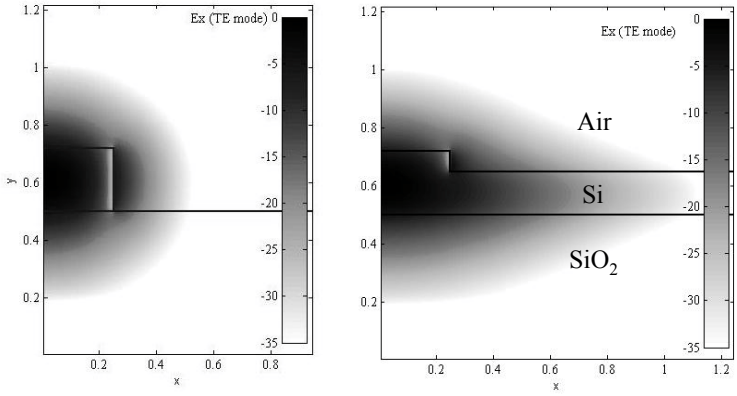

Fig. 1. Fundamental TE-like mode profile of photonic wire (left) and ridge waveguides (right).The field intensity legend is in dB.

stacking. To be CMOS back-end compatible, the maximum temperature of the deposition process should be restricted to 400^oC.

Silicon can be deposited in a variety of ways [8–10]. The nature (amorphous, polycrystalline or crystalline) of the film depends on the process parameters and deposition technique(s) used. Crystalline silicon obviously has the highest quality but requires a monocrystalline substrate and a high deposition temperature. Also polycrystalline silicon requires a temperature above 400^oC and typically has a higher propagation loss [8]. Therefore this work focuses on low temperature deposited amorphous silicon (a-Si).

Plasma enhanced chemical vapor deposition (PECVD) is a well suited process for the deposition of high quality a-Si at low temperatures. If no special precautions are taken, dangling bonds present in the film will cause mid-bandgap absorption in the infra red wavelength range, however, resulting in considerable propagation losses. These dangling bonds can be saturated by incorporating hydrogen (H) in the film during the deposition process however, resulting in hydrogenated a-Si (a-Si:H).

Almost a decade ago Cocorullo et al [11] demonstrated the use of amorphous silicon for photonic applications and since then significant progress has been made to reduce the material loss. Several groups have already demonstrated single-mode waveguides fabricated from hydrogenated a-Si deposited using similar processes with a loss as low as 2 dB/cm for ridge waveguides [9] and 4.5dB/cm for photonic wires [2]. In this paper we present our results on a-Si:H deposited by a PECVD process using CMOS manufacturing tools.

2 Design

Two types of waveguides were designed and fabricated; shallowly etched ridge waveguides to get an approximation for the bulk loss and deeply etched photonic wires. The waveguides widths were kept constant while an etch depth of 70nm was chosen for the ridge waveguides and 220nm for the photonic wires. The mode profiles for deeply and shallowly etched waveguides were calculated using a finite difference method (Fig.1). For the ridge waveguides, the scattering loss is reduced because of the smaller sidewall surface area. At the same time the fraction of optical power in the deposited layer is higher, but with a lower power density than in the photonic wire. As a result, from measuring the propagation loss in the ridge waveguides we estimate an upper limit of the material loss in the deposited a-Si:H.

To demonstrate the high quality of the deposited amorphous silicon we also implemented two types of wavelength selective devices in the same process: all-pass racetrack ring resonators and mach-zehnder interferometers (MZI). The resonators were designed with a bending radius of 4μm and a coupling gap of 180nm between the bus and the ring. For realizing the 1×1 MZIs we used two Y-splitters and introduced a delay length (δL) of 50μm in one of the two arms.

3 Fabrication

200mm silicon wafers were used as the substrate to build the a-Si:H photonic circuits on. A 2μm silicon dioxide layer (BOx) was deposited using a high density plasma CVD process followed by a chemical mechanical polish (CMP). After polishing using AFM we measured a roughness of 0.1nm, which can be directly translated into bottom surface roughness for the a-Si film. A 220nm layer of a-Si:H was deposited over the BOx by PECVD in a commercial parallel plate reactor. Silane (SiH_4) was used as the precursor gas and combined with Helium (He) for dilution. The deposition parameters were tuned to obtain a good quality film. The power was tuned from 180 to 300W, the He-to-SiH4 ratio from 0 to 9. In that way we aimed at achieving an optimum level of hydrogen for dangling bond passivation. On the other hand, cluster and voids will appear in the film with high concentration of H. Hence, controlling the amount of H is critical in achieving low-loss a-Si.

The optimum amount of H in the film is determined through FTIR spectroscopy. The H in the film exist as mono, di and, polyhydrides of Si. Though there are different vibration modes, which are related to different species, the important vibration modes are the stretch mode of SiH and SiH2 at $\approx$ 2000

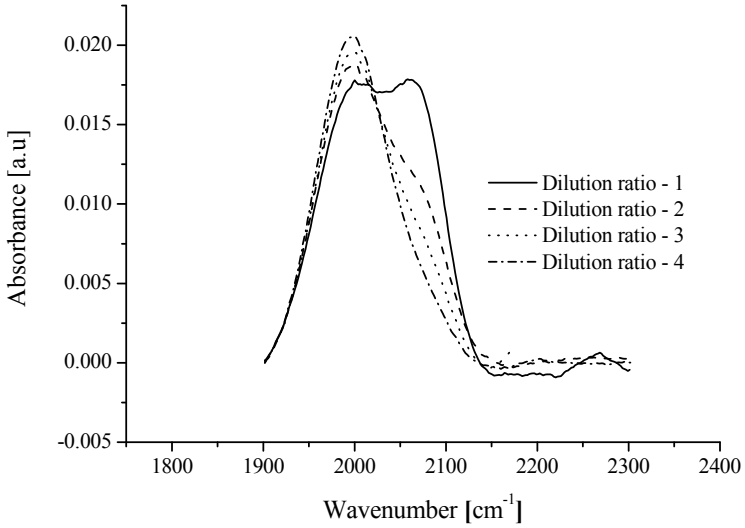

Fig. 2. FTIR spectrum.

cm^{-1} and $\approx$2100 cm^{-1} respectively in the FTIR spectrum (Fig.2). Higher amount of SiH_2 in the film creates clustering of H atoms, thus forming microstructure or voids in the film. The microstructure causes an abrupt change in the refractive index, creating higher scattering loss. The microstructure is determined from the relation $I_{2100}/(I_{2000}+I_{2100})$, where I_{2000} and I_{2100} denote the integrated area under the peaks at 2000 cm^{-1} and 2100 cm^{-1} respectively [12]. Fig.3 illustrates that by increasing the dilution the microstructure in the film can be reduced. Then the power is tuned to achieve lower growth rate, which is known to give low dangling bonds (or defects) [13].

After optimization, the quality of the deposited film with different process conditions was assessed by characterizing the propagation loss in a photonic wire. We obtain a good quality film at He/SiH_4 ratio of 9 and a power of 180W, while the deposition temperature was fixed at 300^oC. The low temperature is not only important to maintain the amorphous nature of the film but also to keep the process CMOS back-end compatible. The photonic wires and ridge waveguides were then fabricated using 193nm optical lithography and an ICP-based etching process [14]. The ridge waveguides were etched 70nm deep while the wires were etched completely through the a-Si:H layer (220nm). Some of the fabricated wires were covered with low temperature (400^oC) plasma silicon dioxide as an upper cladding layer.

4 Results and Discussions

The propagation loss of the fabricated waveguides was characterized by coupling TE polarized light from a tunable laser (1500nm-1600nm) into the waveguides and measuring the output power through grating fiber couplers [15]. To

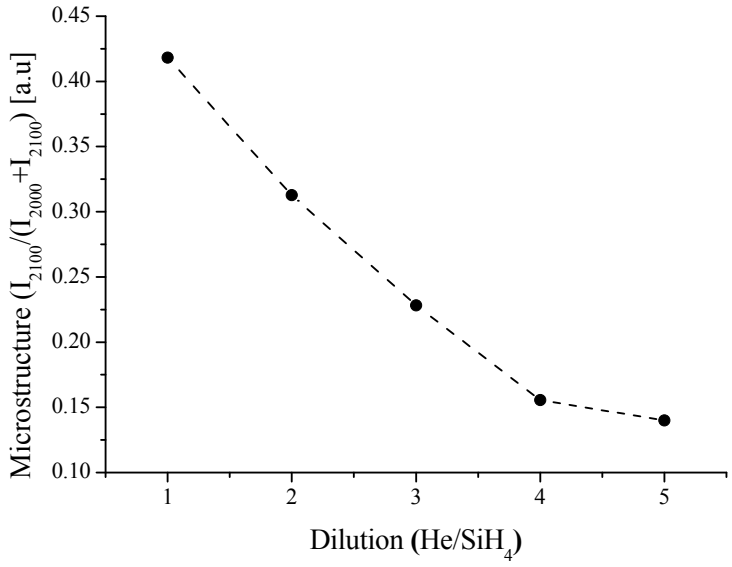

Fig. 3. Microstructure or void in the film.

Table 1
Loss comparison.

Ref	Material Loss [dB/cm]	Wire Loss [dB/cm]	wire dimension [nm]	Top cladding
[16]	1.5	40	500×250	Air
[17]	< 1	6.5	500×200	SiN
[2]	0.5	4.5	500×200	SiO_2
This work	0.7	3.5	480×220	Air
This work	–	3.4	480×220	SiO_2

measure the optical loss we used spiralled photonic wires and ridge waveguides with varying lengths and large bending radius (70μm). The power transmitted through different lengths of waveguides was measured and the loss was extracted by linear regression. The results are shown in Fig.4. Photonic wires of 480nm wide and 220nm thick show a loss of 3.46dB/cm (at 1550nm). To our knowledge this is the lowest propagation loss reported for an a-Si:H photonic wire of such dimension. For the samples with oxide cladding we measured similar losses (3.4dB/cm) (at 1550nm). By deducing the propagation loss measured for monocrystalline SOI based photonics wires fabricated using a similar process from the a-Si:H wire loss, we can estimate the bulk material loss to be ≈0.7dB/cm. Alternatively, the ridge waveguide propagation losses can be considered as an upper estimate for the bulk material loss since in these waveguides the interaction between propagating mode and sidewall roughness is considerably reduced compared to photonic wires. Table 1 summarizes some of the propagation losses published by different groups using a similar deposition process.

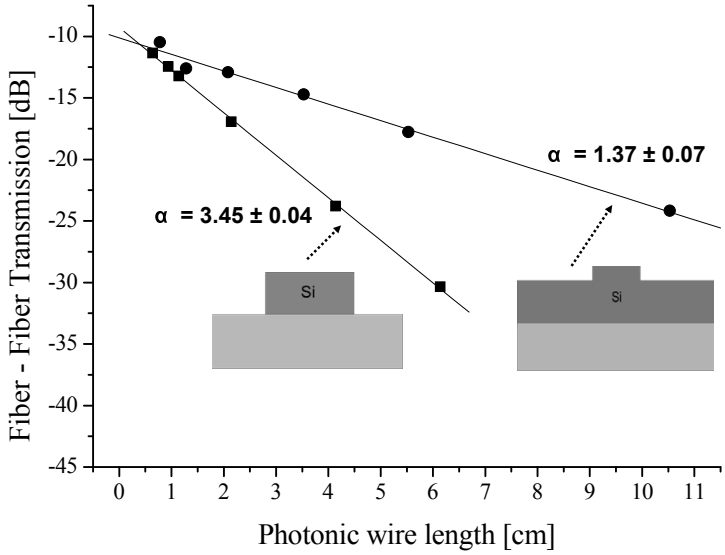

Fig. 4. Linear regression of transmitted power as a function of waveguide length at 1550nm.

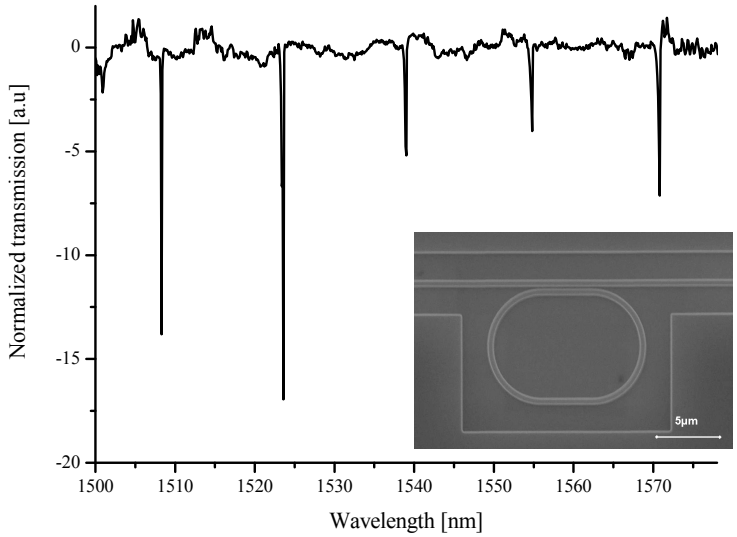

Fig. 5. Normalized transmission spectrum of a racetrack ring resonator and SEM image of the structure.

Fig.5 shows the transmission spectrum of a racetrack ring resonator. The spectrum is normalized to a reference waveguide. The resonator has a free spectral range of 15.6nm, corresponding to a group index of 4.9 and a 3dB bandwidth of 0.16nm, corresponding to a Q factor of ≈10,000 and a finesse of 102. Fig.6 depicts the transmission spectrum of a MZI. We obtain an average free spectral range (ΔL)of 10nm. From the spectral response of the MZI we extracted a group index of 4.8 ($n_g = \lambda_{min}\lambda_{max}/\Delta L\Delta\lambda$). By careful design of the Y splitter we obtain an average extinction ratio of 27dB and a 3dB on-chip insertion loss.

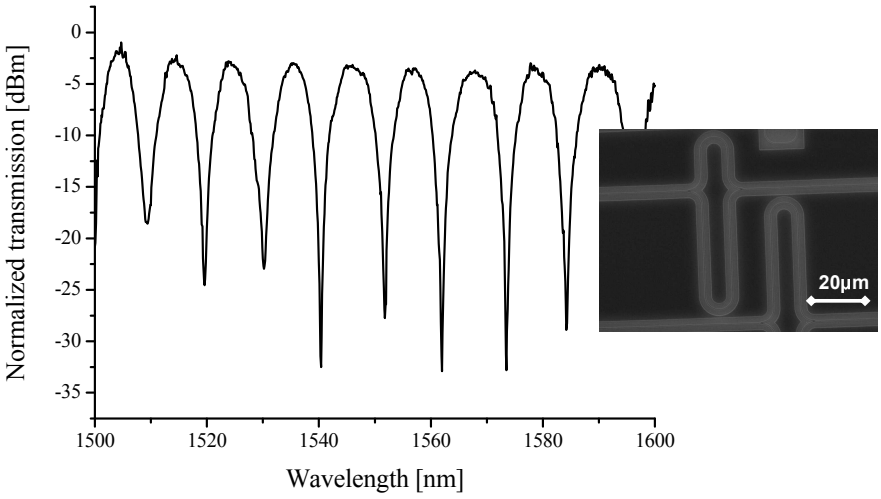

Fig. 6. Normalized TE transmission spectrum of a MZI and SEM image of the structure.

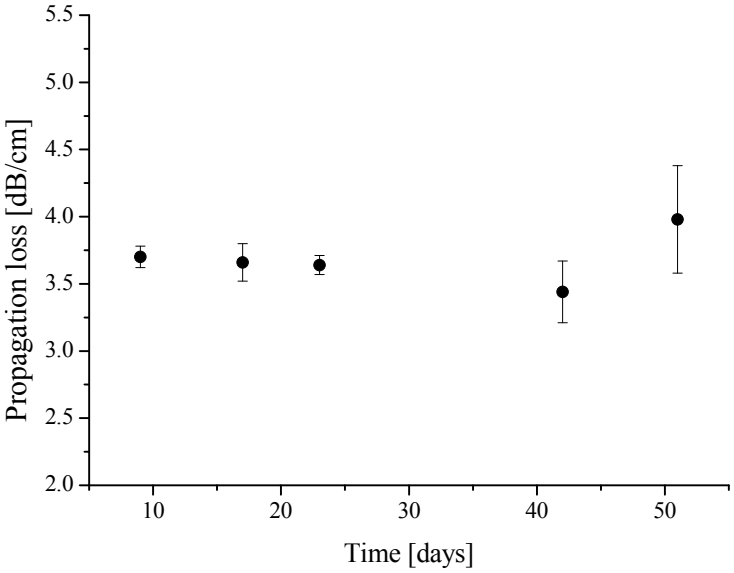

Fig. 7. Propagation loss stability over a time period of 55days.

The stability of a-Si:H over time and with respect to subsequent processing steps is an important property. Different environmental parameters such as temperature and pressure can change the film property. As a preliminary test, we measured the propagation loss of photonic wires without oxide cladding as a function of time. The samples were stored in a sample box at room temperature and without any environmental control. The propagation loss measurements performed over a time period of 55days show no change or change within the measurement error of ± 0.2dB/cm (Fig.7). This indicates the high stability of the deposited film in a normal (room temperature) environment.

Some of the samples were covered with silicon dioxide as upper cladding layer,

which was deposited at 400^{o}C. We did not observe any change in the propagation loss of the photonic wires from the samples with and without oxide cladding. Thus the film remains stable up till 400^{o}C, which is the maximum temperature allowed in the back-end of the CMOS fabrication process.

5 Conclusions

We present our preliminary results on amorphous silicon deposited by plasma enhanced chemical vapor deposition for photonic integrated circuitry. Low-loss photonic wires and ridge waveguides were demonstrated with a loss of 3.46±0.04dB/cm and 1.34±0.07dB/cm respectively. We have also demonstrated wavelength selective photonic devices, such as racetrack resonators and mach-zehnder interferometer. This clearly proves the feasibility of employing low-loss, low deposition temperature amorphous silicon for realizing photonic circuit in a single and multilayer waveguide circuits or adding an optical layer on top of electronic CMOS circuitry.

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