

Compact Silicon-on-Insulator Wavelength Demultiplexer with Heterogeneously Integrated InAlAs/InGaAs Photodetectors

Joost Brouckaert, Gunther Roelkens, Shankar Selvaraja, Wim Bogaerts, Pieter Dumon, Steven Verstuyft, Dries Van Thourhout, Roel Baets
 Ghent University – IMEC, Department of Information Technology
 St. Pietersnieuwstraat 41, 9000 Gent, Belgium
 email: joost.brouckaert@intec.ugent.be

Abstract

We present experimental results of a 4-channel demultiplexer with integrated photodetectors. The device consists of a silicon-on-insulator planar concave grating demultiplexer and heterogeneously integrated III-V photodetectors.

Introduction

Demultiplexers are one of the key components in wavelength division multiplexed (WDM) optical telecommunication systems. The nanophotonic silicon-on-insulator material system is a very attractive candidate for the fabrication of demultiplexers and photonics integrated circuits in general. By making use of photonic wire waveguides, very compact passive waveguide circuits can be fabricated and large-scale integration of different photonic functions on a single chip becomes possible. Moreover, these devices can be fabricated on low cost, high quality SOI substrates using CMOS processing techniques [1].

As silicon is transparent at typical telecom wavelengths (1.3 and 1.55 μm), other materials need to be integrated to obtain efficient photodetection at these wavelengths. The two most promising wafer scale approaches are Ge-on-SOI [2] and III-V-on-SOI detectors [3].

In this paper, we demonstrate a coarse-WDM receiver consisting of a 4-channel planar concave grating (PCG) demultiplexer with heterogeneously integrated III-V photodetectors. These photodetectors are integrated by means of bonding unprocessed III-V dies (epitaxial layers down) onto the SOI waveguide wafer using DVS-BCB as an intermediate adhesive layer. After substrate removal, the detectors can be fabricated on a wafer scale and lithographically aligned to the underlying SOI waveguides. This integration schema avoids time consuming and alignment-critical hybridization of pre-processed III-V detectors.

Design and fabrication

The fabricated device is shown in Figure 1. A planar concave grating (PCG) demultiplexes the input signal into 4 output channels with a spacing of 20nm around a central wavelength of 1550nm. Thin film InAlAs/InGaAs metal-semiconductor-metal (MSM) photodetectors with a length of 40 μm are

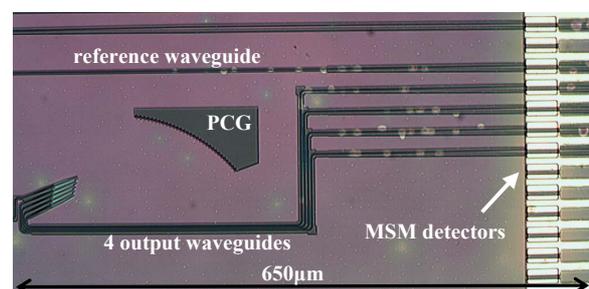


Figure 1: Picture of the 4-channel CWDM receiver

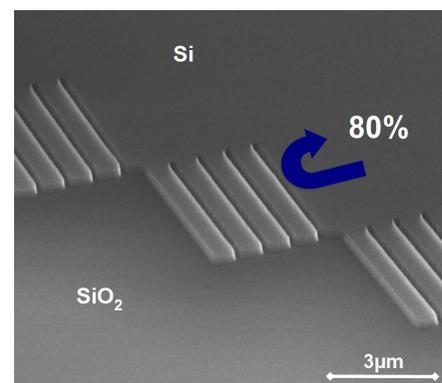


Figure 2: SEM picture of the DBR grating facets.

heterogeneously integrated onto the output waveguides. The total footprint of the demultiplexer, including photodetectors is only $\sim 650 \times 150 \mu\text{m}^2$.

The design of the PCG is based on the Rowland configuration and is clearly described elsewhere [4, 5]. The demultiplexer is fabricated on a 200mm SOI wafer with a 220nm thick Si top layer. Structures were defined with 193-nm deep-ultraviolet (DUV) lithography, and transferred into the silicon using ICP-RIE. We decreased the on-chip loss of the PCG down to 1.9dB by replacing each flat facet with a second order distributed Bragg reflector (DBR) facet [5] (Figure 2). The main advantage of this approach in comparison with coating the backside of the grating with a reflective metal is that this method does not require extra processing steps.

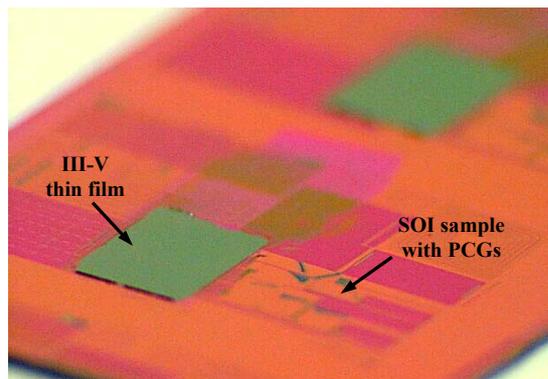


Figure 3: Picture of two unprocessed III-V films ($3 \times 3 \text{mm}^2$) bonded on a processed SOI substrate.

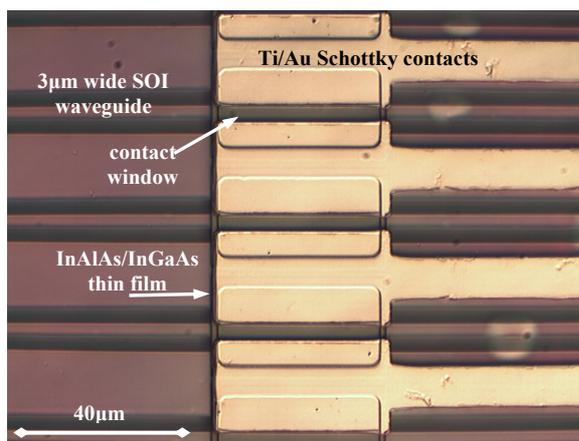


Figure 4: Top view of three MSM detectors on top of $3 \mu\text{m}$ wide SOI waveguides.

Evanescently coupled III-V photodetectors were integrated on top of the output waveguides. The fabrication starts with bonding unprocessed III-V dies (epitaxial layers down) onto the SOI waveguide substrate using DVS-BCB. After removal of the InP substrate and sacrificial etch-stop layers, we obtain a defect-free epitaxial thin film (see Figure 3) consisting of a 40nm thick InAlAs Schottky barrier enhancement layer on a 20nm thick InAlGaAs graded layer on a 145nm InGaAs absorption layer.

From now on, photodetectors can be processed on a wafer scale and lithographically aligned onto the SOI waveguides. To obtain evanescent coupling, the DVS-BCB bonding layer between SOI waveguides and MSM detector is only 130nm thick. Processing, simulation and measurements of these MSM detectors are described elsewhere [3]. Detectors with a length of $40 \mu\text{m}$ have a responsivity of 1.0A/W at $1.55 \mu\text{m}$ and a dark current of 3nA at 5V bias. The detector pitch is $25 \mu\text{m}$.

Measurement results

Light was coupled into the SOI chip using fiber couplers. These are shallowly etched 1-D gratings which allow coupling light from a single mode fiber into the nanophotonic waveguides.

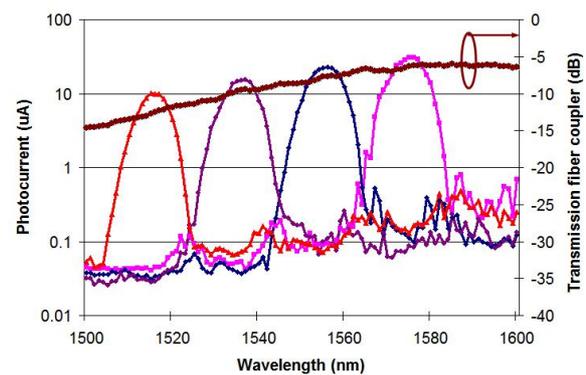


Figure 5: Photocurrent spectrum of integrated demux for TE polarization.

The transmission of these fiber couplers is shown in Figure 5 (right axis). The minimum coupling loss was estimated to be 6dB at a wavelength of 1580nm . The PCGs, fiber couplers and photodetectors are designed for TE-polarization.

Figure 5 also shows the photocurrent spectrum of the CWDM receiver. The crosstalk is about -25dB and no deterioration of PCG characteristics were observed before and after detector integration. The large channel non-uniformity is due to the fiber coupler response as can be seen in Figure 5. The power budget of the CWDM receiver can be calculated as follows. By fine-tuning the fiber coupler, it is possible to make the central PCG wavelength and the maximum fiber coupler transmission coincide at $1.55 \mu\text{m}$. The total loss for the central channels is about 6dB (fiber coupler loss) + 2dB (on-chip PCG loss). Taking into account a detector responsivity of 1.0A/W at $1.55 \mu\text{m}$, the total responsivity for the central channels is $\sim 0.16 \text{A/W}$.

Conclusions

We demonstrated a very compact 4-channel demultiplexer based on the heterogeneous integration of III-V photodetectors on SOI PCGs. As these photodetectors can be processed on a wafer-scale on cheap and high quality SOI substrates, it opens the way for low cost, high volume processing.

References

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