

Silicon nanophotonics on CMOS.

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Introduction

Silicon nanophotonics is a very rapidly growing research domain. The basic idea is to use the tools and materials employed for processing the most advanced electronic circuits also for the fabrication of photonic circuits. These tools are typically much more advanced than those used for the fabrication of classical optoelectronic devices and therefore allow for a much higher performance, much denser integration, mass manufacturing and integration with electronics. In addition, silicon is a very attractive material for the fabrication of ultra compact photonic devices: it has very low losses in the telecom range (1.3 μ m, 1.55 μ m) and the high refractive index contrast with air or with SiO₂, which is typically used as a cladding material, permits strong light confinement. We will show some examples of such devices below. The main drawback is that it is far from straightforward to get light emission from silicon, which is an indirect bandgap semiconductor. Therefore we developed an efficient process for the integration of III-V based semiconductor material with the silicon waveguides, based on a rapid die-to-wafer bonding process

Fabrication

The process typically starts from an SOI substrate with a top silicon layer of 200nm. A 2 μ m box-oxide ensures optical isolation between the waveguide structures and the silicon substrate. The devices are then defined using optical lithography and ICP-etching. Although the critical dimensions of the devices (\pm 200nm) are typically larger than for electronic devices, an extreme level of linewidth control (better than 1nm), roughness and uniformity is required (Fig. 1a). Therefore we recently started using 193nm DUV lithography, resulting in a considerably increased device performance (Fig. 1b). An alternative technology we are using for the definition of three dimensional photonic structures and for locally changing the structure of devices defined through DUV lithography is direct focused ion beam writing as illustrated in Fig. 1c.

Passive devices

Using this rather basic fabrication process extremely powerful devices could already be fabricated. Fig. 2a shows a grating demultiplexer, which allows the separation of different wavelength channels in different output waveguides. We also demonstrated low loss arrayed waveguide optical multiplexers and cascaded Mach-Zehnder based add-drop filters, for use in telecom systems. Each of these can be three to five orders smaller than their now commercially available counterparts fabricated in low index contrast systems. Besides applications in telecom and datacom, there are also large opportunities for building powerful photonic sensing systems, e.g. based on compact resonators as illustrated in Fig. 2b.

Active devices

As explained in the introduction, it is far from trivial to get light directly from silicon. Therefore, we developed an efficient heterogeneous III-V silicon integration process based on a rapid wafer-to-die bonding technology as outlined in Fig. 3a. Using this process, the very critical alignment between optoelectronic devices and the underlying silicon waveguides is ensured through a waferscale lithographic step and not during the pick-and-place process as in typical hybrid integration schemes. Using this process we demonstrated InGaAs-based detectors integrated with silicon waveguides with an efficiency of 80% and a footprint of only 6 μ m \times 25 μ m and also realized Fabry-Pérot type lasers with a power of > 1mW coupled into the silicon waveguide. In collaboration with several European partners (INL Lyon, CEA-LETI, Tracit Technologies) we demonstrated ultra-low threshold microdisk lasers that can be used for on-chip optical interconnect.

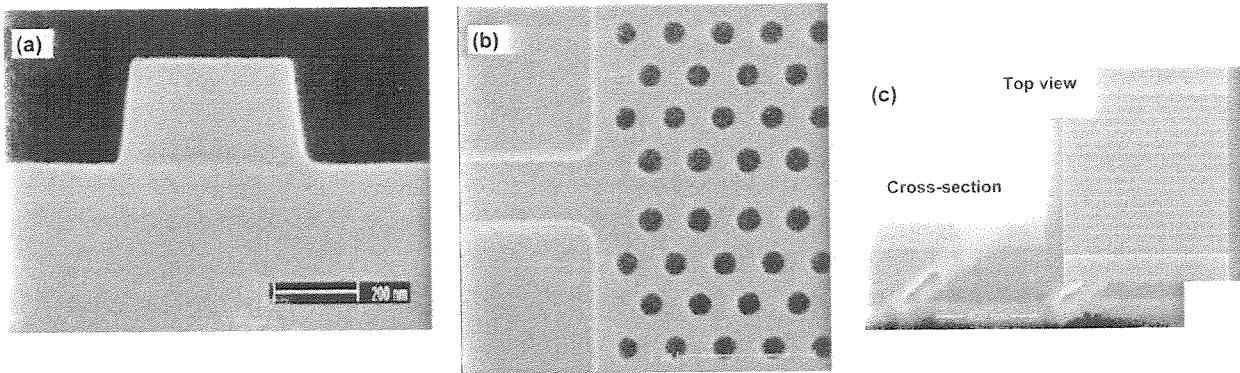


Fig. 1 (a) cross-section of a typical SOI based optical waveguide. Absolute dimensions ($\pm 1\text{nm}$), side wall verticality and side wall roughness ($\sigma < 2\text{nm}$) are the most important factors determining the quality of the process. (b) top view of photonic crystal waveguide defined using 193nm DUV lithography. (c) cross-section of fibre-chip coupling structure fabricated using focussed ion beam etching.

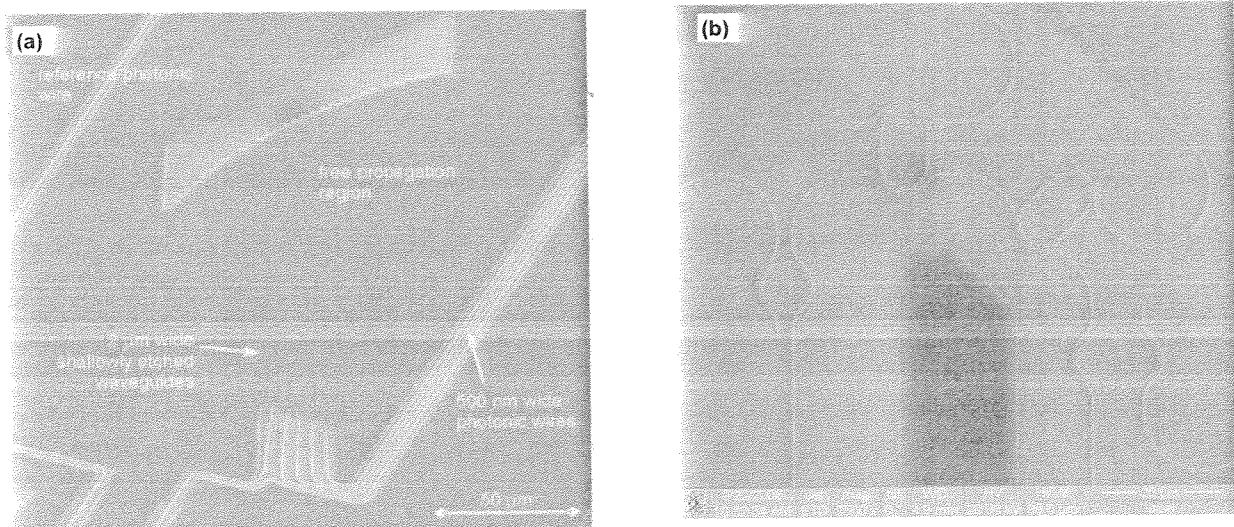


Fig. 2 (a) Compact photonic integrated circuit with grating demultiplexer (b) Two-dimensional strain sensor based on optical resonators

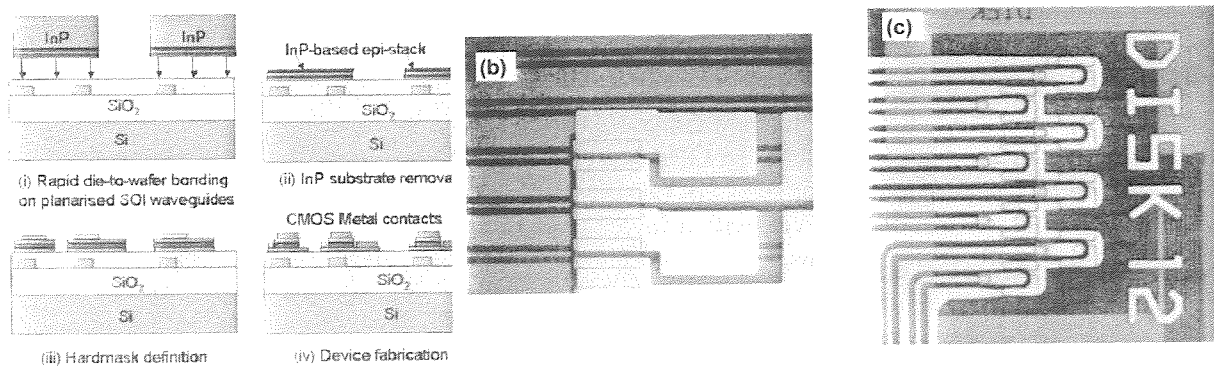
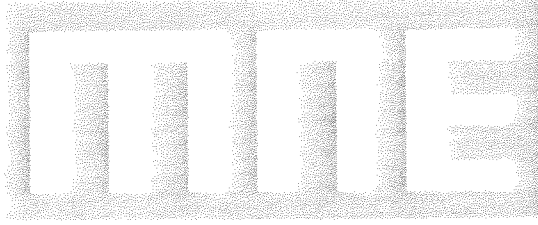


Fig. 3 (a) Heterogeneous integration process. (b) Compact MSM-type detectors on silicon waveguide (c) Array of 8 microdisk lasers with ultralow threshold integrated on Silicon Nanophotonic Waveguides

References

1. W. Bogaerts e.a., "Compact Wavelength-Selective Functions in Silicon-on-Insulator Photonic Wires", J. Selected Topics in Quantum Electronics, 12(6), p.1394-1401 (2006)
2. G. Roelkens e.a., "Adhesive Bonding of InP/InGaAsP Dies to Processed Silicon-on-Insulator Wafers using DVS-bis-Benzocyclobutene", Journal of Electrochemical Society, 153(12), p.G1015-G1019 (2006)



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