

Deposited Silicon-on-insulator material technology for photonic integrated circuitry

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With ever increasing complexity and density of photonic integrated circuits the need for multilayer functionality is arising for next generation photonic circuitry. As crystalline silicon is limited to single layer circuitry deposited silicon is one of the solutions for multilayer circuitry. Therefore, we explored two types of deposition technique for silicon: Low Pressure and Plasma Enhanced CVD process. The material properties are assessed for applicability by FTIR, XRD and SE characterization. Finally, the propagation loss is measured at 1550nm wavelength range. We measured a propagation loss of 3.5 and 13.4dB/cm for 500nm photonic wire fabricated from PECVD and LPCVD process respectively.

Introduction

Silicon photonic integrated circuit is a very attractive platform for wide range application. High index contrast enables small bending radius subsequently resulting in a much denser circuitry. Crystalline SOI material is used in almost all silicon photonic circuitry [1]. While it typically has exceptional material quality it limits the photonic circuit to a single layer. As an alternative, deposited silicon facilitates multi layer stacking of photonic layers and CMOS compatible. However, for this the deposited material should have similar quality in terms of optical properties as the crystalline silicon. Various deposited silicon materials have already been explored, such as SiON, SiN, SiC. Si can be deposited using various deposition processes. The property of the film depends on the process used and process conditions. In this work we explore low pressure CVD and plasma-enhanced CVD process to deposit polycrystalline (poly-) and amorphous (amp-) silicon respectively. Other groups using similar processes have already demonstrated optical loss of 9 and 6.5dB/cm [2, 3] for waveguides fabricated from Poly-Si and a-Si respectively.

Deposition of Silicon

Silicon is deposited by decomposition of silicon containing precursor gases. Gases such as SiH₄, SiCl₄, etc are popularly used precursor. These precursors are decomposed by applying high temperature or plasma. The film properties and composition depends on the degree of dissociation of the precursor. In this section a brief introduction of LPCVD and PECVD process is presented.

LPCVD process is widely used deposition process in CMOS fabrication process. Poly-Si can be deposited in two ways *a)* a-Si is deposited at low temperatures and annealed at high temperature to re-crystallize or *b)* deposit the film at high temperature to directly

form polycrystalline film. In this work we use approach *a*. Silicon is deposited at 560°C by complete decomposition of Silane (SiH₄). The film is then annealed/crystallized at 850°C in Nitrogen atmosphere, grain blocks are formed with different orientations resulting in grain boundaries. As the grains grow the defects also move towards the grain boundaries. Hence the grain boundaries are rich in defects such as dislocations and dangling bonds. The silicon dangling bonds defect creates mid-band gap absorption (in the telecom wavelength range). All these defects cause scattering and absorption of light resulting in propagation loss.

PECVD is a widely used deposition technique for dielectrics. Unlike LPCVD the film is can be deposited at very low temperatures <300°C. Temperature is an important parameter to maintain the amorphous nature of the deposited film. The plasma is buildup by applying RF power between parallel plates inside a chamber containing precursor gas. We use SiH₄ as precursor gas diluted with Helium. By diluting the precursor various film properties can be changes. Due to incomplete decomposition of the precursor gas H is incorporated in the deposited film. H present in the film helps to cure the silicon dangling bond subsequently reducing defects in the film. The deposition rate, film properties can be tuned by just changing the dilution.

Material characterization

In this section different material characteristics of the deposited silicon are analyzed. In this paper we present SE, XRD and FTIR measurements to measure material density, crystallinity and hydrogen content in the deposited silicon.

Figure 1 shows the refractive index as a function of feed gas ratio of PECVD a-Si. The refractive index or the density of the film increases with increasing He/SiH₄ ratio. With lower dilution the film forms clustered hydrogen resulting in low density film. For as deposited LPCVD the material density was low but after crystallizing the density of the film increases.

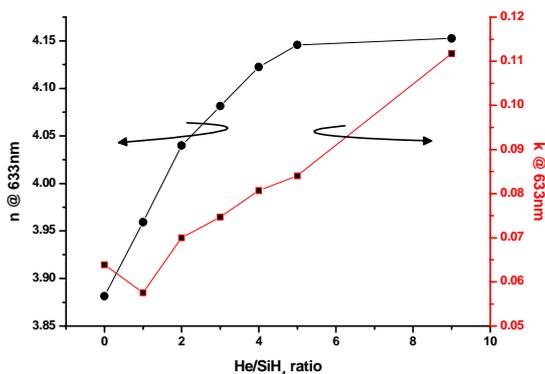


Figure 1 *n* & *k* as a function of He/SiH₄ ratio

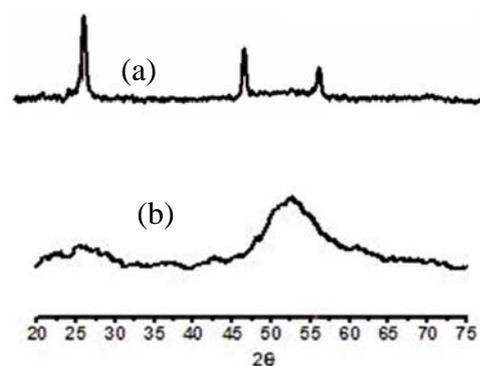


Figure 2 Glancing angle X-ray diffraction
a) polycrystalline silicon, b) amorphous silicon

A glancing angle X-ray diffraction technique is used to investigate the crystallinity of the deposited film. Figure 2 depicts results from such measurement. It can be clearly seen

that distinct peaks appear for poly-Si film where mono-crystalline blocks were formed during annealing; this result was confirmed by transmission electron microscopy (not shown here). On the other hand amorphous silicon doesn't have any such distinct peaks confirming the amorphous nature. The broad peak at $\sim 53^\circ$ is from the thermal vibration of silicon substrate.

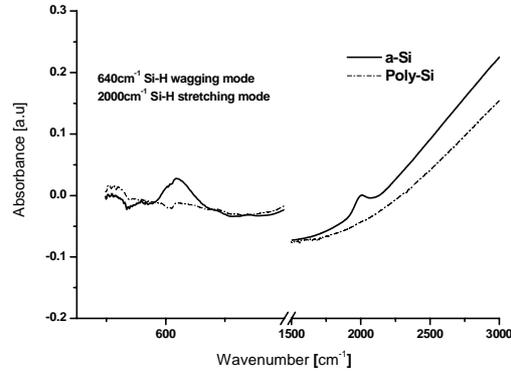


Figure 3 Truncated FTIR spectrum of poly and a-Si

Figure 3 shows the truncated FTIR spectrum from as-deposited LPCVD and PECVD silicon. The FTIR spectrum shows the hydrogen content in the deposited film. Peaks appearing at 640cm^{-1} and 2100cm^{-1} represent hydrogen content in the form of monohydrates (Si-H). Large number of monohydrate contributes to dangling bonds reduction.

Photonic circuit Fabrication and characterization

The photonic wires were fabricated on 200mm silicon handle wafers with $1\mu\text{m}$ of high density plasma (HDP) oxide. The deposition of bottom cladding is followed by a chemical mechanical polish (CMP) process. During CMP the oxide surface is polished smooth to form smoothing bottom interface. Successively, a 220nm silicon layer was deposited by PECVD or LPCVD process [4, 5]. Single mode photonic wires were then patterned by DUV optical lithography and etched using ICP-RIE [6]. Finally the photonic wires are covered with oxide as upper cladding. The propagation loss of photonic wires is measured by using wires of different length (by spiraling).

Light from a broad band source is coupled into the photonic wire and the output at the other end is measured by a spectrum analyzer. Grating couplers were used at the input and output of the wires to couple light [7]. The output power from photonic wires of different length is measured and the propagation loss is extracted by linear regression. Figure 4 shows the linear regression on the measured powers from an a-Si photonic wire. We measured a propagation loss of 13.4dB/cm for photonic wires fabricated on poly-Si photonic wire. While photonic wires fabricated on a-Si we obtain a loss of 3.5dB/cm. The low propagation loss indicates the superior quality of the material for photonic applications.

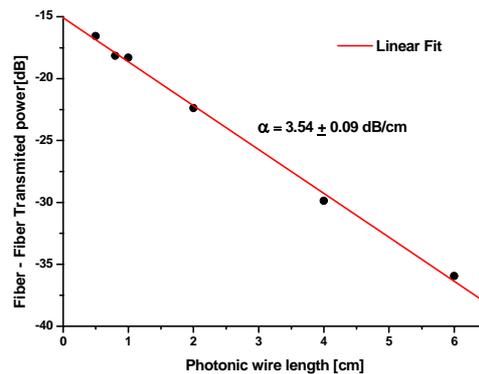


Figure 4 Linear regression of output power as a function of wire length

Conclusion

High quality deposited silicon for photonic integrated circuit is developed. The film properties are analyzed using FTIR, XRD and SE techniques. The analysis is compared with the optical measurement to extract the film quality. Single mode photonic wires were fabricated with low propagation loss. We measured a propagation loss of 3.5 and 13.4dB/cm for 500nm photonic wire fabricated from PECVD and LPCVD process respectively. To our knowledge propagation loss obtained for a-Si is the lowest loss reported in the literature.

Reference

- [1] P. Dumon et al, "Linear and nonlinear nanophotonic devices based on silicon-on-insulator wire waveguides," *Jpn. J.Appl.Phys. Part-1*, vol. 45, pp. 6589-6602, Aug 2006.
- [2] L. Liao et al, "Optical transmission losses in polycrystalline silicon strip waveguides: Effects of waveguide dimensions, thermal treatment, hydrogen passivation, and wavelength," *J. Electron. Mat.*, vol. 29, pp. 1380-1386, 2000.
- [3] R. S. D. K. Sparacin et al, "Low-Loss Amorphous Silicon Channel Waveguides for Integrated Photonics," in *Proc. Conf. Group IV photonics, 2006*, pp. 255-257.
- [4] S. K. Selvaraja et al, "Polycrystalline-silicon as waveguide material for advanced photonic applications," in *Proc. Conf. IEEE/LEOS Benelux workshop, Eindhoven, 2006*.
- [5] S. K.Selvaraja et al, "Low loss amorphous silicon photonic wire and ring resonator fabricated by CMOS process," in *Proc. Conf. ECOC, Berlin, 2007*, PDS 2.2.
- [6] S. K. Selvaraja et al, "Silicon nanophotonic wire structures fabricated by 193nm optical lithography," in *Proc. Conf. IEEE-LEOS Annu. Meeting, Florida, 2007*, pp.48-49.
- [7] D. Taillaert et al, coupler for silicon-on-insulator waveguides," *Opt. Lett.*, vol. 29, pp. 2749-2751, 2004.