

Adhesive Bonding of III-V Dies to Processed SOI Using BCB for Photonic Applications

G. Roelkens, B. Bataillou, J. Brouckaert, F. Van Laere, D. Van Thourhout, R. Baets

Department of Information Technology, Ghent University,
Sint-Pietersnieuwstraat 41, B-9000 Ghent, Belgium

The bonding process of InP/InGaAsP dies to processed SOI using DVS-bis-BenzoCycloButene was developed. Surface preparation and the degree of planarization of bonding layers thinner than 300nm were optimized. Bonding strength and bonding quality was assessed, which shows to be sufficient for post-bonding processing. The heterogeneous integration of active photonic devices fabricated in this bonding layer on top of the SOI photonic layer is described.

Introduction

Silicon-on-Insulator (SOI) is a material that is gaining a lot of importance for the fabrication of photonic integrated circuits. This is due to the high refractive index contrast between Silicon core and SiO₂ cladding layer which makes large scale integration of optical circuits possible. These can be fabricated using standard CMOS technology, which is interesting from the point of view of reproducibility, control and economy of scale (1). Although Silicon-on-Insulator is an important platform for passive optical functions, it consists of materials with an indirect bandgap, which means that it is difficult to fabricate active opto-electronic devices in this material system. For active devices at the telecommunication wavelength of 1.55μm, the InP/InGaAsP material system is used. Therefore, in order to integrate both active and passive optical functionality on a single chip, we will focus on the integration of InP/InGaAsP epilayer structures on top of passive SOI waveguide circuits. This integration process is based on the adhesive bonding of unprocessed InP/InGaAsP dies onto a processed SOI waveguide wafer using divinyl-tetramethyldisiloxane-bis-benzocyclobutene (DVS-bis-BCB) (2). The DVS-bis-BCB is spin coated on the processed SOI wafer and planarizes the topography of the wafer. For the coupling of light between the SOI waveguide layer and the InP/InGaAsP layer structure the bonding layer thickness must be typically below 300nm. In a second step the InP/InGaAsP dies are bonded onto the SOI waveguide wafer and after bonding the InP substrate is removed. This leaves the InP/InGaAsP epitaxial layers bonded to the SOI waveguide circuit and the fabrication of the active opto-electronic components can be done aligned to the underlying SOI features. The processing sequence is shown in figure 1.

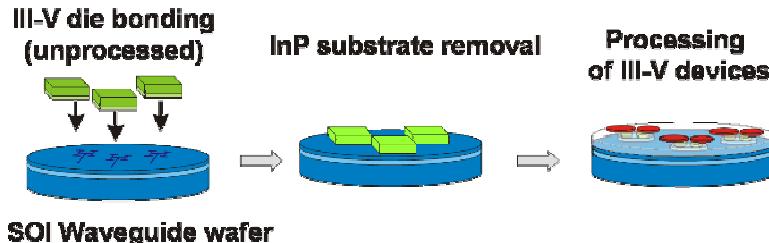


Figure 1. Heterogeneous integration of InP/InGaAsP on top of an SOI waveguide wafer by a die to wafer bonding process

DVS-bis-BCB adhesive die to wafer bonding process

As very thin bonding layers are needed, commercially available B-staged DVS-bis-Benzocyclobutene (Cyclotene 3022-35 from Dow Chemicals) was diluted using mesitylene (1,3,5-trimethylbenzene). Dilution of the DVS-bis-BCB with 150% of mesitylene leads to a bonding layer thickness of 150nm when spin coated at 5000rpm. We evaluated the planarization properties of the ultra-thin DVS-bis-BCB layers on the SOI waveguide topography. The height of the topography was 220nm while the density of the features varies over the wafer surface. Three different types of topography were investigated: 10µm wide trenches on a pitch of 30µm, 10µm wide trenches on a pitch of 120µm and an isolated step in the topography. Preliminary measurements showed that spin coating of multiple layers with the same aggregate thickness of a single layer, showed significantly better planarization properties than single step spin coating. Therefore we assessed the degree of planarization by using a double coating obtaining a total layer thickness of about 300nm. Different combinations of spin coating and curing were tried and the degree of planarization was measured as shown in figure 2.

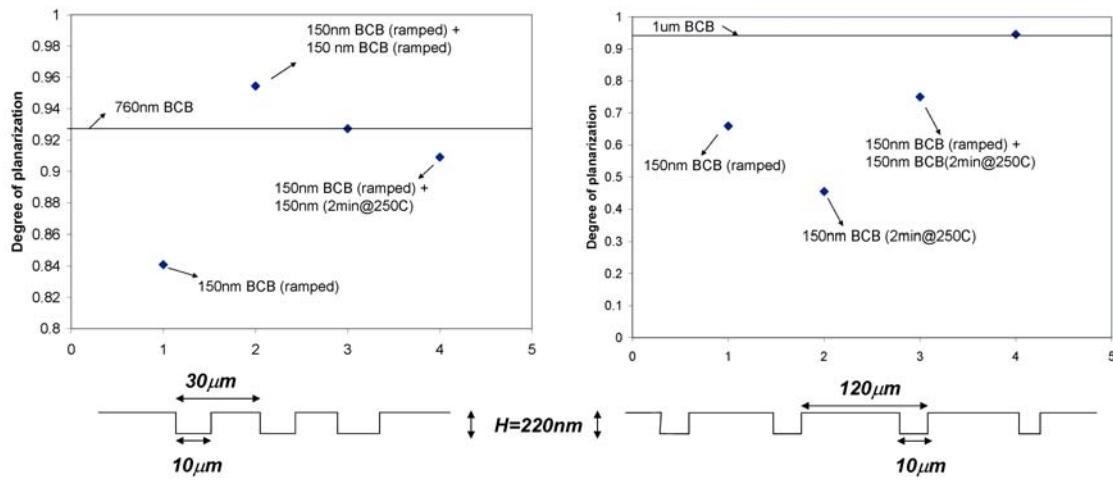


Figure 2. Degree of planarization of thin DVS-bis-BCB layers on different types of topography

From these measurements several conclusions can be drawn. First, it is clear that the planarization of the 30µm pitch features is better than that of the 120µm features. Secondly, the superior planarization properties of double spin coated layers is clear: in the case of a 30µm pitch even a higher degree of planarization can be obtained using an

aggregate 300nm BCB layer than with a single 760nm thick BCB layer. The type of curing of the first spin coated layer also plays a role. Soft-curing the BCB by slowly (1.6C/min) ramping to 210C (indicated by “ramped” in figure 2) gives a higher degree of planarization than a rapid thermal anneal (2min at 250C) due to the reflow of the BCB in the case of slow ramping.

From these results we designed the SOI topography to obtain a degree of planarization higher than 90% (meaning a residual non-planarity below 20nm). This residual non-planarity can than be compensated for by the elastic deformation of the InP surface and the partially cured DVS-bis-BCB.

The optimum degree of polymerization of the DVS-bis-BCB layer prior to bonding was evaluated by bonding unprocessed flat wafer surfaces. 300nm BCB was spin coated on a Pyrex host wafer and placed on a hot plate in a nitrogen environment at 250C for a variable time to evaporate the mesitylene solvent and partially cure the BCB. A time-temperature-transformation isothermal cure diagram is shown in figure 3 with the results of the bonding. When the DVS-bis-BCB is still liquid, the film is punctured upon attachment of the InP/InGaAsP dies. When the degree of polymerization is too high, the film is not tacky any more and dies debond. Good bonding quality is obtained by transforming the liquid BCB to a sol/gel rubber with an intermediate degree of polymerization.

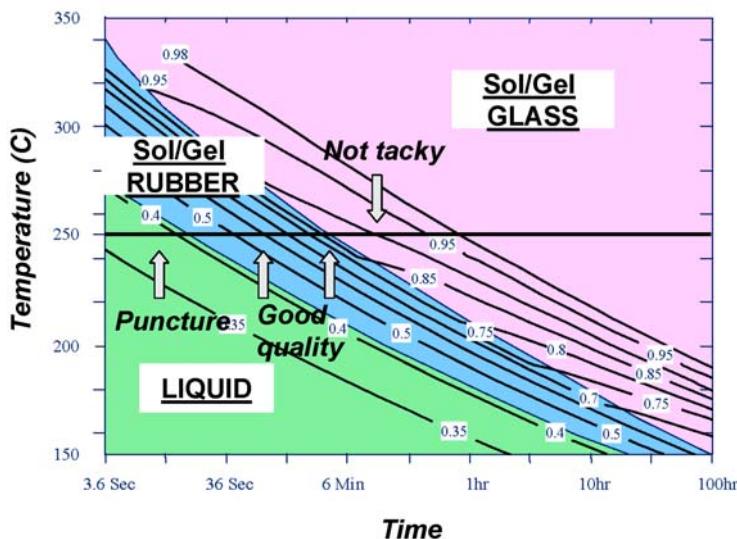


Figure 3. Time-Temperature-Transformation diagram of DVS-bis-BCB and the results of the bonding

Before bonding, the SOI waveguide substrate, with a designed topography for planarization, is cleaned using SC-1 solution ($1\text{NH}_3:4\text{H}_2\text{O}_2:20\text{H}_2\text{O}$) at 70C. This surface treatment lifts off particles from the surface and renders the surface hydrophilic. After surface cleaning, adhesion promoter AP-3000 from Dow Chemicals is applied. Mesitylene diluted Cyclotene 3022-35 is spin coated at 5000rpm on the SOI and is soft-cured (210C for 40min, ramped at 1.6C/min). Subsequently, a second layer is spin coated at 5000rpm and undergoes a rapid thermal annealing for 2min at 250C, thereby increasing the degree of polymerization into the optimal region for bonding. Both curing steps are performed in a nitrogen environment to prevent the oxidation of the DVS-bis-

BCB. The cleaved InP/InGaAsP dies (with a size ranging from a few mm² to 1cm²) are temporarily attached to a Pyrex carrier using a thermoplastic photoresist. The surfaces are cleaned by removing a sacrificial InP and InGaAs layer using 3HCl:H₂O and 1H₂SO₄:3H₂O₂:1H₂O respectively. This cleaning step removes the hydrocarbon contamination and lifts off the particles on the dies (mainly from the cleaving operation). The InP surface is conditioned for an optimal bonding strength by dipping in 1HF:10H₂O (as will be shown in the subsection on characterization of the bonded layer stack). This surface treatment renders the InP surface hydrophilic (3). The InP dies are bonded in a vacuum environment to avoid the inclusion of air at the bonding interface. The bonding is performed at 150C in order to detach the InP dies from the Pyrex carrier and are cured for 1 hour at 250C under a uniform pressure of 300kPa in a nitrogen environment.

Characterization of bonded layer structures

The die to wafer bonded structures were characterized on bonding quality and bonding strength. The bonding quality was assessed by Scanning Acoustic Microscopy (SAM) revealing no delamination at the bonding interface. Infrared transmission inspection, optical inspection by bonding on a Pyrex host substrate and SEM cross-section imaging were also performed not revealing any bonding defects. A cross-section of a bonded layer structure after InP substrate removal is shown in figure 4.

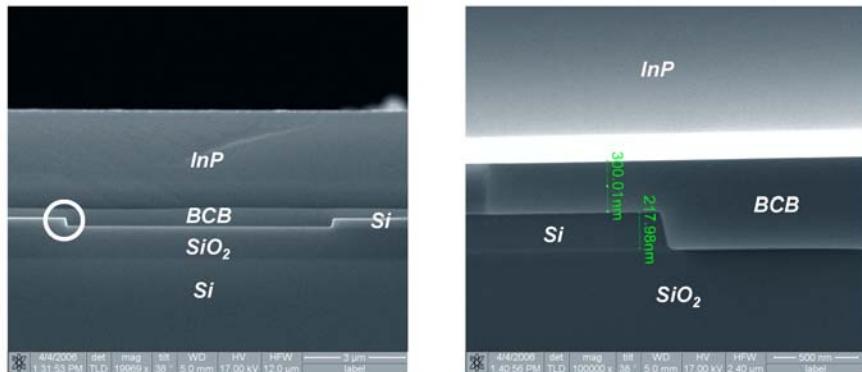


Figure 4. Cross-section and SAM top view image of a bonded layer structure. The SOI waveguide layer, BCB bonding layer and InP/InGaAsP layer are clearly distinguishable.

The bonding strength was assessed by performing die shear tests on the bonded samples. 25mm² InP dies with different surface conditioning were bonded to a Silicon host substrate and the shear force needed to detach the InP dies was measured. The results are depicted in figure 5. From these results it is clear that the HF treatment before bonding gives the highest bonding strength and that this is due to a chemical change in the surface and not due to a particle removal effect. This can be seen by comparing the results for the HF, HF+SC-1 and HF+SC-1+HF maximum shear forces. For comparison the influence of an O₂-plasma (formation of oxides on the InP surface) and the influence of an 1H₂SO₄:3H₂O₂:1H₂O surface treatment (for etching the sacrificial InGaAs layer) are also shown. The critical adhesion energy of the bonded stack was measured using the Maszara razor blade method (4). It increased from 0.2J/m² before curing to 10J/m² after curing for a bonding layer thickness of 300nm.

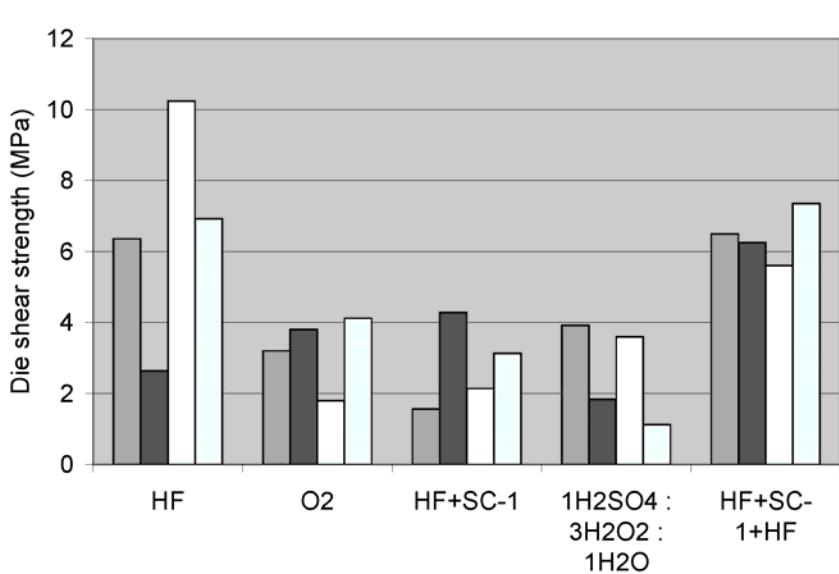


Figure 5. Maximum shear stress that can be applied to a bonded InP die bonded using 300nm of DVS-bis-BCB

Heterogeneous integration of active photonic devices

After bonding and removal of the InP substrate using a combination of mechanical grinding and chemical wet etching until an InGaAs etch stop layer is reached, active opto-electronic devices can be fabricated in this layer structure. Stand alone (not coupled to an SOI waveguide) laser diodes and light emitting diodes were fabricated and subjected to damp heat testing (85 degrees, 85% relative humidity). No degradation of the light emitters was observed showing the good quality of the adhesive bonding process.

To demonstrate the heterogeneous integration process, InP/InGaAsP photodetectors were integrated on top of and coupled to an SOI waveguide circuit. The layout of the coupling structure and bonded photodetector is shown in figure 6. An inverted taper approach is used to couple light from the SOI passive waveguide layer to a polymer waveguide above the taper structure, which is then butt coupled to the photodetector. A top view of a fabricated structure is also shown, showing the InP/InGaAsP layer structure bonded to the SOI waveguide circuit and butt coupled to the polymer waveguide. The SOI inverted taper is not visible as it is buried underneath the polymer waveguide.

Photodetectors were characterized by endfire coupling using a lensed fiber with a spot size of 2.5μm. TE polarized light is injected into an 1.2μm wide SOI waveguide and the IV-curves of the device were compared with and without illumination. We assumed that the fraction of the power that is coupled into the SOI waveguide is the theoretical value resulting from numerical simulations, thereby giving a lower limit of the responsivity of the devices. The IV-curves with and without illumination with an estimated 95μW power at 1555nm in the SOI waveguide is plotted in figure 7. This corresponds to a responsivity of 0.23A/W. The length of the device is 50μm.

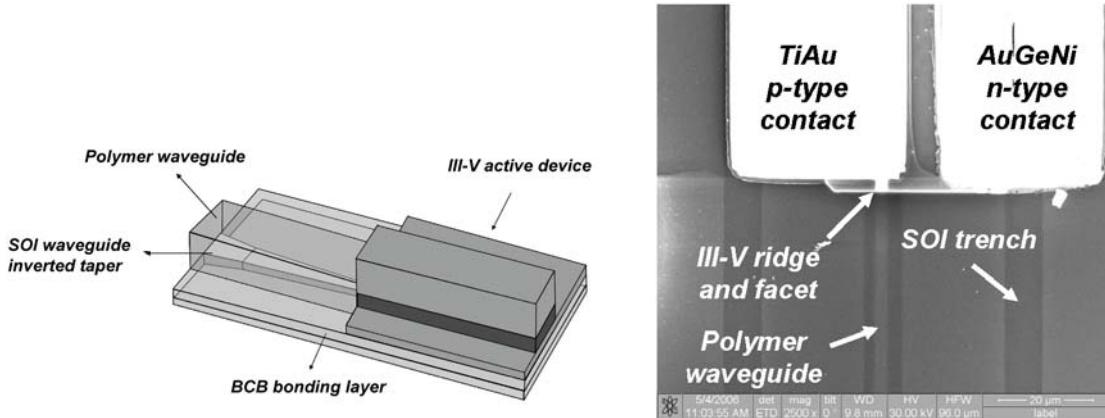


Figure 6. Layout of the bonded photodetector structure and a top view of the fabricated structure

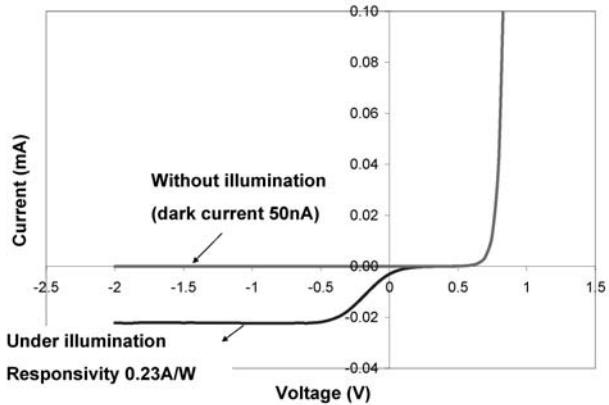


Figure 7. Current versus voltage characteristics of bonded photodetectors coupled to an SOI waveguide circuit

Acknowledgements

This work was partly supported by the European union through the Network of Excellence ePIXnet and the IST PICMOS project, by the Belgian IAP-PHOTON network, the IWT-GBOU project and the Fund for Scientific Research (FWO). The authors would like to thank Meint Smit for the fruitful discussions.

References

1. W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman and D. van Thourhout, *J. Lightwave Technol.*, **23**, 401 (2005).
2. F. Niklaus, H. Andersson, P. Enoksson and G. Stemme, *Sensors and Actuators A*, **92**, 235 (2001).
3. Y. Sun, Z. Liu, F. Machuca, P. Pianetta and W.E. Spicer, *Journ. Of Appl. Physics*, **97**, 12 (2005).
4. W.P Maszara, G. Goetz, A. Caviglia and J.B. McKitterick, *Journ. Of Appl. Physics*, **64**, 4943 (1988).