A nanophotonic 4x4 wavelength router in Silicon-on-insulator

Pieter Dumon, Wim Bogaerts, Dries Van Thourhout, Roel Baets,
Johan Wouters, Stephan Beckx and Patrick Jaenen

Promoter(s): Roel Baets

Abstract—**We fabricated and packaged a very compact 4x4 wavelength router in Silicon-on-insulator. This device is for use in a 10 gigabit/s optical backplane interconnect based on tuneable lasers and wavelength routing. Fabrication was done using CMOS compatible processes, enabling volume fabrication. The router consists of a very compact arrayed waveguide grating using submicron waveguides and bend radii of just 3μm. This is achieved by exploiting the very high refractive index contrast. By applying a double etch scheme, the insertion loss of the arrayed waveguide grating has been reduced to 3.5dB for the best routing path. Vertical fibre couplers are used to interface to an standard eight-fibre array connector. The resulting total fibre-to-fibre insertion loss of the router is 12.5dB. The crosstalk level is still -12 to -14dB, which is within spec for the envisaged application.**

Keywords—**Nanophotonics, arrayed waveguide grating**

I. Introduction

THE compact waveguide bends that can be achieved with high index contrast semiconductor waveguides allow for very small integrated devices, raising the integration scale. In this way, more functionality can be achieved on a smaller die size. In Silicon-on-insulator (SOI) wire waveguides, bend radii of just a few m can have ultra-low losses. This material system is therefore an attractive option for passive integrated wavelength routing devices. However, high device performance, low fibre to chip insertion losses and packaging are all more difficult issues with higher index contrast systems. Here we present a 4x4 arrayed waveguide grating (AWG) fabricated in Silicon-on-Insulator with CMOS processing techniques. It is based on nanophotonic wire waveguides of about 500nm width and using a bend radius of just 3 m. This wavelength router operates in the C-band. The device is connected to fibres using vertical fibre couplers and an eight-fibre array connector. The pigtailed device is mounted in a housing together with a Peltier element and thermistor for temperature control.

II. Silicon-on-insulator AWG

STRUCTURES are etched in SOI wafers with a 220nm thick Si top layer and a 1m buried oxide. Patterns are defined in resist using 248nm deep UV lithography [1]. To create high-index contrast waveguides, the Si layer is etched through. These waveguides support a TE mode with propagation losses of about 2.5dB/cm for a 500nm wide wire [2]. Bends used in the AWG have a 3m radius, with a measured excess loss lower than 0.01dB for a 90 bend.

P. Dumon, W. Bogaerts, D. Van Thourhout and R. Baets are with the Department of Information Technology, Ghent University (UGent), Gent, Belgium. E-mail: Pieter.Dumon@UGent.be . J. Wouters, S. Beckx and P. Jaenen are with the Interuniveristy MicroElectronics Centre, Leuven

In order to couple to fibre, grating couplers are used [3]. These couplers convert the mode between a broad access waveguide and the fibre mounted under an angle of 9 from the vertical axis. The gratings are created in a more shallow etch step preceding the 220nm deep etch. Currently a simple linear taper converts between the access waveguides and the narrow wires. The shallow etch step is used to create star couplers with a lower index contrast too. By using a lower index contrast, insertion losses in the star couplers are reduced [4]. After etching shallow gratings and star couplers and deep wires, the die is covered with a 750nm thick top silica layer. This enhances the fibre coupler transmission and serves as a passivating and protective cover. Additionally, fibre coupler transmission is enhanced by applying a better index matching material (glue) between fibre and chip. Note that the inputs of the device must be polarization controlled. A polarisation diversity scheme can resolve this [5].

The fibre-to-chip insertion loss with an air gap between the fibre and top silica cladding is about 5dB (>30%) with a 3dB bandwidth of 30nm, estimated from the transmission of the shortest alignment waveguide on the chip.

Figure II shows the mask design, with a 300 m x 150 m AWG and 8 access waveguides with grating couplers. In the centre, additional fibre couplers and waveguides are used for alignment.

III. Characterization and coupling to fibre

CHARACTERIZATION and final pigtailing of the device is done with a commercially available eight-fibre array connector. This assembly consists of single-mode fibres in Silicon V-grooves with a pyrex top lid. The fibre spacing is a standard 250m. The facets are polished under an angle of 8 and the connector is mounted under a 9 angle. Because of the resulting 1 tilt between fibre facets and sample, the connector can rest on the sample without damaging the fibre cores (or the AWG, which is much smaller than the connector). The connector is first aligned to the chip visually using on-chip markers and then actively using alignment waveguides connecting fibres two by two. Due to the large alignment tolerances of the fibre couplers [3], this first alignment is very fast. In a next step, the in-plane rotational alignment and a possible tilt between connector and chip in the direction of the array are corrected for. The connector is then moved in-plane to align with the AWG access grating couplers and the connector is moved downwards. In this stadium the device can be characterized.

In order to obtain a packaged device, the connector is attached to the chip using UV-cureable glue, which also serves as an index-matching material. The connector with chip is mounted on an Aluminium plate on top of a Peltier element for temper-

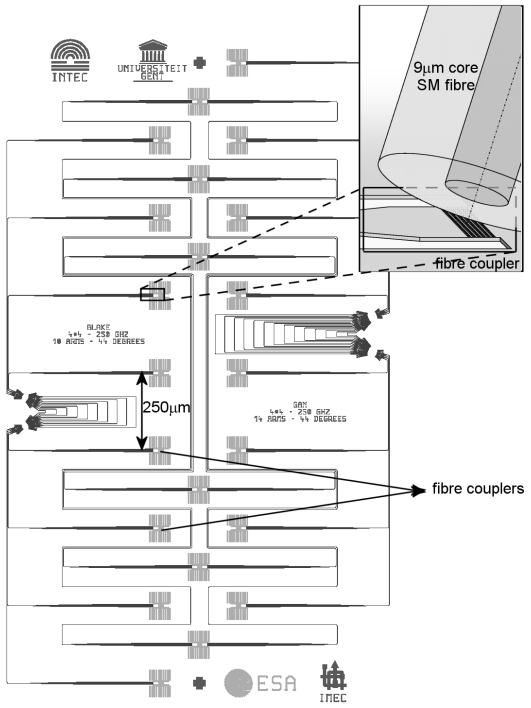

Fig. 1. mask layout with AWG and fibre couplers. Spacing between the couplers is 250 m, compatible with a standard array connector

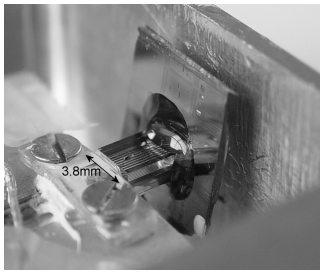

Fig. 2. picture of the fibre pigtailed device. Cleaved chip area is much larger than actually needed.

ature control. An Aluminium box serves as a housing for the component and as the thermal ground. Figure III shows a picture of the chip with attached connector, mounted in the housing box. The sample hangs in the air, with a highly conductive but still fairly long thermal path (aluminium + silicon) between Peltier element and chip. For the next generation, a more compact packaging approach will be used.

IV. Performance of the packaged AWG

THE AWG has a channel spacing of 250GHz and a 1THz designed free spectral range (FSR). Figure IV shows the fibre to fibre transmission spectra from input 3 to all outputs. The actual FSR is slightly larger (1.025THz). Fibre-to-fibre insertion losses are between 12.5 and 17dB depending on the route and wavelength channel. We measured the insertion loss of the actual AWG to be 3.5 dB for the best channel combination. The coupling loss is therefore about 4.5dB. The sidelobe level (crosstalk) is -12dB to -14dB. This performance enables the device to be used in a reconfigurable interconnect network

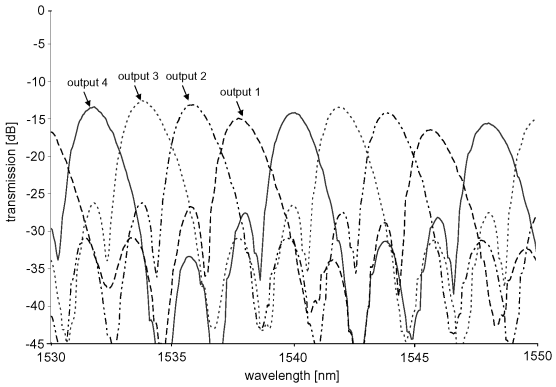

Fig. 3. Fibre to fibre transmission of the pigtailed device, from input 3 to all outputs

based on a combination of tuneable lasers and this passive wavelength router.

Due to the strong light confinement and high index contrast, wavelength filters in SOI are rather sensitive to temperature. On the other hand, we tuned the AWG for over 1nm with a 10C temperature change.

V. Conclusions

WE fabricated and packaged a 4x4 wavelength router based on an arrayed waveguide grating, vertical fibre couplers and a fibre array connector. The channel spacing is 250GHz. AWG insertion loss has been reduced by a double etch scheme. Best fibre to fibre insertion loss is 12.5dB with an actual device insertion loss of 3.5dB. The crosstalk level is about -12dB.

Acknowledgments

This work was carried out in the context of the ESA/ESTEC multigigabit optical backplane project, and supported by the E.U. through the IST-ePIXnet NoE. P. Dumon thanks the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT-Vlaanderen) for a specialization grant. W. Bogaerts acknowledges the Flemish Fund for Scientific Research (FWO).

References

[1] W. Bogaerts et al *Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology*, IEEE Journal of Lightwave Technology, 23(1), pp. 401-412, 2005.

[2] P. Dumon et al *Low-loss photonic wires and ring resonators fabricated with deep UV lithography*, IEEE Photonics Technology Letters, 16(5), pp. 1328-1330, 2004.

[3] D. Taillaert et al, *An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers*, IEEEJournal of Quantum Electronics, 38(7), pp. 949-955, 2002.

[4] C. van Dam et al, , IPR 1996, Boston, MA, pp. 52-55.

[5] D. Taillaert et al, *A compact two-dimensional grating coupler used as a polarization splitter*, IEEE Photonics Techn. Letters, 15(9), 2003, pp. 1249-1251