Technologies for On-Chip Optical Interconnects

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Abstract We propose an integration approach for on-chip optical interconnect compatible with waferscale processing technologies and future advanced electronic circuits. The use of ultra-compact SOI-based wiring circuitry is demonstrated. First heterogeneously integrated optoelectronic devices coupled to these waveguides are shown.

Introduction

In future generation electronic circuits, a severe bottleneck is expected on the global interconnect level. With decreasing device dimensions, it is increasingly difficult to keep propagation delays acceptable and even with the most optimistic estimates for conductor resistivity and dielectric permittivity, the performance roadmap projected by the ITRS will not be met. Therefore there is a need for radically different interconnect approaches and one of the most promising solutions is the use of an optical interconnect layer. An optical interconnect layer could allow for an enormous bandwidth increase, for immunity to electromagnetic noise, for a decrease in the power consumption, the possibility for synchronic operation within the circuit and with other circuits and for a reduced immunity to temperature changes. In the context of an EU-funded project (IST-PICMOS), we are investigating the feasibility of adding a photonic interconnect layer on top of silicon CMOS-circuitry, in a way which is compatible with future generations of electronic circuits, both in terms of fabrication and in terms of cost.

Integration strategy

Figure 1 shows the proposed integration scheme. In a first step, the required passive optical interconnect circuitry is realised (the waveguide wafer). Subsequently, III-V dies containing suitable epitaxial layers are bonded top-down on the waveguide wafer and their substrate is removed using a combination of mechanical polishing and wet etching techniques [3]. In a next step, the required optoelectronic devices (sources, modulators, detectors) are collectively processed (mesa definition, metallization). This allows a wafer-scale alignment of the optoelectronic devices with the underlying passive waveguides using lithographic techniques and thereby avoids the costly alignment procedures required in classic hybrid integration approaches based on flip-chipping techniques.

In a last step the photonic layer consisting of the waveguide wafer integrated with the optoelectronic devices can be bonded on top of the CMOS-wafer, after which the necessary electrical connections can be made and the dies are separated for packaging.

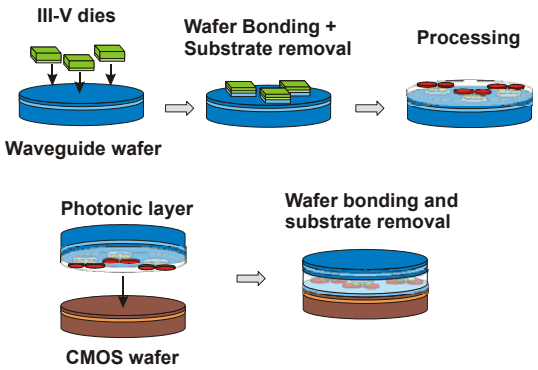

Figure 1 Integration approach for realising on-chip optical interconnect layer

Silicon wire waveguides for on-chip optical interconnect

Different approaches have been proposed for realizing the passive photonic interconnect circuitry, including SiN and polymer waveguides. We recently demonstrated the possibility for realizing sub-micron Silicon wire waveguides using 248nm DUV-lithography and CMOS-compatible technologies [2]. Due to the extremely high index contrast in both horizontal and vertical direction, very compact and high density circuits can be realized. Figure 2 shows the minimal allowable pitch (crosstalk < 20dB over 1 cm for 2 neighboring waveguides) as function of the Silicon wire width, for different heights of the core. Also the bend loss as function of the bend

radius is shown, demonstrating negligible radiation losses for R>2μm [1]. SOI wires further may open the possibility for more complex interconnect strategies using WDM-techniques by incorporating compact wavelength selective devices based on micro-resonators. Issues that remain to be solved are the sensitivity to process deviations and the realization of low loss intersections.

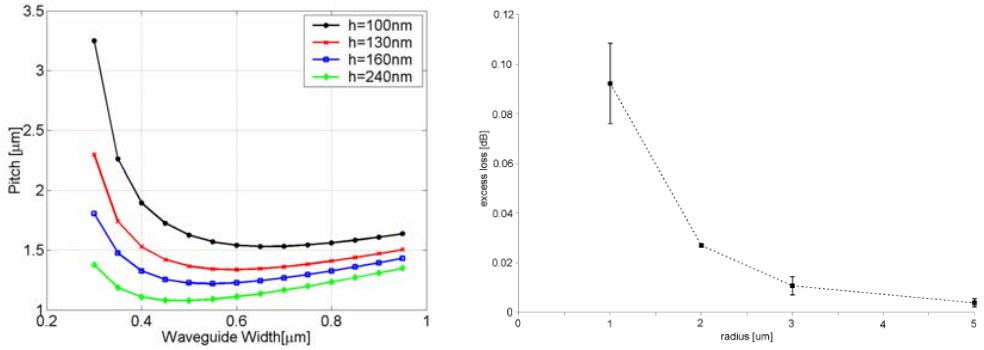

Figure 2 Minimum allowable center-to-center spacing for a maximum crosstalk of 20dB/cm (left) and bend loss (right)

Heterogeneously integrated optoelectronic devices

Some of the optoelectronic devices and the different coupling strategies being investigated are shown in Figure 3. The left picture shows a micro-DBR-laser evanescently coupled to the underlying SOI waveguides. By changing the intermediate layer or the coupling length, the compromise between threshold current and attainable output power can be optimized. Optimizing the metal contact for minimal absorption is one of the main issues. The right picture shows detectors fabricated on compact ($10x10\mu m^2$) grating couplers before the final metallization step.

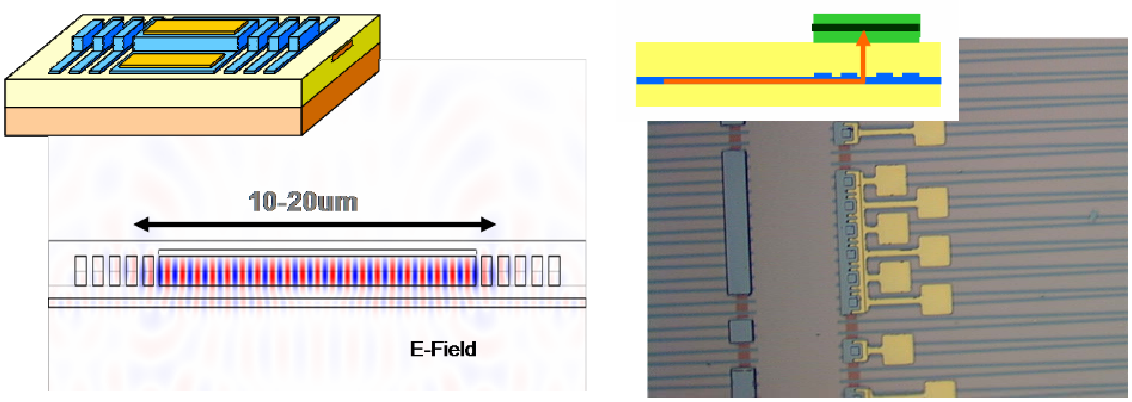

Figure 3 Micro-DBR laser evanescently coupled to Silicon wire waveguide (left). Silicon wire waveguide coupled to detector using grating coupler

Conclusions

We propose an integration approach for on-chip optical interconnect compatible with waferscale processing technologies. Ultra-compact photonic wiring circuitry is demonstrated. First heterogeneously integrated optoelectronic devices coupled to SOI waveguides are realized.

Acknowledgment

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References

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