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## E2 (Invited)

# SILICON-ON-INSULATOR BASED HIGH INDEX CONTRAST WAVEGUIDE DEVICES: RESEARCH IN EUROPE

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***Abstract:*** *This paper provides a short description of three European projects in which Silicon-on-Insulator based high index contrast waveguide devices play a prominent role. These projects include the European Network of Excellence FP6-ePIXnet, the European research project on on-chip optical interconnect FP6-PICMOS and the European Space Agency project on Multi-Gigabit Optical Backplane Interconnections.*


### 1. Introduction

In recent years a new technology has been emerging from research labs worldwide: the use of standard Silicon-on-Insulator (SOI) wafers and standard Silicon processing technologies to create ultra-compact so-called "nanophotonic" components and circuits in Silicon [1-3]. In these circuits one uses high refractive-index-contrast single-mode waveguides with a cross-section of the order of the wavelength squared to make passive or active devices. The core of the waveguide is Silicon while the cladding is either a dielectric such as silica or air. The waveguide can be a conventional waveguide based on guiding by total internal reflection or a photonic crystal waveguide based on guiding by Bragg diffraction. The active functions – light emission, modulation, switching, amplification, detection - can be based on the properties of Silicon itself or on the properties of a special cladding material.

The term "nanophotonic" calls for some interpretation. The typical smallest feature sizes – widths, thicknesses, lengths – in wavelength-scale photonic structures are in the range of one tenth of a wavelength to one wavelength. For operation at a wavelength of 1550 nm for example – corresponding to a wavelength in Silicon of about 500 nm – the required smallest feature sizes are typically between 50 and 500 nm. This matches nicely the capabilities of present day's CMOS technology. However, the accuracy and reproducibility of the spectral behavior of the optical functions are directly correlated to the geometric accuracy of these features in the device. As a rule of thumb one can say that a spectral accuracy of 1 nm (relative to a wavelength of 1550 nm) translates into a geometric accuracy of 1 nm (relative to a feature size of 50-500 nm). Furthermore the high-index contrast interfaces in these devices need to be smooth down to the 1 nm level to avoid scattering losses.

This means that the development of SOI-based nanophotonic ICs present a number of challenges both at the design level and in the fabrication technology. Over the past few years tremendous progress in the performance of SOI waveguides and waveguide circuits has been reported worldwide. While most work is based on the use of electron-beam lithography for defining the patterns with nanometric accuracy, there has also been considerable work on using mainstream CMOS optical lithography tools for the patterning. This opens the way to low-cost volume manufacturing of very advanced photonic circuits.

In Europe there are probably about 20 research labs and institutes that are active in research on SOI-based nanophotonics. In this paper we will describe three ongoing European projects, coordinated by the authors, in which SOI nanophotonic circuits made by means of CMOS tools play a prominent role.

### 2. ePIXnet (European Network of Excellence on Photonic Integrated Components and Circuits)

ePIXnet is a European Network of Excellence (NoE) [4] with photonic integration as leading thread. The integration of complex or high performance photonic functions will become the key enabler for a cost-effective and ubiquitous deployment of photonics in a wide range of applications, including ICT, sensors and biomedical applications. The network brings together 34 academic and industrial actors and contributes to the quality of education and research by stimulating long lasting partnerships and by providing access to unique facilities and knowledge in the field.

This is particularly relevant for the field of photonic integration because the technologies needed for photonic integrated components and circuits are characterised by high investment and exploitation cost. This calls for more integration of research at an international level.

The NoE focuses on five major themes: photonic integration technology, nanophotonics, advanced semiconductor materials, ultrafast light sources and ultrafast signal processing. The backbone of the Network is formed by 14 activities.

One of those activities focuses specifically on nanophotonic circuits in SOI based on CMOS-compatible process technology. This integration activity will exploit the maturity of advanced CMOS process technology, available at IMEC, Belgium, for the fabrication nanophotonic circuits in SOI. With this

technology, we have already demonstrated nanophotonic waveguides with very low propagation losses [1,5]. The partners in this SOI-oriented research activity involve, apart from Ghent University-IMEC, the Technical University of Denmark (COM), CNRS lab IOTA, the University of Twente (MESA), KTH-Stockholm, the University of St Andrews, Glasgow University, the University of Valencia, RWTH Aachen and AMO.

For the pattern definition, deep UV lithography is used. The very high cost of CMOS process technology motivates the approach of sharing access to a single facility and sharing the cost of masks and processing. In the course of the projects, a number of masks are compiled, using contributed designs from a number of partners. These designs are then fabricated together and distributed among the partners for characterisation. A similar collaboration have been carried out in the framework of the now-finished European IST-PICCO project, with successful results [6,7,8].

For the first design-fabrication-measurement cycle within the ePIXnet project, 4 partners contributed designs to the mask. Figure 1 shows an example of a $11^{th}$-order filter consisting of cascaded Mach-Zehnder interferometers in photonic wire waveguides.

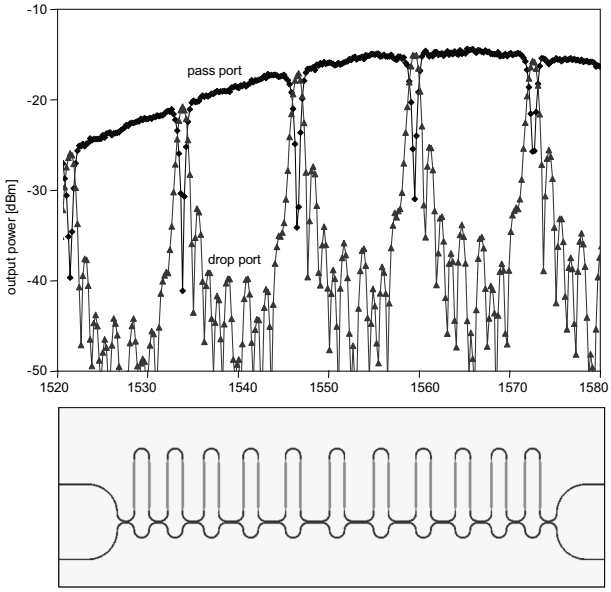


*Figure 1: 11-stage cascaded Mach-Zehnder filter with its pass and drop transmission spectrum.*

Also, within the same workpackage, similar devices are made at partners' facilities using alternative pattern definition technologies, like e-beam lithography, focused ion beam or nanoimprint lithography. This allows for a direct comparison with deep UV lithography.

## 3. PICMOS (Photonic Interconnect Layer on CMOS by Wafer-scale Integration)

For future generation electronic circuits a severe bottleneck is expected on the global interconnect level. One of the most promising solutions is the use of an optical interconnect layer. The EU-funded FP6-PICMOS-project will demonstrate the feasibility of adding a photonic interconnect layer on top of silicon electronic ICs [9]. The partners of this project involve Ghent University-IMEC, ST Microelectronics, CEA-LETI, Ecole Centrale de Lyon, TRACIT, NCSR-Demokritos and Technical University of Eindhoven.

This interconnect layer will be fabricated by a combination of wafer bonding and wafer-scale processing steps. It will be planar and will be built from a high-density passive optical wiring circuit in SOI integrated with InP-based sources and detectors using a wafer bonding approach.

The enormous advantage of using sub-micron Silicon wire waveguides for on-chip optical interconnect is the possibility for reaching very high data densities. Because of the strong mode confinement, the centre-to-centre spacing of neighboring waveguides can be smaller than 1.2um. In addition extremely small bending radii can be reached. For a bending radius of 2um, the measured bending loss is smaller than 0.03dB/90$^o$ [10]. In the future one could think of using ultra-compact resonators to exploit the possibilities of wavelength demultiplexing and further increase the data density.

The main challenge of the PICMOS-integration approach, which is based on the bonding of suitable III-V-based epi-layers on top of the SOI waveguide circuits and a collective postprocessing step for realizing the sources and detectors, is the design of an efficient coupling structure between the active optoelectronic devices and the SOI-waveguides. Figure 2a shows an electrically connected micro-disk laser to be evanescently coupled to an underlying SOI-waveguide.

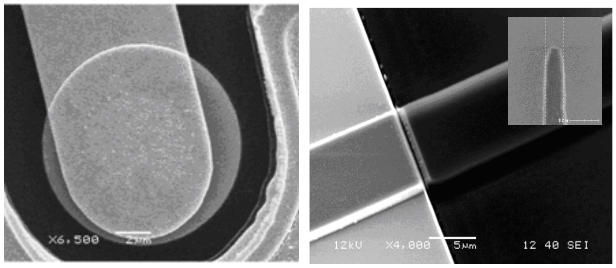


*Figure 2: Electrically connected III-V Micro-disk (left) and FP-laser coupled to SOI-taper using polymer overlay (right).*

Figure 2b shows a Fabry-Perot-laser coupled to the SOI waveguide circuits using an intermediate polymer overlay [11]. To facilitate this coupling very narrow (~100nm) SOI-taper tips are required. Normally these are out of reach of standard 248nm DUV lithography. However, we demonstrated such tapers using a

combination of resist and hard mask trimming. Also successful low-loss fiber-to-chip couplers using an inverted taper approach were demonstrated using these narrow taper tips. Next to the approaches shown in Figure 2, also grating-based coupling was demonstrated.

## 4. ESA-project on Multigigabit Optical backplanes

This project aims at demonstrating a multigigabit optical backplane based on a passive arrayed waveguide grating (AWG) router and wavelength tunable transmitters. The optical backplane is expected to solve the interconnect bottleneck in spacecrafts and satellites which is created by the introduction of high data rate sensors and on-board processing of sensor data. The project is coordinated by Ghent University-IMEC and other partners are Intune Technologies (Dublin) and NCSR-Demokritos (Athens).

A 4x4 AWG in SOI is developed in this project as an alternative to currently available Silica-on-Silicon AWGs. SOI allows much smaller dimensions, and in principle the AWG can be integrated with other passive components such as couplers [12]. This in turn will allow the fabrication of more complicated routers (e.g. also allowing multicasting) in the future. Specifications for the AWGs to be used in the demonstrator included a crosstalk of less than -12 dB and a fibre-to-fibre loss of less than -17 dB.

For the packaging of the SOI AWGs, use has been made of vertical fibre coupling gratings [13]. These are one-dimensional shallow gratings, coupling the beam incident from the SM fibre to a broad (10μm) SOI waveguide and vice versa. Eight couplers on the chip, spaced 250 μm apart, serve as input and output ports, connected themselves to the router structure by tapers. The fibre array connector, with fibres mounted in V-grooves, is then glued under an angle to the SOI chip and the arrangement is put in a protective housing. A picture of the fibre array glued to the router is shown in Figure 3. The transmission characteristics vs. wavelength at the different output ports are shown in Figure 4 for an input at port 3.

Backplanes for space applications need to comply with extra requirements, e.g. they have to be very robust and able to survive launch conditions. They also have to exhibit radiation hardness. For this reason, the radiation hardness of both the tunable transmitters and of AWGs in various technologies (SoS, SOI, polymer) has also been investigated in the project.

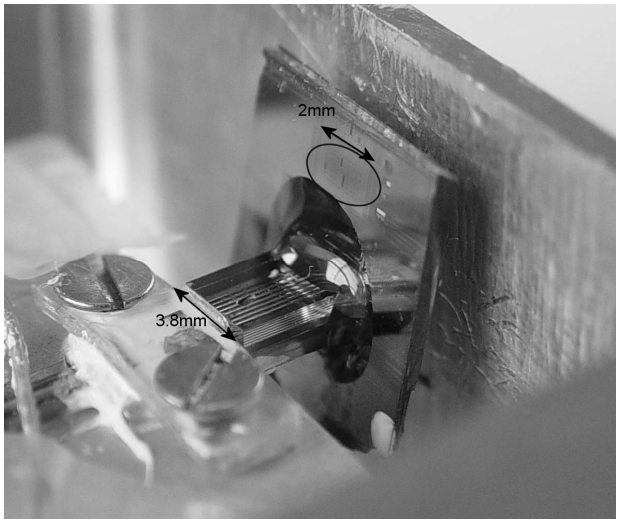


Figure 3: Picture of the fibre array glued to the SOI chip.

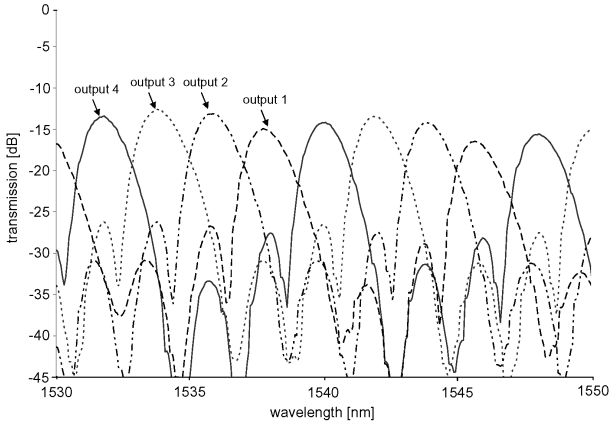


Figure 4: Wavelength characteristics of the different output ports for an input at input port 3.

## 5. Conclusions

In just a couple of years Silicon-on-Insulator has become a major platform for photonic integrated circuits. This is due to its compatibility with both nanophotonic integration concepts and with the technological capabilities of advanced CMOS technology.
In spite of early attempts to deploy this platform commercially there is still a multitude of very tough research challenges. The necessity of access to advanced CMOS research and prototyping facilities calls for a strong international collaboration approach to address these challenges..

## 6. Acknowledgement

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