Building Blocks and Subcircuits for Programmable Silicon Photonic Circuits

Bouwstenen en subcircuits voor programmeerbare circuits in siliciumfotonica

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Acknowledgement

If a few years ago you asked me what do I think about doing a Ph.D. in Photonics Engineering, most probably my reply to you would be *"Photonics what???"*. When I arrived in the Photonics Research Group, $3/4$ of a decade ago, I had absolutely no idea what photonics was about. *"Light on a chip? What for? How? And why?"*. Those were more or less my thoughts when I stumbled upon this job opportunity to join the PRG and help the development of the IPKISS framework. I entered this group as a software engineer and now, seven and a half years later, I'm proud to be a Photonics Engineer. None of this would be possible if I didn't have the trust and support of my supervisor, Prof. Wim Bogaerts. I still don't know how I convinced him on giving me a position as Ph.D. student, as I had virtually zero experience in photonics at the time, but he trusted me and gave me all the necessary support to make it happens, and things seems to have worked out. I extend my gratitude to all the professors in the PRG, who work hard to guarantee the excellence of this group.

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And, finally, I hope this work might inspire more people to join the programmable photonics front, which I believe (and hope) has a bright future ahead.

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Antonio Ribeiro

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List of Acronyms

A

AWG	Arrayed Waveguide Grating
ASPIC	Application Specific Integrated Photonics Circuit

B

BEOL	Back End of the Line
BC	Backcoupling
BOX	Buried oxide
BS	Backscattering
BUL	Basic Unit Length
BW	Bandwidth

C

CMOS	Complementary metal–oxide–semiconductor

D

DC	Directional Coupler
D.C.	Duty Cycle

E

EIC	Electronics Integrated Circuit
ER	Extinction Ratio

F

FDTD	Finite Difference Time Domain
FEM	Finite Element Methode
FEOL	Front End of the Line
FPGA	Field Programmable Gate Array
FPPA	Field Programmable Photonics Array
FPPIC	Field Programmable Photonics Integrated Circuit
FSR	Free Spectral Range

G

GC	Grating Coupler

I

IC	Integrated Circuit
IL	Insertion Loss

M

MZI	Mach Zenhder Interferometer
MMI	Multi-mode Interferometer
MPW	Multi-project Wafer

O

P

PCell	Parametric Cell
PDM	Phase Difference Monitor
PIC	Photonics Integrated Circuit
PS	Phase Shifter
PWM	Pulse Width Modulation

R

RR	Ring Resonator

S

SOI	Silicon on Insulator

T

W

WG	Waveguide

Nederlandse samenvatting –Summary in Dutch–

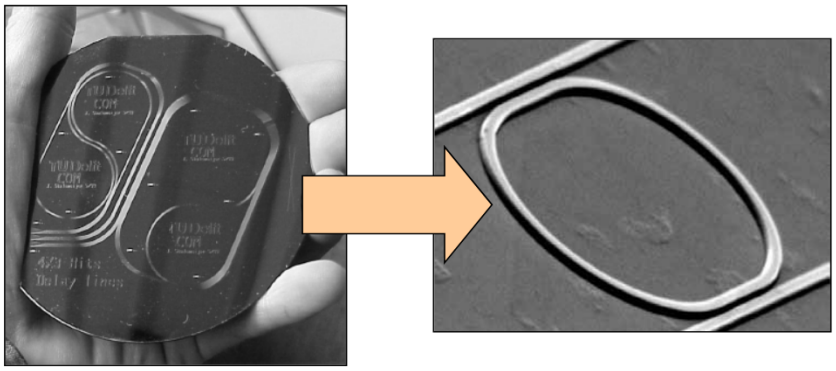
Fotonica speelt vandaag de dag een belangrijke rol in de wereld, met toepassingen op meerdere gebieden zoals detectie, beeldvorming, microscopie en hogesnelheidscommunicatiesystemen, waar een groot deel van de verbindingen gebruik maakt van licht als informatiedrager.

In dit werk bespreken we de mogelijkheden om de implementatie van fotonische circuits (*Photonics Integrated Circuits* of PIC's) uit te breiden om zo softwaregedefinieerde functies in optische chips mogelijk te maken. Hiermee willen we een functie-agnostisch optisch circuit implementeren dat na fabricage via software geconfigureerd kan worden om, door de gebruiker gedefinieerde, willekeurige functies te implementeren.

Siliciumfotonica

Siliciumfotonica is de technologie die de implementatie van fotonische circuits op een siliciumchip mogelijk maakt. Door het hoge indexcontrast tussen de materialen die gebruikt worden voor de golfgeleiderkern en -mantel (respectievelijk Silicium en Siliciumoxide), siliciumfotonica om optische circuits drastisch miniaturiseren. Dit maakt het mogelijk om een groot aantal optische functies op eenzelfde chip te integreren met behulp van de fabricagetechnologie die ontwikkeld was voor de elektronica-industrie, en in het bijzonder voor de fabricage van *complementary metal oxide semiconductor* (CMOS) elektronica.

Aangezien silicium fotonica compatibel is met de toestellen en processen van de CMOS-industrie, erft het platform de voordelen van de technologie zoals een hoge fabricagecapaciteit en nauwe integratie met elektronica. Deze integratie met elektronica, gecombineerd met de hoge thermo-optische coëfficiënt van silicium, maakt de implementatie van optische faseverschuivers mogelijk met behulp van eenvoudige lokale warmte-elementen ("heaters"). Deze heaters kunnen niet alleen gebruikt worden om het circuit te stabiliseren, maar ook om actieve componenten zoals afstembare optische koppeling te implementeren. Deze eigenschappen van het platform openen mogelijkheden voor de implementatie van grootschalige configureerbare fotonische apparaten die de mogelijkheden van PIC's kunnen uitbreiden.



Figuur 1: Siliciumfotonica maakt de miniaturisatie van optische circuits mogelijk door het hoge indexcontrast tussen golfgeleiderkern en -mantel (respectievelijk silicium en siliciumoxide).

Programmeerbare PICs

De huidige state-of-the-art silicium PIC's zijn meestal zeer gespecialiseerde circuits, zorgvuldig ontworpen om één enkele functie te implementeren voor een specifieke toepassing. Dit type circuit kunnen we daarom een *application-specific photonics integrated circuit* (ASPIC) noemen en deze beschrijving geldt voor vrijwel alle fotonische chips die momenteel op de markt zijn. Omdat elk circuit is ontworpen om één specifieke functie te vervullen, kunnen ze zeer performant zijn (zoals laag inkoppelverlies, optimaal stroomverbruik, etc.), maar dit tegen een kostprijs: flexibiliteit. Om een oplossing met een ASPIC te implementeren, moet men het optische circuit tot op het niveau van de geometrie ontwerpen, elk onderdeel van het apparaat simuleren (in de meeste gevallen met behulp van zware fysieke simulaties) alvorens een prototype te maken, dat soms maanden fabricagetijd vergt.

Ditzelfde probleem werd in het verleden door de elektronica-industrie ondervonden, en het werd verholpen door de introductie van programmeerbare chips, zoals *microprocessors* en *field-programmable gate arrays* (FPGA). Dit zijn geïntegreerde schakelingen die zijn ontworpen om na fabricage door een klant of een ontwerper te worden geconfigureerd, en dit door middel van programmering in software. Dit verhoogt de flexibiliteit van het apparaat drastisch, en verkort de ontwikkeltijd voor een nieuwe toepassing.

Programmeerbare fotonica breidt de huidige PIC-technologie uit om de implementatie van volledig programmeerbare siliciumfotonica-circuits mogelijk te maken. De functies van deze circuits worden gedefinieerd via het programmeren van de chip na fabricage en de chips kunnen worden gebruikt voor een breed scala aan toepassingen.

Bouwstenen en subschakelingen voor programmeerbare fotonica

Om dergelijke programmeerbare fotonische circuits te implementeren hebben we een groot deel van dit werk gewijd aan de ontwikkeling en optimalisatie van de bouwstenen en componenten die gebruikt worden in de circuits. Anderzijds hebben we ook gewerkt aan de verfijning van de noodzakelijke technieken voor het aansturen en besturen van fotonische circuits, inclusief optimalisatiealgoritmen en terugkoppelingen (feedback loops).

We beginnen onze discussie met de implementatie van optische faseverschuivers en afstembare optische koppelingen. We demonstreren verschillende implementaties van thermo-optische faseverschuivers en bespreken hoe we hun kenmerken, zoals vermogensrendement en snelheid, kunnen aanpassen door de geometrie van de *heaters* die gebruikt worden bij de implementatie ervan aan te passen. We breiden ons werk uit door te bespreken hoe we een diode in serie kunnen integreren met de *heater*, wat een asymmetrie in de IV-respons van het element creëert, die op zijn beurt kan worden gebruikt om tijd-multiplexed toegang tot de *heaters* te implementeren.

We bespreken de implementatie van MZI-gebaseerde optische koppelingen en de impact van de implementatie van MZI's met imperfecte componentes zoals bijvoorbeeld directionele koppelaars met een andere koppelingsverhouding dan $50/50$, die kunnen leiden tot niet-ideale prestaties voor onze afstembare koppelaars. Om dit probleem aan te pakken demonstreren we een $2 \times 2 \times 2$ afstembare koppelaar die een correcte koppeling waarborgt over het gehele bereik van $0,00\%$ tot $100,0\%$, met lage optische verliezen en een hoge onderdrukkingsverhouding van het ongewenste kanaal, en dit zelfs wanneer de directionele koppelaars incorrect gefabriceerd zijn, tot zelfs een onevenwichtige koppelingsverhouding van $25/75$.

Met de toename van de omvang en het aantal afstembare elementen in fotonische circuits hebben we een gelijke toename van het aantal elektrische aansluitingen en stroombronnen die nodig zijn voor het aansturen van de schakeling. Om dit schalingsprobleem aan te pakken hebben we technieken ontwikkeld om meerdere elektro-optische componenten met minder elektrische bronnen aan te sturen. Hiervoor hebben we een digitale aandrijftechniek geïntroduceerd die het gebruik van *Pulse Width Modulation* (PWM) voor het aansturen van de faseverschuivers mogelijk maakt. Dit, gecombineerd met het gebruik van heaters met geïntegreerde diodes, maakt het mogelijk om meerdere elementen in een afstembare circuit tegelijk aan te sturen in de tijd. Dit vermindert drastisch het aantal elektrische contacten en de stroombron die nodig is om het circuit te bedienen.

Om de werking van afstembare fotonische componenten te verbeteren, bespreken en demonstreren we de implementatie van gesloten terugkoppelingscircuits om een nauwkeurige aansturing van fotonische circuits te realiseren. Dit gebeurt door het gebruik van optische meetpunten voor vermogens- (en fase-) monitoring te combineren met aandrijftechnieken voor circuitbediening. De terugkoppelingslussen worden aangestuurd door speciale algoritmes, afhankelijk van de functie die van het optische circuit wordt verwacht. We demonstreren gesloten terugkoppel-

circuits voor de implementatie van vermogensregeling in afstembare koppelingen (maximalisatie en minimalisatie van de vermogensoverdracht) en voor controle van de optische fasevertraging. Tot slot gebruiken we dergelijke terugkoppelingslussen voor het aansturen van individuele componenten in een groter circuit in onze demonstratie van een 4×4-poort universele lineair circuit.

Herconfigureerbare lineaire circuits

Een groot aantal optische bewerkingen, zoals koppelingsstructuren, frequentiefiltering, optische vertragingen, schakelnetwerken en quantumoptische bewerkingen, kunnen worden gerealiseerd met behulp van lineaire optische circuits [1]. Een generiek en herconfigureerbaar optisch lineair circuit is een schakeling van linearir optische elementen dat elke lineaire transformatie tussen de ingangen en uitgangen kan implementeren door het veranderen van zijn interne configuratie. Deze aanpak introduceert een veelzijdige en flexibele optische component die kan worden geconfigureerd om verschillende complexe functies uit te voeren.

We implementeerden een 4×4-poort universeel lineair circuit met behulp van een feed-forward netwerk van *Mach-Zehnder Interferometer* (MZI) afstembare koppelingen, oorspronkelijk voorgesteld in [2, 3]. Onze implementatie was de eerste realisatie van een dergelijk circuit in siliciumfotonica [4], en we waren in staat om meerdere functies, zoals een schakelmatrix en een zelfaanpassende bundelkoppeling, te demonstreren door het apparaat te herprogrammeren in software.

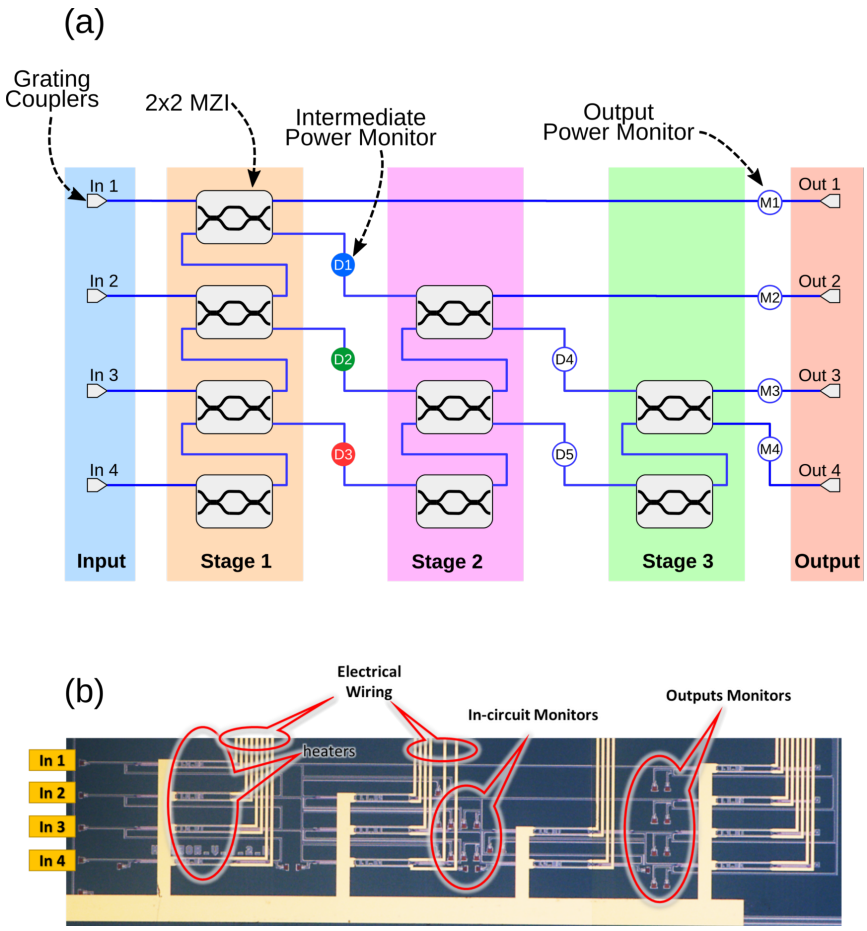
Herconfigureerbare optische netwerken

Een alternatieve architectuur voor het implementeren van programmeerbare fotonische circuits is een configureerbaar optisch netwerk [5, 6]. Deze topologie breidt het concept van de herconfigureerbare lineaire schakeling uit door de mogelijkheid te introduceren om optische terugkoppelingslussen in het circuit te implementeren. Door de optische afstembare koppelingen in een net-topologie te plaatsen kunnen we een verscheidenheid aan optische circuits implementeren door de koppelingsverhoudingen van de koppelingen te programmeren en daarmee de connectiviteit tussen de elementen in de schakeling te veranderen.

In hoofdstuk 6 leggen we onze ontwerpkeuzes uit voor de implementatie van een grootschalig programmeerbaar optisch net. We bespreken de implementaties van faseverschuivers en afstembare koppelingen die specifiek zijn toegesneden op het gebruik in grootschalige, tijd-gedeelde aanstuurschema's en we bespreken ook de strategieën die worden gebruikt om een groot circuit met meer dan 300 actieve elementen aan te sturen en te besturen.

Slotoverwegingen

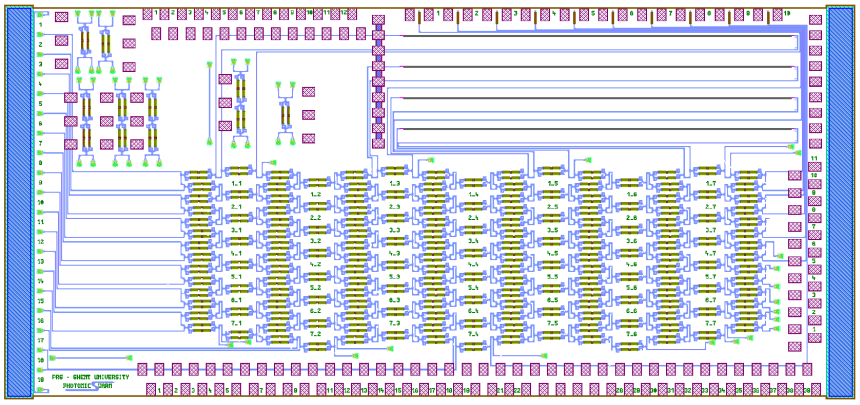
Programmeerbare siliciumfotonica is zich op de kaart aan het plaatsen als een al-



Figuur 2: (a) Schematic of the 4 × 4-port universal linear circuit (b) Microscoopfoto van de 4 × 4-poort universele lineaire schakeling. Dit was de eerste demonstratie van een volledig programmeerbare lineaire operator geïmplementeerd in silicium.

ternatief voor snelle prototype-ontwikkeling van geïntegreerde fotonische circuits. Hierdoor wordt de doorlooptijd voor de implementatie van PIC's verkort en kan gebruik worden gemaakt van de lage-kosten/hoge-volume troeven van het siliciumfotonica platform.

In dit werk onderzoeken we niet alleen verschillende topologieën voor de implementatie van programmeerbare fotonica circuits, maar wijden we ook aanzienlijke inspanningen aan de implementatie van robuuste bouwstenen, aansturingstechnieken en optimalisatiealgoritmes die gebruikt kunnen worden om programmeerbare fotonica circuits op te schalen. Hierdoor kunnen meerdere toepassingen worden geïmplementeerd door het herprogrammeren van de connectiviteit van de PIC's.



Figuur 3: GDSII Layout van een herconfigureerbaar netwerk schakeling ontworpen met 7×7 *hexagonale cellen. Sommige lagen werden weggelaten ter illustratie.*

We verwachten dat de hier gepresenteerde bouwstenen en technieken gebruikt kunnen worden om de schaal van de huidige state-of-the-art siliciumfotonica circuits te vergroten en programmeerbare PIC's te implementeren met een groter aantal programmeerbare elementen, wat leidt tot een groter aantal complexe toepassingen die worden geïmplementeerd met behulp van programmeerbare siliciumfotonica.

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English summary

Photonics plays an important role in today's world, with applications in multiple areas such as sensing, imaging, microscopy, and high speed communication systems, where a great part of the connections uses light as an information carrier.

In this work we discuss the possibilities of extending the implementation of *Photonic Integrated Circuits* (PICs) to enable software-defined functions in optical chips. With that we expect to implement a function-agnostic optical circuit that can be configured after fabrication via software to implement arbitrary functions defined by the user.

Silicon photonics

Silicon photonics is the technology that brings the implementation of photonics integrated circuits to the surface of a silicon chip. Due to the high index contrast between the materials used to implement the waveguide's core and cladding (Silicon and Silicon Oxide, respectively), silicon photonics enables the miniaturization of optical devices, which leads to the integration of a large number of optical functions on a chip using the fabrication technologies developed for the *complementary metal–oxide–semiconductor* (CMOS) industry.

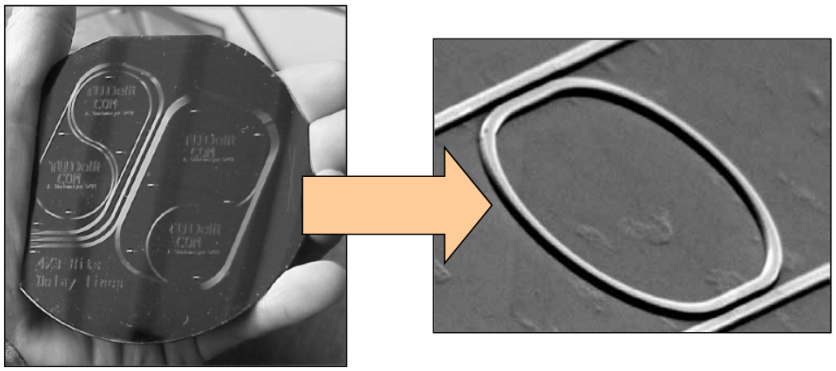

Figure 4: Silicon photonics allows the miniaturization of optical circuits due to the high index contrast between waveguide core and cladding materials (Silicon and Silicon Oxide, respectively).

As silicon photonics is compatible with the manufacturing tools and processes used in the CMOS industry, the platform inherits advantages from the technology such as high volume fabrication capability and tight integration with electronics. This integration with electronics, combined with the high thermo-optical coefficient of silicon, allows the implementation of optical phase shifters using simple localised heaters that can be used not only to stabilize the circuit, but also to implement active components such as tunable power couplers. This characteristics of the platform opens possibilities for implementation of large-scale configurable photonics devices that can extend the capability of PICs.

Programmable PICs

The current state-of-the-art silicon PICs are usually very specialized devices, carefully designed to implement one single function. This type of device can be called an *application-specific photonics integrated circuit* (ASPIC) and this description applies to virtually all the photonic devices in the market at the moment. Because each device is engineered to accomplish one specific function, they can achieve very high performance (such as low insertion loss, optimum power consumption, etc.), but at a cost: flexibility. To implement a solution with an ASPIC, one has to engineer the optical device down to its geometry, simulate each part of the device (in most cases using expensive physical simulations) before prototyping it, which can take months for fabrication.

This same problem was faced by the electronics industry in the past, and it was address by the introduction of programmable devices, such as *microprocessors* and *field-programmable gate arrays* (FPGA), i.e. integrated circuits that are designed to be configured by a customer or a designer after manufacturing. This is done through programming, and drastically improves the flexibility of the device.

The concept of programmable photonics extends the current PIC technology to enable the implementation of fully programmable silicon photonics devices, whose functions are defined via programming after device fabrication and can be used to realize a wide range of applications.

Building blocks and subcircuits for programmable photonics

To implement such programmable photonics circuits we dedicated a large part of this work on the development and optimization of the building blocks and components used in the circuits, as well as on the refinement of the necessary techniques for driving and controlling photonics circuits, including optimization algorithms and feedback loops.

We start our discussion with the implementation of optical phase shifters and tunable couplers. We demonstrate several different implementations of thermo-optic phase shifters and discuss how to tailor their characteristics such as power efficiency and speed by modifying the geometry of the heaters used in its imple-

mentation. We extend our work discussing how to integrate a diode in series with the heater, which creates an asymmetry in the IV-response of the device that can be exploited to implement time-multiplexed access to the heaters.

We discuss the implementation of MZI based 2×2 waveguide couplers and how the use of imperfect components, such as directional couplers with a coupling ratio different than $50/50$, can lead to tunable couplers with non-ideal performance. To circumvent this issue we propose and demonstrate what we call a '$2 \times 2 \times 2$ tunable coupler' that guarantee the implementation of tunable couplers that covers the whole range of 0% to 100% coupling ratio, offering low insertion loss and high extinction ratio even when fabricated with directional couplers with coupling ratio as imbalanced as $25/75$.

With the increase in size and number of tunable elements in photonics circuits we have an equal increase in number of electrical connections and power sources needed for operating the circuit. To solve this scalability problem we developed techniques to drive and control multiple optical components with fewer electrical sources. We addressed this problem by introducing digital driving technique based on *Pulse Width Modulation* (PWM) for driving the phase shifters. That, combined with the use of heaters with integrated diodes, allows the implementation of time-multiplexed access to the tunable devices in the circuit. This reduces drastically the number of electrical contacts and power source needed to actuate the circuit.

To improve the operation of tunable photonics components we discuss and demonstrate the implementation of closed feedback loops to realize tight control of photonics circuits. This is done by combining the use of optical taps for power (and phase) monitoring with driving techniques for circuit actuation. The feedback loops are controlled by dedicated algorithms, depending on the function that is expected from the optical circuit. We demonstrate closed feedback loops for implementing power control in tunable couplers (maximization and minimization of power transmission) and for phase control. Finally we use such feedback loops for controlling individual components in a larger circuit in a 4×4-port universal linear circuit demonstration.

Reconfigurable linear circuits

A great number of optical operations, such as coupling structures, frequency filtering, optical delays, switch networks, and quantum optics operations, can be implemented using linear optical devices [1]. A generic and reconfigurable optical linear device is a device that would implement any linear operation between its inputs and outputs by changing its internal configurations. This approach introduces a versatile and flexible optical component that can be configured to perform different complex applications.

Initially proposed in [2, 3], we implemented a 4×4-port universal linear circuit using a feed-forward network of *Mach-Zehnder Interferometer* (MZI) tunable couplers. This was the first implementation of such device in silicon photonics [4], and we were able to demonstrate the implementation of multiple functions, such

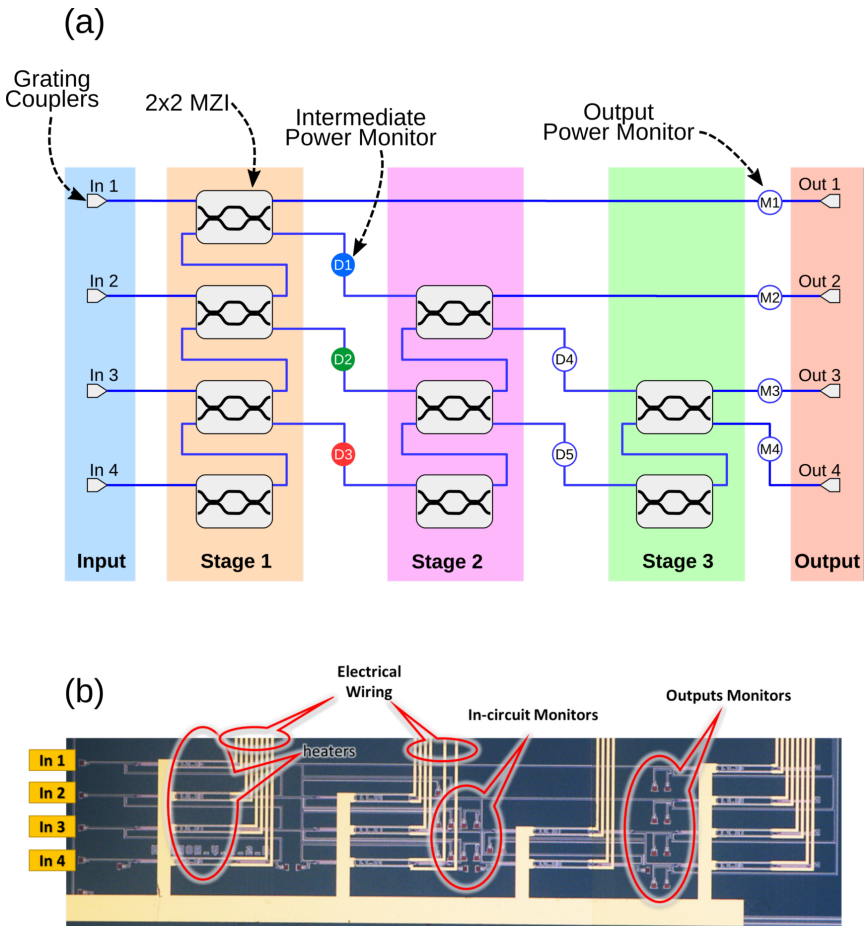

Figure 5: (a) Schematic of the 4×4*-port universal linear circuit (b) Microscope picture of the* 4×4*-port universal linear circuit. This was the first demonstration of a fully programmable linear operator implemented in silicon.*

as a switching matrix and a self-adapting beam coupler, using the same circuit, by reprogramming the device.

Reconfigurable optical meshes

An alternative approach for implementing programmable photonics circuits are configurable optical meshes [5, 6]. This topology extends the concept of the reconfigurable linear circuit by introducing the possibility of implementing optical feedback loops in the circuit. By arranging the optical tunable couplers in a mesh topology we can implement a variety of optical circuits by programming the cou-

pling ratios of the couplers and, with that, rearranging the connectivity between the elements in the circuit.

In Chapter 6 we explain our design choices for implementing a large-scale programmable optical mesh. We discuss the implementations of phase shifters and tunable couplers that are specifically tailored for being used in large scale time-multiplexed driving schemes and we also discuss the strategies used to drive and control a large circuit containing more than 300 active elements.

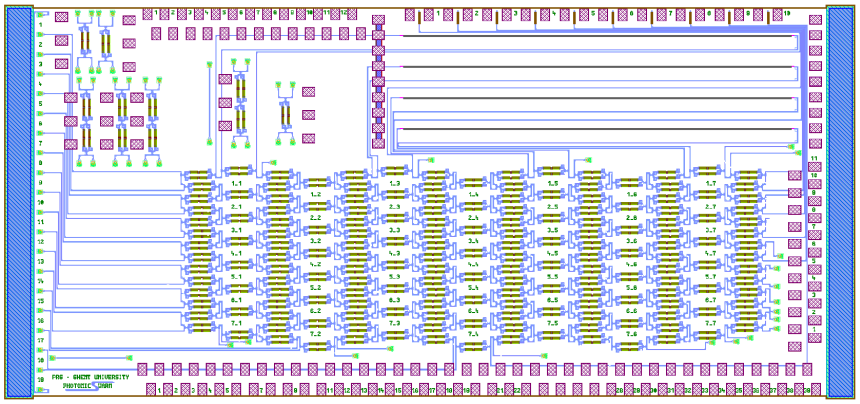

Figure 6: GDSII Layout of a reconfigurable mesh circuit designed with 7×7 *hexagonal cells. Some layers were omitted for illustration purpose.*

Final considerations

Programmable silicon photonics is emerging as an alternative for rapid prototyping and deployment of integrated photonics circuits, reducing the turn-around time for PICs implementation and allowing the exploitation of the low-cost-at-high-volume characteristic of the silicon photonics platform.

In this work we explore different topologies for implementation of programmable photonics circuits, but also dedicate substantial effort on the implementation of robust building blocks, driving and control techniques, and optimization algorithms that can be used to scale up programmable photonics circuits, enabling the implementation of multiple applications by reprogramming the connectivity of the PICs.

We expect that the building blocks and techniques here presented can be used to increase the scale of today's state-of-the-art silicon photonics circuits and implement programmable PICs with a larger number of programmable elements, leading to larger number of complex applications being implemented using programmable silicon photonics.

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1 Introduction

Photonics is the branch of science that deals with information processing by the means of manipulation of light. Photonics technology plays an important role in today's world of high speed communication systems where a great part of the information uses light as a carrier. Optical communication is largely used today in all sorts of application, from metropolitan scale and fiber to the home, all the way to submarine optical cables that are responsible to connect continents. One reason that optical communication is so attractive is that it is cheaper and faster than its electronics counterpart [1–3]. Also, optical fibers are especially advantageous for long-distance communications, because light propagates through the fiber with much lower attenuation compared to electrical cables, which allows long distance communication with few repeaters. Photonics also has great advantages regarding power consumption when compared to electronics [4–6], which makes it a perfect candidate to interconnect nodes in large datacenters [7–9].

1.1 Integrated Silicon Photonics

Integrated photonics is the technology that integrates a large number of optical functions on a chip to create a *photonic integrated circuit* (PIC). A PIC usually contains multiple components arranged in a circuit that can be used to implement a broad range of functions, such as wavelength filtering, multiplexing, modulation, etc. Today there coexist a wide diversity of technology platforms to build PICs, using different material systems such as III-V semiconductors, Lithium Niobate,

high-index glasses and nitrides, polymers, and of course silicon [10].

Silicon photonics inherits a great number of advantages from the electronics industry by using the mature *complementary metal–oxide–semiconductor* (CMOS) technology for the PIC fabrication. CMOS is particularly friendly for integrated photonics implementation as its main material, silicon, is transparent for infrared wavelength, used in telecommunication [11]. The CMOS process technology also creates opportunities for tight integration with electronics and allows low-cost-at-high-volume fabrication of integrated optical devices due to the nature of the technology [12].

One downside of silicon as a platform for integrated photonics is that it is not possible to implement lasers directly on silicon due to its indirect band gap nature of the material [4]. That means that we have to either rely on external laser sources for silicon photonics chips or integrate laser-friendly materials on silicon wafers for laser implementation [13]. It is also possible to integrate lasers on silicon photonics chips via transfer printing [14], which segregates the silicon photonics processing from the laser fabrication, simplifying the PIC fabrication process.

1.1.1 Waveguide and light confinement

The most fundamental building block in a PIC is the waveguide, used to guide the light on the optical chip. A waveguide in integrated silicon photonics consists of a silicon core surrounded by another (dielectric) material with a lower refractive index, usually air or silicon oxide (SiO_2). This arrangement confines the light in the waveguide via total internal reflection and, typically, an integrated waveguide operates as a single mode waveguide.

The high refractive index of the silicon ($n = 3.478$ at $\lambda = 1550\ nm$ wavelength) compared to the index of the surrounding material (as air, $n \approx 1$, or SiO_2, $n = 1.444$) results in a high contrast between waveguide and cladding and, therefore, a high confinement of the guiding mode in the waveguide. This allows for sub-micrometer waveguide dimensions and tight bends, enabling the miniaturization of the photonics components [12, 15] and the integration of a large number of components in a reduced space, making the platform ideal for large scale systems [16, 17].

Silicon photonics technology evolved to a point where we can fabricate waveguides with very low propagation loss, in order of a $0.2dB/cm$ to $1.0\ dB/cm$ [18]. The loss in the waveguide comes mostly from the roughness at the sidewall of the waveguide due to fabrication imperfection as silicon has low power absorption [19] for the wavelength used in silicon photonics applications [12].

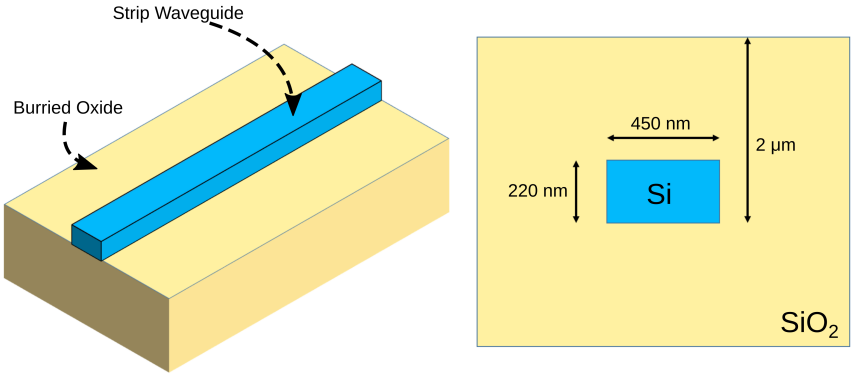

Figure 1.1: (a) Air cladding SOI waveguide. (b) Typical geometry and dimensions for a single mode silicon-on-insulator strip waveguide with silicon oxide cladding.

1.1.2 Electro-optic integration

Due to the miniaturization of its components, silicon photonics allows the integration of many optical functions on a chip. However, photonics elements alone are not enough to implement mostly of real world applications. Electronics is needed to add control to photonics components (e.g., by electrically tuning the performance of the photonic circuit), to act as a monitor (e.g., to read photodetectors), or to implement high speed modulation and detection, as an example. Photonics and electronics need to be combined into the single circuit to use the full potential of the silicon photonics platform.

The integration between photonics and electronics can be monolithic (fabrication of the electronics and the photonics in the same chip, either in the *front-end of the line* (FEOL) or in the *back-end of the line* (BEOL)) or using a hybrid integration, where the electronics and the photonics chips are fabricated separately and later integrated via *flip-chip* or *wirebonding* techniques.

1.2 imec's silicon photonics platforms

For this work we relied on the *multi-project wafer* (MPW) runs provided by imec for the fabrication of the photonics chips. imec provides two platforms for silicon photonics in the MPW services for silicon photonics: a passive *silicon-on-insulator* (SOI) platform (Fig. 1.3(a)) which consist basically on a silicon layer on a 2 μm buried oxide substrate for waveguide fabrication, and the iSiPP50G

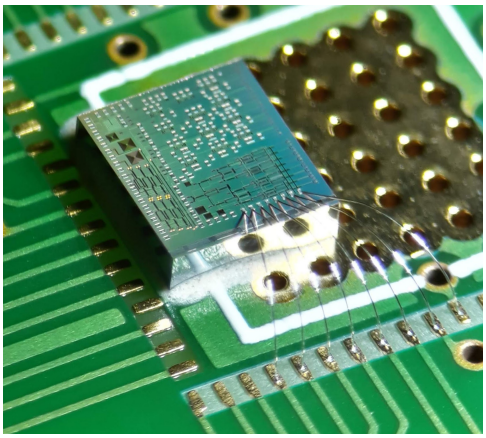

Figure 1.2: A silicon photonics chip with integrated electronics elements such as diodes and germanium photodetectors.

platform (Fig. 1.3(b)), which contains the same elements from the passive platform, but with the addition of doping layers for implementation of modulators and heaters, metal for electrical routing and contact pads, germanium photodiodes for detector, among others. Both platforms provide multiple etching levels (for implementation of rib waveguides, grating couplers, etc.) and an SiO_2 cladding.

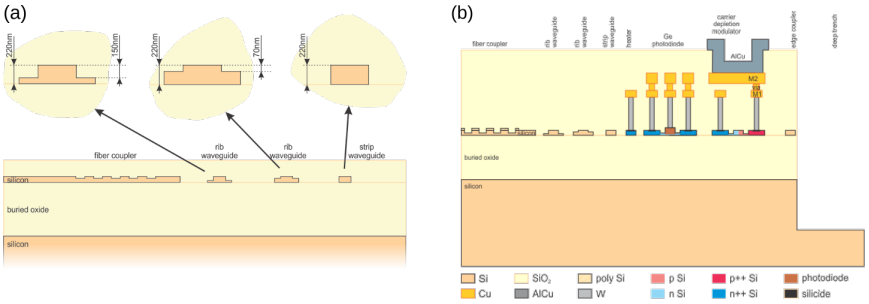

Figure 1.3: (a) Passive silicon-on-insulator platform. (b) iSiPP50G platform consisting of silicon layer for photonics devices plus doping, metals for electrical circuits, photodetectors, etc. Reproduction from [20]

Although not containing the layers needed to implement phase shifters and modulators, circuits implemented using the passive platform can be post-processed to add active elements such as heaters for phase-shifting (as discussed in 2.2.1). This approach brings multiple benefits when the targeted application don't make use of any extra elements of the iSiPP50G platform (e.g. photodiodes or fast modulators) because it enables a) the use of a technology that is cheaper than its more

complete counterpart and b) the passive MPW fabrications have a shorter turn-around time, speeding up the development and learning process.

1.3 Programmable circuits

The current state-of-the-art PICs are usually very specialized devices, carefully designed to implement one single function. This type of device can be called an application-specific photonic integrated circuits (ASPIC) and this description applies to virtually all the photonic devices in the market at the moment. Because each device is engineered to accomplish one specific function, they can achieve very high performance (such as low insertion loss, optimum power consumption, etc.), but at a cost: flexibility. To implement a solution with an ASPIC, one has to engineer the optical device down to its geometry, simulate each part of the device (in most cases using expensive physical simulations) before prototyping it. A whole cycle of design, simulation and fabrication can take up to one year, even for simpler circuits. Optimizing a device asks for multiple cycles of design and prototyping.

The same problem is found in electronics, and this was addressed by the introduction of programmable devices, such as microprocessors and field-programmable gate arrays (FPGA), i.e. integrated circuits that are designed to be configured by a customer or a designer after manufacturing. This is done through programming, and drastically improves the flexibility of the device.

A programmable photonic circuit is an optical device that works in the same fashions as an FPGA. It is a function-agnostic PIC that is programmed after manufacturing to define the function that it will be implementing. Such devices can be categorized as *field-programmable photonic integrated circuit* (FPPIC) and can enable rapid prototyping of new functions and even substitute ASPIC solutions when the application does not impose extreme performance requirements.

1.3.1 Concepts

An FPPIC is programmed by modifying the connectivity of the waveguides and active components in the circuit. The core of an FPPIC is a linear optical circuit. A great number of optical operations, such as coupling structures, frequency filtering, optical delays, switch networks, and quantum optics operations can be implemented using linear operations [21, 22]. In the past years multiple concepts of programmable photonic circuits based on linear operators have been proposed. This approach has been demonstrated in multiple platforms [21, 23] and for different applications, such as quantum optics [21] and machine learning [22].

Optical linear processors can be implemented as a feed-forward network, as illustrated in Fig. 1.5(a). A feed-forward programmable optical linear circuit can

be represented by a *T-matrix* generic circuit (Fig. 1.4) whose parameters can be modified via programming.

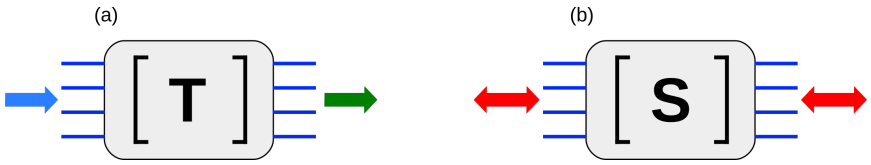

Figure 1.4: (a) Feed-forward networks can be described by a T-matrix representation, as the optical signal propagates in a single direction, without the possibility of implementing feedback loops. (b) Optical meshes that can implement feedback loops can be described using a S-matrix representation.

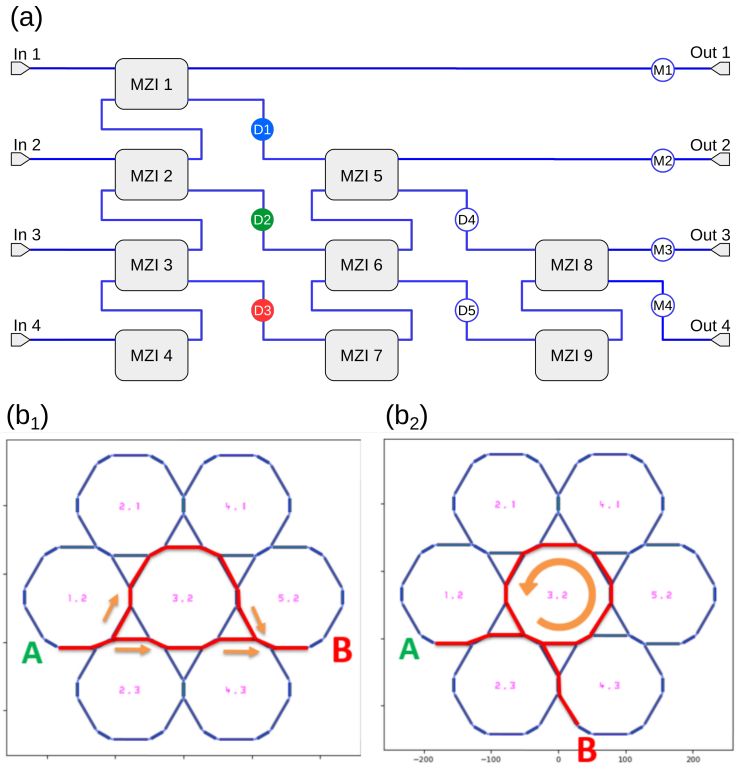

Figure 1.5: (a) Feed-forward optical network. (b1) Optical mesh operating as a Mach-Zender Interferometer filter. (b2) Optical mesh operating ass a ring resonator.

Although flexible, these linear optical processors have their drawbacks, in particular the limitation due the fact that light always propagates forward in the circuit, which prevents the implementation of optical feedback and delay lines. An

alternative to this topology are optical meshes [24–26], illustrated in Fig. 1.5(b), where tunable couplers are arranged in a mesh topology. In this topology the light can be guided in any desired path, including splitting, creating feedback loops, delay lines, etc. This sort of reconfigurable optical circuits can be represented as a generic *S-matrix* circuit, as illustrated in Fig 1.4(b). This gives a larger number of choices to create different optical circuits by rearranging the combinations of the elements of the circuit. In this work we explore both classes of programmable PICs as well as the integration between programmable circuits and other integrated components such as high speed modulators and photodetectors.

1.4 Contributions of this work

Our first contribution to programmable photonics was the implementation of the 4×4-port universal linear circuit [23], which is, to our knowledge, the world's first implementation of such circuit in Silicon Photonics. After this demonstration it was clear for us that we needed better building blocks to scale up the size and the complexity of programmable circuits. Because of that, we dedicated a substantial amount of time developing the necessary building blocks and subcircuits needed to do so.

One main challenge that we had to outcome was the actuation and control of a large number of tunable elements in a photonics circuit. Operating a large-scale programmable circuit requires a large amount of voltage sources and, as a result, a large amount of contact pads, which increases the footprint of the circuit. To solve this problem we developed techniques to multiplex the access to the phase shifters in the circuit using Pulse Width Modulation and matrix addressing using diode-loaded heaters [27].

In parallel to the components and circuit developments, a significant amount of effort was dedicated to the development of control algorithms used to operate the programmable circuits, including algorithms that incorporate closed-feedback loops to control tunable couplers and phase shifters.

1.5 Overview of the thesis

The goal of this work is to introduce and discuss basic concepts and techniques developed during this Ph.D. to design and operate programmable integrated photonics circuits. This document is written following a bottom-up approach, where we first define the basic elements needed to design the programmable circuits, followed by the techniques needed to operate such elements and, at last, we use these building blocks to implement and demonstrate our programmable PIC.

We start our discussion in Chapter 2, where we introduce methods for light

manipulating in a waveguide and introduce a major component used in this work: the phase shifter. Chapter 3 deals with splitting and combining of light, with a special focus on tunable power couplers. Chapter 4 explains our developments regarding driving and multiplexing techniques, necessary to deal with large scale PICs. Following, in Chapter 5, we discuss light detection and control loops. In this chapter we take our time to introduce some techniques used to monitor power levels and relative phase in photonics circuits, followed by a discussion on control loops used to operate the photonics components. Chapter 6 is dedicated to the demonstration of programmable photonics circuits using the building blocks and techniques discussed in the previous chapters. Finally, in chapter 7 we draw our final conclusions and discuss the panorama for future work.

1.6 Publications

1.6.1 International Journals

1. Antonio Ribeiro, and Wim Bogaerts. *Digitally controlled multiplexed silicon photonics phase shifter using heaters with integrated diodes*. Optics Express, 25(24):29778–29787, 2017.

2. Antonio Ribeiro, Alfonso Ruocco, Laurent Van Acker, and Wim Bogaerts. *Demonstration of a 4x4-port universal linear circuit*. Optica, 3(12):1348–1357, 2016.

1.6.2 International conferences

1. Antonio Ribeiro, Umar Khan, and Wim Bogaerts. *Matrix Addressing Silicon Photonics Phase Shifters using Heaters with Integrated Diodes*. In European Conference on Integrated Optics (ECIO), Valencia, Spain 2018.

2. A. Ribeiro, and W. Bogaerts *Thermo-optical Phase Shifter with Integrated Diodes for Multiplexed Control* The Optical Fiber Communication Conference (OFC), United States, p.Th32.A.4 (2018)

3. Y. Xing, U. Khan, A. Ribeiro, and W. Bogaerts *Behavior Model for Directional Coupler* 2017 IEEE Photonics Scociety Benelux Annual Symposium, Netherlands, p.128-131 (2017)

4. A. Rahim, B. Haq, M. Muneeb, A. Ribeiro, R. Baets, and W. Bogaerts *16x25 GHz Optical OFDM Demultiplexer in a 220nm Silicon Photonics Platform using a Parallel-Serial Filter Approach* 43rd European Conference on Optical Communication (ECOC 2017), Sweden, p.1-3 (2017)

5. A. Ribeiro, K. Miura, T. Spuesens, and W. Bogaerts *Phase shift control with active feedback* Proceedings Symposium IEEE Photonics Society Benelux, Belgium, p.291-294 (2016)

6. A. Ribeiro, A. Ruocco, L. Van Acker, and W. Bogaerts *Demonstration of a4x4-port self-configuring universal linear optical component* Progress In Electromagnetics Research Symposium (invited), China, p.3372-3375 (2016)

7. A. Ribeiro, K. Miura, T. Spuesens, and W. Bogaerts *On-chip Differential Phase Monitoring with Balanced Photodiodes* Group IV Photonics, China, p.80-81 (2016)

8. A. Ribeiro, S. Dwivedi, and W. Bogaerts *A Thermally Tunable but Athermal Silicon MZI Filter* 18th European Conference in Integrated Optics 2016 (ECIO), Poland, p.paper ECIO/0-25 (2016)

9. A. Ribeiro, A. Ruocco, L. Van Acker, and W. Bogaerts Demonstration of a 4x4-port Universal Coupler 12th International Conference on Group IV Photonics, Canada, p.PD5 (2015)

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2
Phase Shifters

Optical signal manipulation is an essential building block required to the implementation of integrated photonics circuits. We can use optical manipulation to implement functions such as high speed modulation [1], or to perform controlled power distribution using tunable couplers [2], for instance.

In programmable photonics we make use of a large number of tunable power couplers (further discussed in Chapter 3) which uses a combination of phase shifter and interferometry [2–4] to manipulate both the phase and amplitude of an optical signal.

In this chapter we will discuss how to perform phase shifting in an integrated silicon photonics chip and, in particular, focus on the implementations of thermo-optical phase shifters that are used along this work.

2.1 Waveguides

When light travels in a homogeneous medium, the refractive index n of the material can be used to quantify the number of phase cycles in the signal per unit of length as the signal propagates. Optical phase modulation is done by manipulating the number of phase changes the signal experiences during propagation.

When light propagates in a waveguide, the guided mode is not fully confined in the waveguide core, as the evanescent tail of the mode sits in the cladding of the waveguide (Fig. 2.1(b)), so we cannot assume that the guided mode will behave as if the light is travelling in a homogeneous silicon medium. Therefore, the effective

refractive index experienced by the light will be, in fact, different than the refractive index of the waveguide core (silicon). The index experienced by a guided mode in the waveguide is called *effective refractive index* (n_{eff}), and it depends on the materials of the waveguide (core and cladding), but also on the geometry of the waveguide and the mode in question. In this work we perform our analysis on single mode *transverse-electric* (TE) waveguides, as it is the most common used waveguide in silicon photonics and, specifically, in large scale circuits.

We can calculate the effective index from a waveguide analytically, but for convenience and reliability we can use simulation tools to extract the properties of the waveguide. Simulation solutions are specially useful when calculating the optical modes for complex geometries, where analytical evaluation might become prohibiting expensive and/or inaccurate. We used a mode solver to identify the effective index of the waveguide. Fig. 2.1(a) shows the cross-section of the $220nm$ thick, $450nm$ wide Si strip single mode waveguide and Fig. 2.1(b) shows the $0th$ TE mode profile for $1550nm$ wavelength. For this mode we obtained an $n_{eff} = 2.35542$ from simulation.

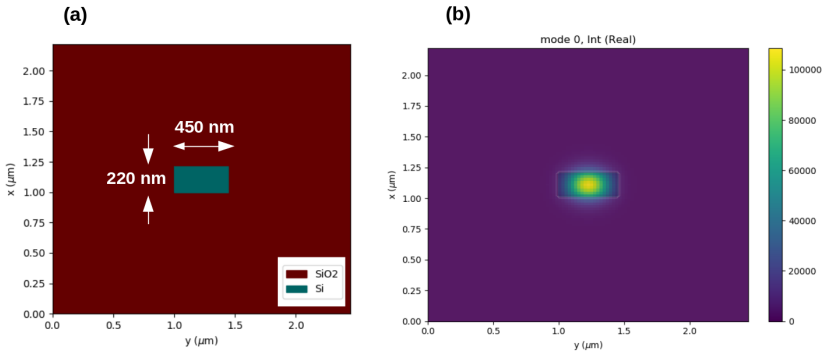

Figure 2.1: (a) Cross-section schematic of a strip silicon waveguide on SiO_2 substrate. (b) 0th order TE mode of the waveguide.

2.1.1 Waveguide bends

It is important to add that that the refractive index of a waveguide is influenced by potential bends in the waveguide [5]. When performing a circular bend, the the phase front of the optical mode rotates around the rotation center of the bend. As the group velocity of the phase front cannot exceed the local speed of light, it affects the refractive index of the waveguide mode in the bent section [6, 7] (Fig. 2.2). This mode mismatch between the straight waveguide and the bend section is a source of reflection in the circuit, and can be problematic in circuits with a large number of bends.

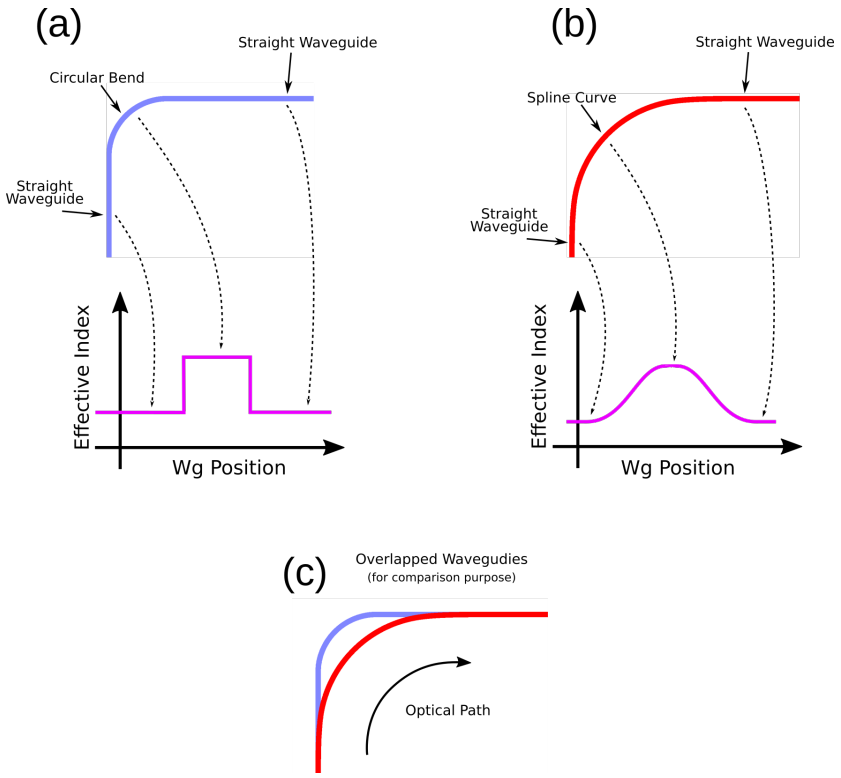

Figure 2.2: (a) Effective index in function of the position of the waveguide for a circular bend. Notice that there is an abrupt change in the effective index of the straight and circular sections of the waveguide. (b) Effective index in function of the position at the waveguide for a bend using a spline curve. The adoption of a spline curve for the bend section avoids abrupt change in the refractive index along the optical path, which reduces potential reflections. (c) Comparison between a circular and a spline-based waveguide bend.

To avoid this abrupt mode transition we adopt an adiabatic transition between the straight section and the bend of in a waveguide, in such way that we have a smooth mode transition along the optical path. We implement this adiabatic transition by using a spline function to trace the waveguide bend, which removes the abrupt effective index change along the optical path.

2.1.2 optical phase and light manipulation

The optical phase notation in a waveguide with length L is given by:

$$\phi = \frac{2\pi L n_{eff}}{\lambda} \tag{2.1}$$

If we want to implement a phase shifter to manipulate the phase ϕ of a monocromatic signal at wavelength λ we can either change the waveguide length L or the effective index n_{eff} of the waveguide. Although changing the length of the waveguide to implement a phase shift has been demonstrated using *microelectromechanical systems* (MEMS) [8–10], this is still not part of standard silicon photonics building blocks and, therefore, not considered in this work. The second option is to manipulate the n_{eff} of the waveguide.

As the n_{eff} depends both on the refractive index of the core and cladding materials used in the waveguide, we can affect the n_{eff} by manipulating either the cladding or the core of the waveguide. Phase shifters have been demonstrated by tuning the refractive index of the cladding of the waveguide using liquid crystals [11] or microfluids [12]. Again, both liquid-crystals and microfluids options make use of building blocks that are not compatible with the standard available SiPh platform, therefore are not considered in this work.

Finally, we can manipulate the n_{eff} of the waveguide by changing the refractive index of its silicon core. Fig. 2.3 shows the variation of Δn_{eff} in function of the change in the refractive index of the silicon core Δn, obtained from simulation. It is possible to change the refractive index of silicon by modulating the density of free carriers in the silicon [13]. Although fast, this approach introduce extra loss in the waveguides as it requires it to be doped (which increases the loss of the waveguide), and electrically contacted to apply the modulating signal. Alternatively, it is possible to use techniques such as the Pockels Effect [14] and the Kerr Effect [15], although they result in a much lower change in the effective index of the silicon.

2.2 Thermo-optical phase shifters

One of the most popular solutions to implement phase shifters in silicon waveguides is to use the thermal sensitivity of silicon to change the refractive index of the core of the waveguide.

Silicon has a very high thermo-optic coefficient ($dn/dT = 1.8 \times 10^{-4} K^{-1}$ [16]) when compared to other optical materials such as glass [17], which makes the silicon core of the waveguide highly sensitive to thermal variations, while the cladding suffers less from the effect.

We can estimate the induced phase change of a light wave propagating in a silicon waveguide for a temperature change of $5K$ and a propagation length of $500\mu m$:

$$\Delta n = 1.8 \times 10^{-4} \cdot 5 = 0.9 \times 10^{-3} \tag{2.2}$$

If we reconstruct the the simulation from Fig. 2.1 and introduce this calculated Δn in the refractive index of the silicon core of the waveguide, we obtain a new

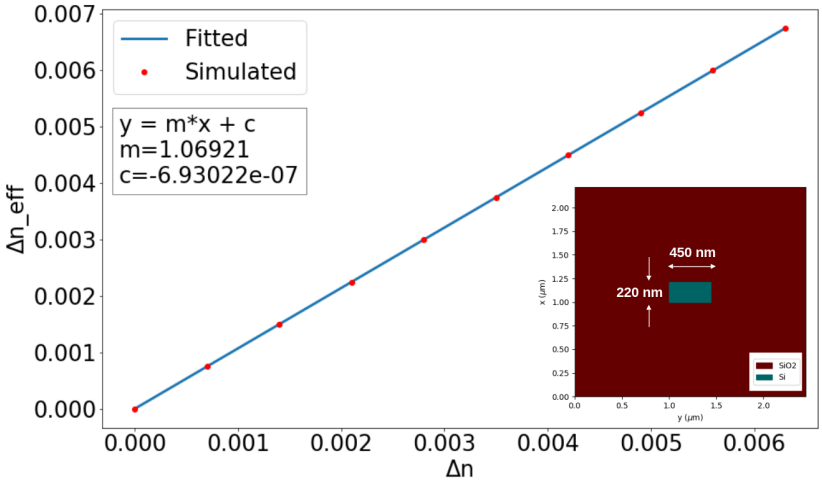

Figure 2.3: Correlation between the change in the refractive index of the silicon (Δn) and the change in the refractive index of a 220 nm thick, 450 nm wide silicon waveguide with SiO_2 cladding.

$n_{eff} = 2.356382$, so $\Delta n_{eff} = 0.9623 \times 10^{-3}$. We can plug this difference back at Eq. 2.1 to get the induced phase change:

$$\Delta\phi = \frac{2\pi \cdot 500 \times 10^{-6} \cdot 0.9623 \times 10^{-3}}{1.55 \times 10^{-6}} = 0.621\pi \; radians \tag{2.3}$$

This shows that even a small change in temperature can lead to a relative large change in the optical phase. While on one hand this characteristics imposes some challenges regarding the thermal tolerances of the device (which can be addressed by engineering the device to be tolerant to overall temperature variations [18]), on the other hand this same effect can be used to implement thermo-optic based phase shifters by locally changing the temperature of the waveguides.

Thermo-optical phase shifters can be implemented by placing a heater close to the waveguide on which we want to induce the phase shift (Fig 2.4). The heater is engineered as a resistor, and controlling the power dissipated by the heater (e.g., by changing the voltage applied to it) controls the change in the effective index of the targeted waveguide, therefore changing the phase of the optical signal.

Heaters are relatively simple to implement and its fabrication can be integrated in the CMOS process [2, 3]. Thermo-optic phase shifters have been successfully used to tune and stabilize a large range of silicon photonics components such as ring resonators [19, 20] and interferometric switches [2, 4]. Nonetheless, it is also possible to include thermo-optical phase shifters in thermal-tolerant devices, once they are designed to compensate global changes in the temperature while the

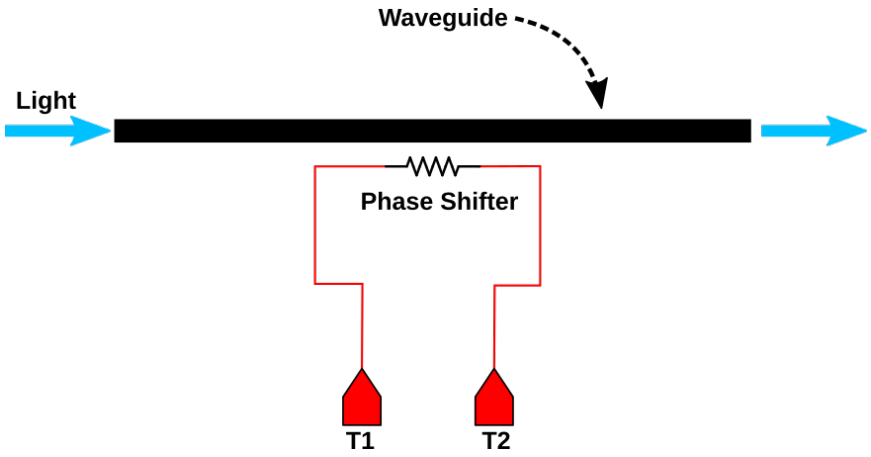

Figure 2.4: A thermo-optical phase shifter can be implemented by placing a resistor-based heater close to the target waveguide. Applying voltage to T_1 and T_2 increases locally the temperature around the heater, which changes the effective index of the waveguide.

thermo-optical phase shifters address a specific area of the photonic device [21].

2.2.1 Titanium line heaters

It is possible to implement phase shifters on passive PICs by adding simple resistive heaters on top of a waveguide with an additional process after the chip fabrication. This postprocessing step is an important feature because it adds electro-optic functionality onto the relatively simpler passive PICs.

The resistor is processed on top of the cladding layer, above the silicon waveguide in the PIC (Fig. 2.5(b)). The resistor consist on two metal layers: first a $100nm$ titanium layer for the resistor, followed by a second layer of $600nm$ gold, which is used for the pads and wires (Fig. 2.5(a)). As the two metal layers (Au and Ti) don't have the same pattern (Fig. 2.5(c)), we have to do two lithography process steps: first for the high-resistivity layer and a second one for the wires and contact pads.

We used *finite element method* (FEM) to simulate the temperature change in the silicon core of the waveguide when driving current through the titanium heater. We built the model on Comsol multiphysics solver for a $200\mu m$ long heater driven with a $5V$ potential difference (Fig. 2.6). We obtained an increase in temperature of $\Delta T = 18.4K$ in the core of the waveguide when driving, and from this we can stipulate a change in the refractive index of the silicon of:

$$\Delta n = 1.8 \times 10^{-4} \cdot 18.4 = 3.312 \times 10^{-3} \tag{2.4}$$

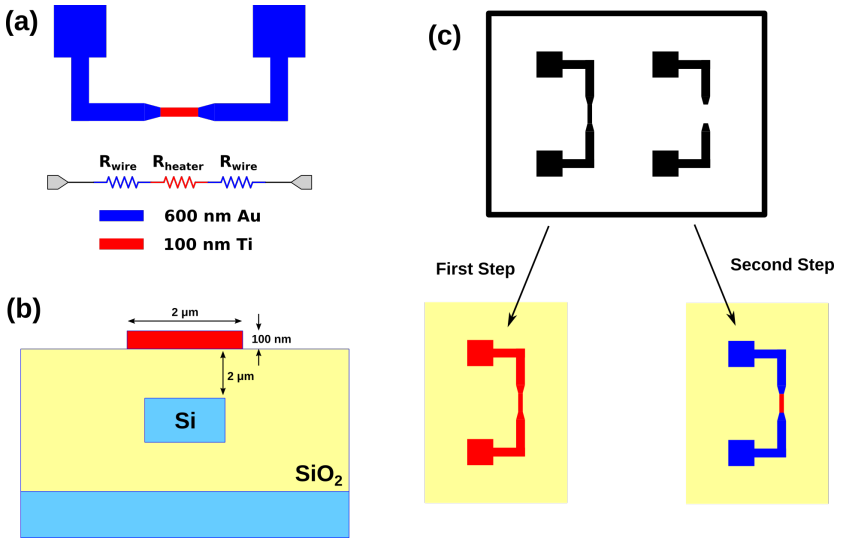

Figure 2.5: (a) Schematic of the titanium heater with gold wires for electrical contact. (b) Cross-section of a waveguide with a titanium heater processed on top of the fabricated device. (c) Illustration of the layers of a contact mask, and how the patters are transferred from the mask to the chip.

We can use this value back in our waveguide model in the mode solver to simulate the new effective index for the heated-up waveguide. From that we obtained a new $n_{eff} = 2.35896$, which gives us a $\Delta n_{eff} = 3.54 \times 10^{-3}$. Plugging this back in Eq. 2.1 let us estimate the phase shift for this $200\mu m$ long phase shifter at $5V$:

$$\Delta\phi = \frac{2\pi \cdot 200 \times 10^{-6} \cdot 3.54 \times 10^{-3}}{1.55 \times 10^{-6}} = 0.914\pi\ rad \tag{2.5}$$

The total power dissipation at $5V$ was $18.5mW$ according to the simulation results, which gives us a phase shifting efficiency of $20.24mW/\pi$. This simulated results shows that we can have a relatively efficient phase shifter using postprocessed top heaters.

For implementing phase shifters on imec's passive silicon photonics platform we processed the fabricated chips using the lift-off process. The passive chip (Fig. 2.7(a)) waveguide is a $220nm$ silicon strip on a buried SiO_2 substrate. On top of the waveguide we have an extra $2\mu m$ SiO_2 top cladding layer. First we spincoat a layer of photoresist on the sample (Fig. 2.7(b)). The contact mask is aligned with the existing alignment patterns on the sample to define the pattern to be transferred onto the PIC(Fig. 2.7(c)). Once the mask is in place, we illuminate the sample with *ultra violet* (UV) light (Fig. 2.7(c)) and, following, we perform a

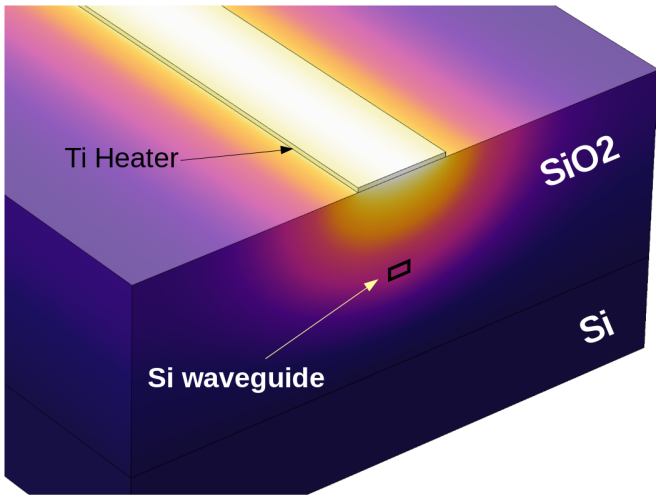

Figure 2.6: FEM simulation of the heat transfer from the titanium resistor to the waveguide core.

baking step on the sample. After baking, the photoresist is developed, and the area exposed to UV light remains on top of the substrate (Fig. 2.7(d)). At this point we transfer the pattern of the contact mask to the silicon chip. We then proceed with the metal deposition (Fig. 2.7(e)). In this step the metal is deposited on top of the whole sample, but it will only adhere to the SiO_2 substrate in the openings of the photoresist. After the metal deposition is done, the sample is washed in acetone to remove the photoresist and what is left is the metal with the pattern defined by the contact mask (Fig. 2.7(e)). This whole process is repeated a second time for the second metal layer.

To characterize the fabricated phase shifter we placed it on a symmetric Mach-Zender interferometer, as illustrated in Fig. 2.8(a). By changing the power yielded by the heater we change the interference pattern of the MZI. A change of $\pi radians$ in the optical phase shifts the transmission from one output to the other. From the plotting of the the transmission of the MZI in function of the electrical power in the heater (Fig. 2.8(b)) we then can extract the phase shift efficiency of the phase shifter of 21 mW/π. This result matches with the expected efficiency from our simulation model. On table 2.1 we summarize the parameters of our standard titanium heater, used in the circuits fabricated using the imec's passive silicon photonics platform.

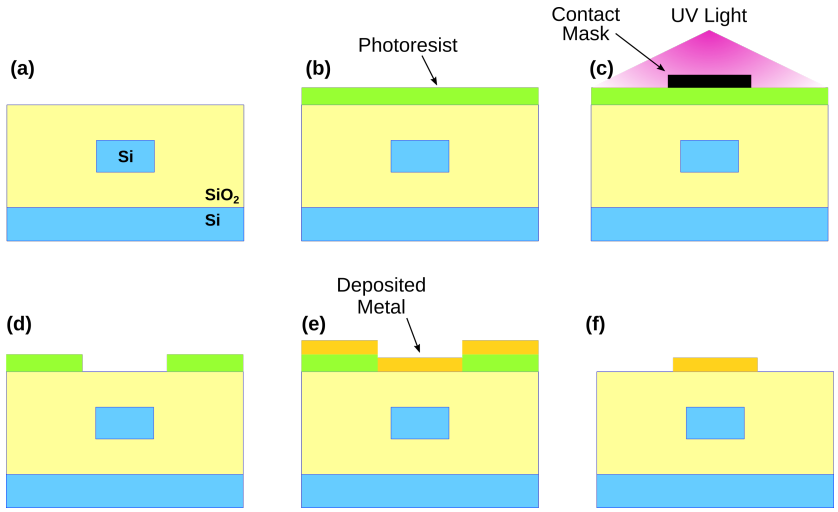

Figure 2.7: Lift-off processing steps (a) Initial passive silicon-on-insulator PIC. (b) Sample with applied photoresist. (c) Contact mask alignment and UV light application. (d) Transferred pattern after photoresist development. (e) Metal deposition. (f) Resulting metal layer after lift-off process.

Length:	200 μm
Width:	2 μm
Ti thickness:	100 nm
Au thickness:	600 nm
Resistance @5V*:	1.3 $k\Omega$
Efficiency*:	21 mW/π

*Table 2.1: Summary of the parameters of the standard titanium heater. *Experimentally obtained.*

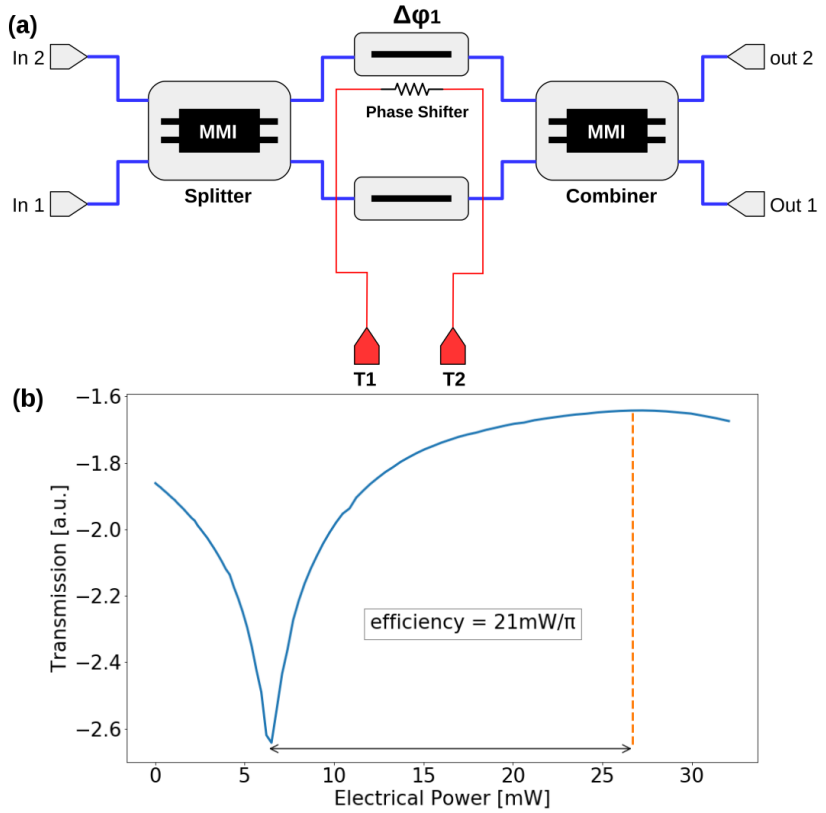

Figure 2.8: (a) A Mach-Zehnder interferometer used to characterize the phase shifter. (b) MZI transmission in function of the electrical power applied to the heater.

2.2.1.1 Heaters as non-linear resistors

As the induced phase shift is proportional to the temperature in the waveguide, we expect to see an induced phase shift that grows quadratically with the voltage applied to the heater. We can express this relationship between voltage and phase shift by the expression:

$$\Delta\phi = A \cdot \frac{V^2}{R} \tag{2.6}$$

where V is the voltage applied to the heater, R is the electric resistance of the heater, and A is a constant that correlates with the efficiency of the heater.

However, the relationship expressed in Eq. 2.6 assumes an ideal scenario where the the resistance of the phase shifter is constant for any voltage V applied to the heater. As we can see in Fig. 2.9(bottom), the measured resistance of the heater

increases with the voltage, due to the increase in the temperature of the resistor [2]. Fig.2.9(top) shows the result of this non-linear behaviour of the resistance of the heater when operating an MZI. Notice that the measured transmission of the MZI in function of the applied voltage deviates from the ideal response, which might impose some challenges regarding phase shift control using thermo-optical phase shifters. We will come back to this issue in the coming chapters, where we discuss the driving and control techniques used to address this problem.

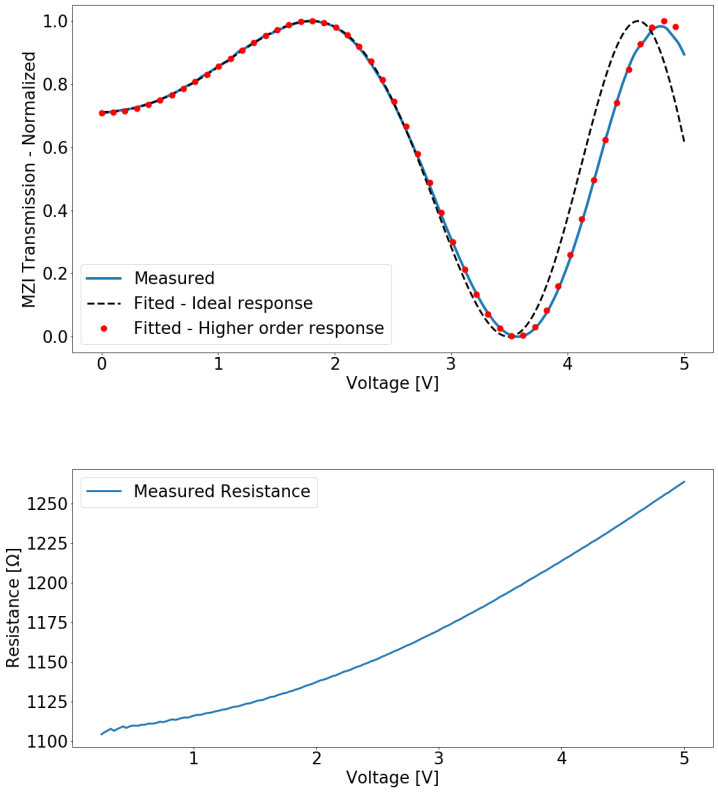

Figure 2.9: (top) Normalized MZI transmission in function of the voltage applied to the phase shifter. (bottom) Value of the resistance of the heater in function of the applied voltage.

2.2.2 Doped silicon heaters

Silicon photonics chips fabricated using the ISIPP50G platform from imec have access to a number of extra features besides the silicon layer used for waveguide

patterning. The platform allows P and N doping and electrical contact to the silicon layer, as well as metal for routing (copper) and contact pads (aluminum). A simplified cross section view of the extra layers available on the full platform run can be seen in Fig. 2.10 (a more complete cross section diagram can be seen in Fig. 1.3(b)). The extra layers can be used to implement high speed modulators [1] and PN junctions for diode implementation [22]. Also, as the doped silicon has a higher conductivity than the intrinsic one, we can use a doped silicon strip to implement a resistor (Fig. 2.10(b)). We can engineer the characteristics of the resistor by changing its geometry (length and width) as well as choosing the doping used in its implementation. We can implement a phase shifter using this resistor (Fig. 2.10(b)) without the need of extra postprocessing steps, maximizing the use of the standard SiPh platform for complex PICs implementation.

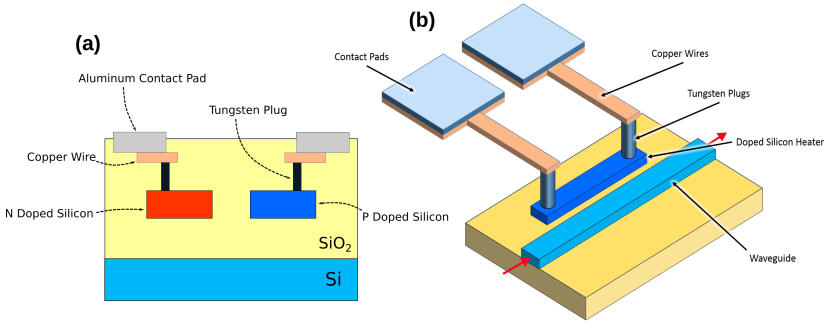

Figure 2.10: (a) Cross-section of the simplified subset of available layers in the SIPP50G platform. (b) 3D illustration of a phase shifter implemented using a doped silicon resistor implemented in the ISIPP50G platform.

Different from the titanium top heater discussed in section 2.2.1, the doped silicon heater is placed in the same layer as the waveguide (Fig. 2.13) rather than on top of it. Because of that we have some freedom regarding the distance between the heater and the waveguide. Initially we want to place the heater as close as possible to the waveguide, to increase its influence and, consecutively, its efficiency. However, placing the heater too close to the waveguide can lead to mode coupling between the waveguide and the resistor. This could lead to an increase of loss in the circuit, once doped silicon is a lossy medium, or even to the creation of cavities, which could compromise its operation.

To avoid mode coupling we simulate the coupling between the waveguide and the resistor for different gaps separating them. Fig. 2.11 shows the simulated power coupling k between two $200\mu m$ long waveguide for different gap distances. We notice that for distances above $550\ nm$ we have negligible coupling between the waveguides, therefore we can judge this as a minimum safe distance between the heater and the waveguide. The simulation was realized using *Finite-difference*

time-domain (FDTD) method using the software Lumerical FDTD. We can further reduce the risk of mode coupling between the waveguide and the heater by designing the heater with a different width from the waveguide. This will prevent phase matching between the the optical mode in the waveguide and in the heater. For our heater we adopted a width $w = 1.4\ \mu m$ as the standard value for all implementations.

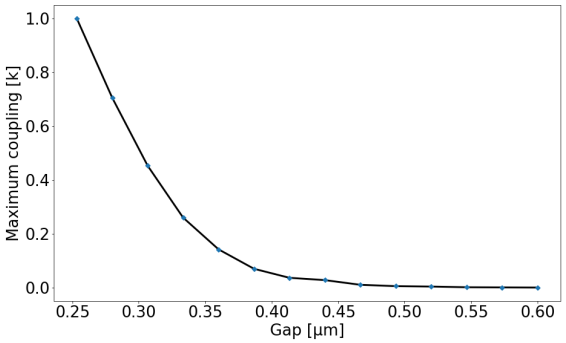

Figure 2.11: Simulated power coupling between two $200\ \mu m$ *long waveguides in function of the gap distance separating them. Notice that for gap* $> 0.55\ \mu m$ *we have negligible coupling between the waveguides.*

Once we obtained the minimum distance gap between waveguide and heater, our next step is to calculate the value of our doped silicon resistor. The resistance R of a resistor of length L and width w is given by:

$$R = \frac{L \cdot R_{sheet}}{w} \tag{2.7}$$

where $R_{sheet}[\Omega/sq]$ is the sheet resistance of the silicon layer. This value is obtained from the fab and depends on the thickness of the silicon layer and the doping concentration. The expected sheet resistance for a $220\ nm$ thick P-doped silicon slab stays in the order of magnitude of 50 to $100\ \Omega/sq$.

After fixing the resistor width at $w = 1.4\ \mu m$ we can calculate the value of the resistor for a given length and sheet resistance value. Fig. 2.12 shows the calculated resistance for multiple values of R_{sheet} and multiple resistor length. The first thing we notice from the calculated values is that, when compared to the titanium resistor, a doped silicon heater of same length will have a much higher resistance. That means that the silicon heater will demand a higher voltage to yield the same electrical power when compared to a titanium heater of same length. This doesn't have any direct impact on the efficiency of the device though. We fixed

our standard resistor length to $L = 50\ \mu m$ to keep the resistance value in the same order of magnitude of the titanium heater.

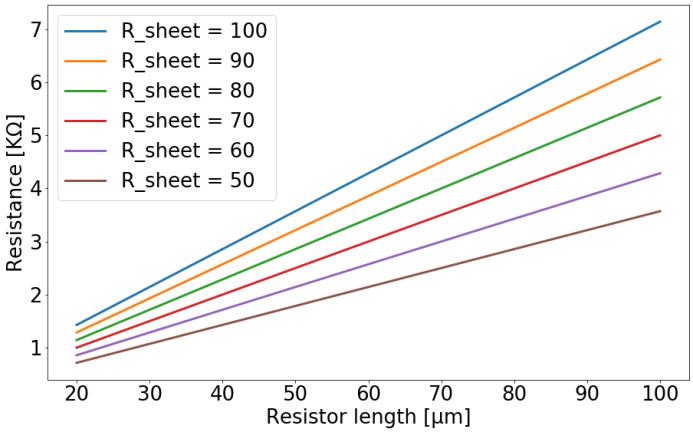

Figure 2.12: Calculated resistance of a doped silicon strip resistor for multiple sheet resistance values.

We can estimate the efficiency of the phase shifter using the same approach used in section 2.2.1. First we simulate the temperature of the waveguide using FEM in COMSOL (Fig. 2.13). For this simulation we defined a 200 μm long [1], 1.4 μm wide resistor and placed it next to the waveguide, respecting a gap of 600 nm. We then set the resistor as a heat source dissipating 18.5 mW (the same value obtained from the titanium heater simulation, for direct comparison). From the simulation we obtained a temperature change in the waveguide core of $\Delta T = 14.6K$. Following, we calculate the change in the refractive index of the silicon for this temperature change:

$$\Delta n = 1.8 \times 10^{-4} \cdot 14.6 = 2.628 \times 10^{-3} \tag{2.8}$$

We then plug the calculated Δn in the mode solver to calculate the new effective index of the waveguide. From the simulation we obtain a new $n_{eff} = 2.35823$, which results in a $\Delta n_{eff} = 2.81 \times 10^{-3}$. Finally we can calculate the induced phase change:

$$\Delta\phi = \frac{2\pi \cdot 200 \times 10^{-6} \cdot 2.81 \times 10^{-3}}{1.55 \times 10^{-6}} = 0.725\pi\ radians \tag{2.9}$$

[1] Although $L = 200\ \mu m$ is not the adopted value for our standard doped silicon resistor length, we opted to simulate it for this length for a more direct comparison with the titanium heater. The choice of length doesn't impact the efficiency of the device tough

which give us an efficiency of $25.5\ mW/\pi$. Although this figures worse than the titanium heater discussed in section 2.2.1, we can further improve this by engineering the geometry of the phase shifter. We will come back at this in section 2.2.3.

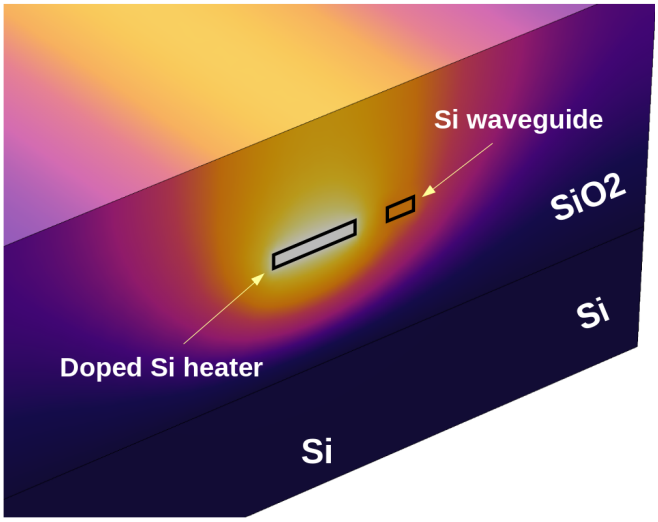

Figure 2.13: Doped silicon heater thermal simulation.

We characterized the phase shifter using the same approach used for the titanium heater, where we place the phase shifter in a MZI (Fig. 2.14(a)). As our choice for the silicon heater is a much shorter element ($L = 50\ \mu m$), we placed four heaters in the same waveguide, so we can have enough heating length (see Eq. 2.1). The four heaters are electrically connected in parallel to increase the power output for a given driving voltage.

Fig 2.14(b) shows the transmission of the MZI in function of the power in the heater. We can see from the plot that we approach the expected $25.5\ mW/\pi$ from the simulations. We can further increase the efficiency of the heaters by engineering the geometry of the phase shifter. Table 2.2 summarizes the parameters of the standard silicon heater used in this work.

2.2.3 Phase shifter geometry

As discussed earlier, a doped silicon heater has a higher resistance when compared to a titanium heater of same length. Because of that the silicon doped phase shifter requires a higher voltage level to yield the same electrical power when compared to the titanium option. To ensure compatibility between the two solutions the doped silicon heaters implemented during this work are constructed using a bank of heaters that are electrically connected in parallel, which, in essence, reduces

Width:	$1.4\ \mu m$
Length:	$50\ \mu m$
Gap:	$600\ nm$
Doping:	P-type
Resistance@5V:	$1.78\ K\Omega$
Efficiency*:	$26\ mW/\pi$

*Table 2.2: Summary of the parameters for the doped silicon heater. *Experimental value obtained for a phase shifter with four heaters, electrically connected in parallel.*

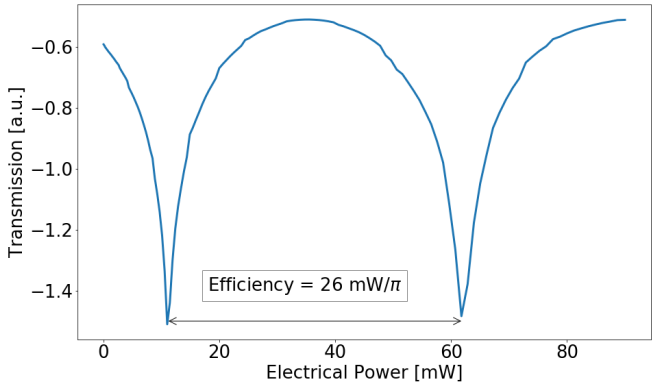

Figure 2.14: Induced phase shift in function of the power in the heater.

the equivalent resistance of the heater. Fig. 2.15 illustrates how we implement a segmented doped silicon heater to reduce the total resistance of the heater. By choosing the number of sections (and, consecutively, the size of each section) we control the value of the resistance of the heater without affecting its total length. With this parametrization we can choose between driving the heater with a high-current/low-voltage power source or vice-versa, depending on the requirements of the application. The same approach can be used with diode-loaded heaters, which is specially useful once we have to design the phase shifter to operate within the voltage boundaries imposed by the breakdown voltage of the diode.

A second characteristics of phase shifters that can be manipulated by engineering its geometry is its power efficiency. In large scale photonics circuit with a large number of tunable components, power efficiency is a concern in the circuit design. We can increase the power efficiency of the phase shifter by improving its thermal energy usage. As we can see from the simulation in Fig. 2.16(a), the heater radiates thermal energy to a broad volume, and only a small part of this heated volume contains the the waveguide itself. That means that a big part of the generated heat

is not being used to induce a phase shift and is being wasted instead. There are multiple ways to increase the efficiency of of a thermo-optical phase shifter, such directly heating the waveguide [4], creating isolation trenches in the cladding layer (Fig.2.17) or even under-etching the silicon substrate below the BOX layer [23]. Although such modifications have been demonstrated to have a large impact in the efficiency of the heaters, trench placement requires either a high customized processing, not always available for most MPW runs, or some level of postprocessing, which should be avoided as it increases the fabrication costs. Directly contacting the waveguide can lead to excessive loss, which have a negative impact in large scale circuits [24].

As an alternative to increase the efficiency of the phase shifter we can modify the routing of the waveguide along the resistor in the phase shifter. Fig. 2.16(b) and Fig. 2.18(bottom row) show a paperclip-shaped phase shifter, where the waveguide is wrapped around the heater to better harvest the dissipated heat. This modification allows the heat radiated by both sides of the heater to be captured by the waveguide, increasing the power efficiency of the device (as we heat a longer waveguide section with the same heater). This approach has the drawback of requiring a longer waveguide when compared with the simple phase shifter, and is a parameter that has to be evaluated when using such geometry choice in designs where the optical length has significant impact (e.g. ring resonators).

Fig. 2.18 shows the three main geometry choices for doped silicon phase shifters that are used in this work. The choice of the device depends on the power efficiency requirements and driving voltage levels boundaries. All geometries can be implemented with diode-loaded heaters as well.

2.2.4 Diode-loaded heaters

Both the titanium strip and the doped silicon resistors are pure resistive elements. Because of that the heaters have a symmetric response to the driving voltage. Inverting the polarity of the driving signal will have no effect whatsoever on the response of the phase shifter (Fig. 2.19). We can break the symmetry of the resistor by introducing a diode in series with it, making it work only in forward biased and acting as an open electrical circuit when reverse biased. The break in the symmetry of the device can be explored to create circuits that share contact pads to drive multiple phase shifters depending on the polarity of the driving signal [22].

We can implement a diode in series with our silicon resistor by creating a *PN* junction directly in the resistor. A typical silicon heater is doped with either *P-type* or *N-type* dopants to increase its conductivity. In our design we doped the main body of the heater using *P-type* dopant, and near one of the electrical contacts we used a *N-type* dopant, creating a *PN* junction inside the heater (Fig. 2.20(a)). This approach converts the standard heater to a resistor with a diode in series.

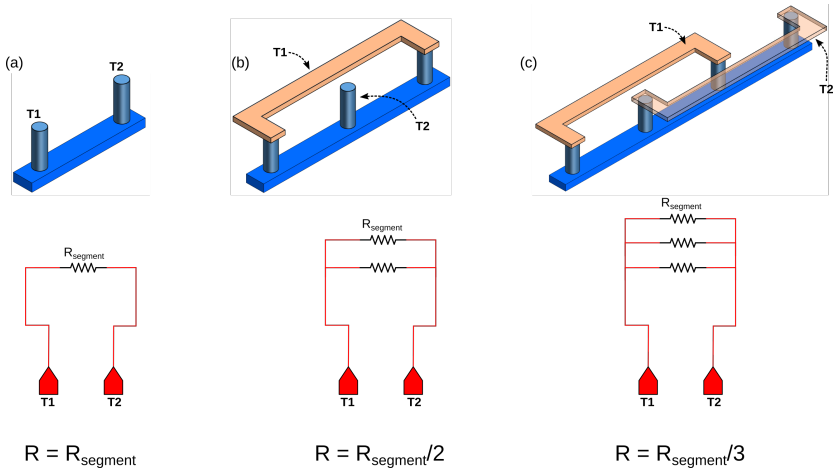

Figure 2.15: (a) Simple doped silicon resistor. (b) Segmented doped silicon resistor. (c) Segmented resistor with three segments in parallel. The equivalent resistance of the heater depends on the number of segments, and it is expressed by $R = R_{segment}/n$, where n is the number of segments.

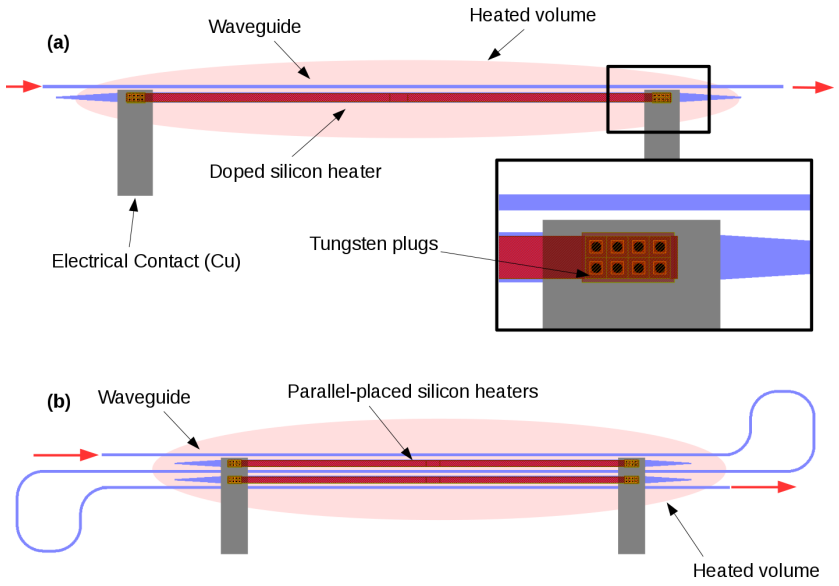

Figure 2.16: (a) GDSII layout of a doped silicon heater. (b) A paperclip-folded phase shifter. In this design the waveguide is folded around the heaters, creating a more compact and power-efficient device.

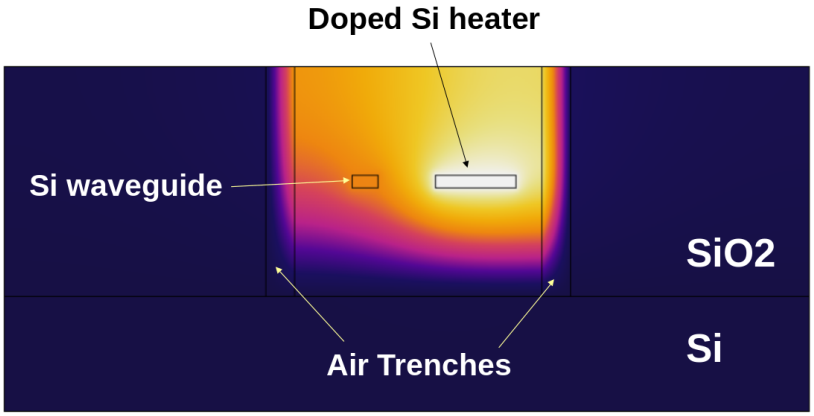

Figure 2.17: Phase shifter with extra air tranches for insulation. The etched area increases the heat confinement, increasing the power efficiency of the device.

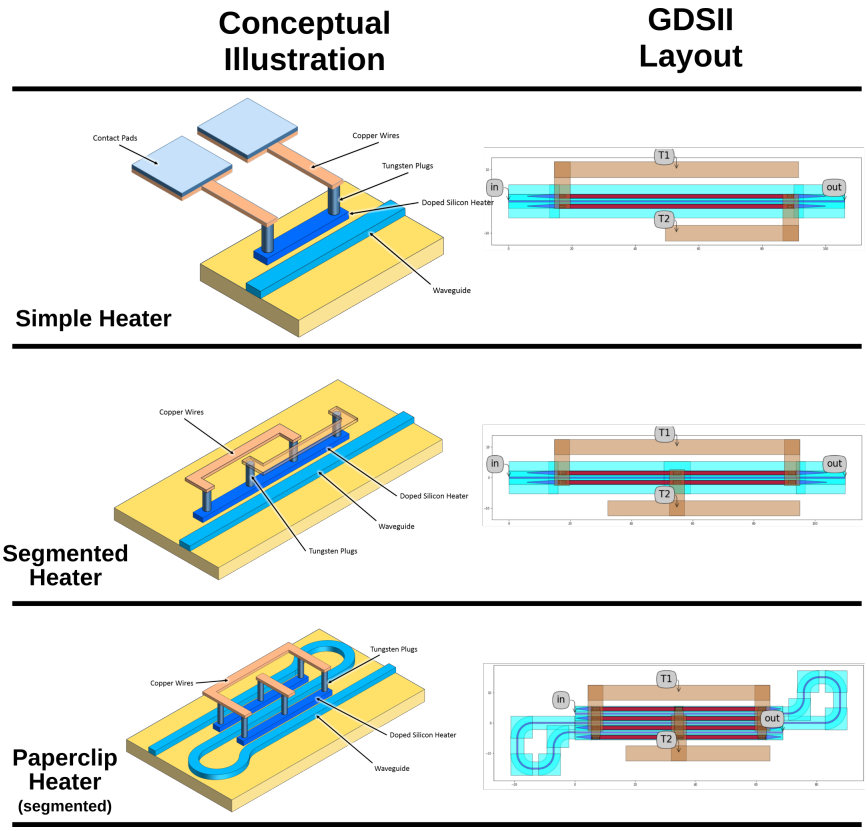

Figure 2.18: Illustration concept of phase shifter geometries and their GDSII layout.

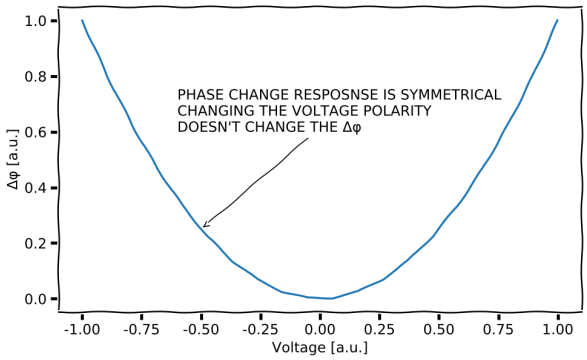

Figure 2.19: Phase response of a phase shifter in function of the driving signal. Notice that changing the polarity of the driving signal doesn't affect the induced phase change.

We implemented the diode heater using a $50\ \mu m$ long, $1.4\ \mu m$ wide silicon heater. The ratio between the lengths L_p and L_n was chosen from the IV-curve of the fabricated device, shown in Fig. 2.21. We selected the diode with dimensions $L_n = 8\ \mu m$ and $L_p = 37\ \mu m$ as the standard component to be used in this work as is slightly more linear IV response than the other diodes.

We characterized the fabricated diodes by extracting its I-V curve. We used a variable voltage source to drive the heater within a voltage range of $-10.0V$ to $+10.0V$, while recording the current through the device. The I-V curve of the fabricated devices (Fig. 2.22) shows a clear diode behavior, with negligible current flow in reverse bias, before the breakdown point. The measured diodes yielded a conduction threshold voltage of $0.75\ V$, while the reverse breakdown voltage was at $-7\ V$. From this values we assume that it is safe to operate the heaters in the $\pm 7\ V$ range. The measured resistance at $5V$ was $5.3\ k\Omega$ and the electrical power delivered at $7V$ was $9.6\ mW$ per heater. To achieve higher power output without compromising the operational range of $\pm\ 7V$ we can drive multiple heaters in parallel. Table 2.3 summarizes the parameters of the diode-loaded heaters used in this work.

2.2.4.1 Application of diode-heaters in photonics circuits

Fig. 2.23 shows an example of application of the diode-loaded heaters to reduce the number of contact pads used in a circuit. Fig. 2.23(a) shows a standard implementation of an asymmetric MZI filter with phase shifter in its both arms. The frequency response of the filter can be tuned by changing the phase of the light in the arms of the MZI. It is possible to induce either a blue-shift or a red-shift on the

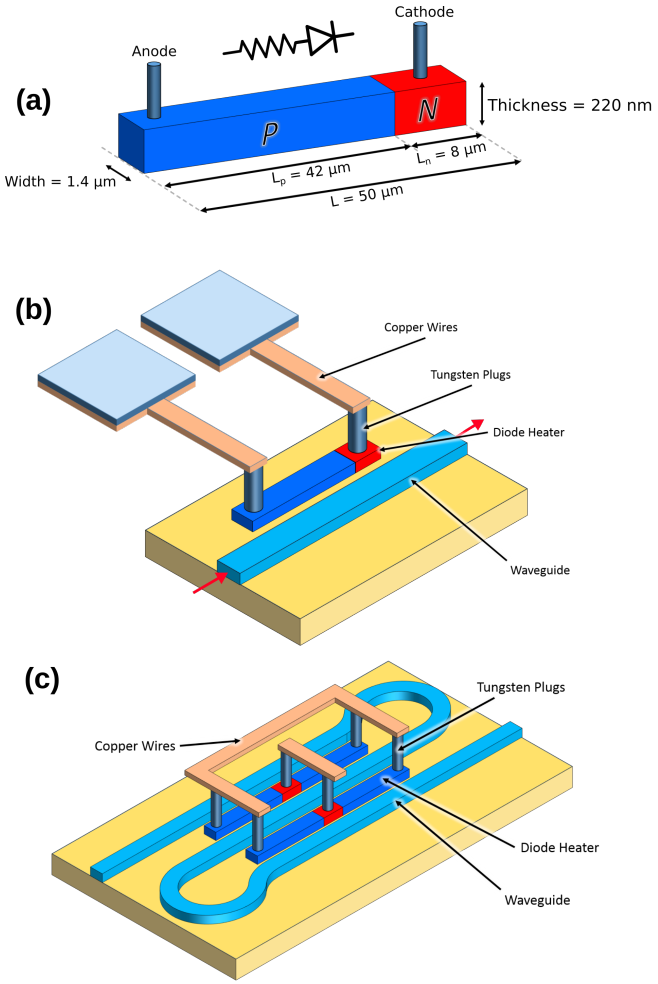

Figure 2.20: (a) Illustration of a diode-loaded heater implemented in the ISIPP50G platform from imec. The dimensions shown in the figure represents the standard diode-heater used in this work. (b) Illustration of a phase shifter implemented using a diode heater. (c) A paperclip-shaped phase shifter with a bank of four diode heaters.

Width:	$1.4\ \mu m$
Total length:	$50\ \mu m$
N length:	$8\ \mu m$
P length:	$42\ \mu m$
$V_{threshold}$:	$0.75\ V$
V_{break}:	$-7\ V$
Resistance@$5\ V$:	$5.3\ K\Omega$

Table 2.3: Summary of the parameters of the diode-loaded heaters.

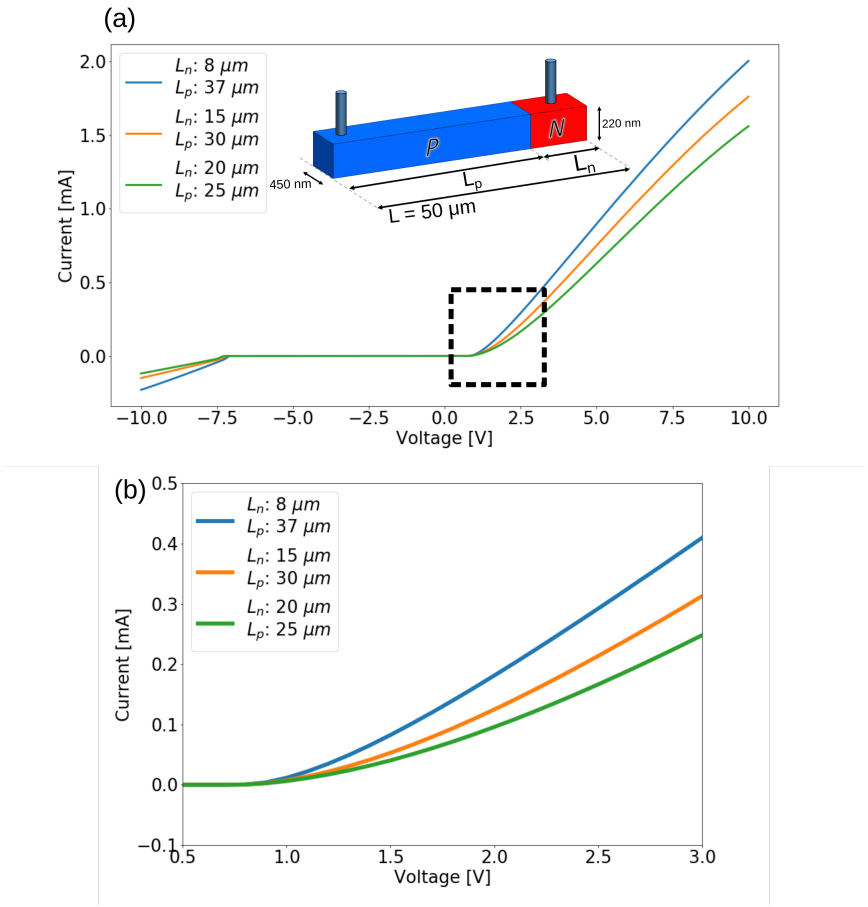

Figure 2.21: (a) IV-curves for diode heaters with different ratios of P and N-doped regions. (b) Zoom-in in the threshold region.

spectrum of the MZI filter, depending on which arm of the MZI we apply the phase shift [22]. To operate this device we need a total of three contact pads: one for a common ground and one more for each phase shifter, one on each arm of the MZI (Fig. 2.23(a)). As we don't intend to drive both phase shifters at the same time, we can use the heaters with integrated diodes and share the contact pads, reducing the footprint of the circuit, as illustrated in Fig. 2.23(b). In this implementation both heaters are connected in parallel, but with inverted polarity. Such scheme allows to drive either the top or the bottom heater depending on the polarity of the driving signal.

Fig. 2.24(a) shows the spectrum profile of the MZI in inactive state (center row, in red). Using this as a reference, we can show that driving the heaters with a

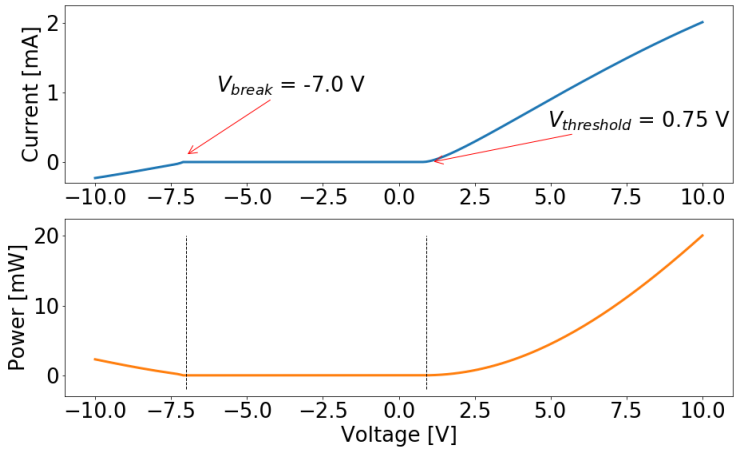

Figure 2.22: (top) IV curve of the standard diode heater used in this work. (bottom) Dissipated power in function of applied voltage in the diode heater.

DC signal will induce a shift in the spectral response of the MZI, and the direction of the shift depends on the polarity of the DC signal. For the first three rows we can see a blue-shift of the spectrum and in the bottom three rows, when we apply a signal with an inverted polarity, we observe a red-shift of the spectrum. In Fig. 2.24(b) we can see the measured spectrum shift (in nm) induced by the heaters as a function of the driving voltage. It is clear from these results that the circuit has two operating regimes, one for blue shift and other for red shift, depending on the polarity of the driving signal. We can also observe a region between $-1\ V$ and $+1\ V$ where we have almost no response from the heaters, because the bias is below the threshold voltage of the diode ($0.75\ V$). Outside this region the dissipated power grows quadratically with the applied voltage.

It is possible to further explore the use of diodes to multiplex the access to the phase shifters and reduce the number of contact pads needed to drive more complex circuits. We are coming back to this subject in chapter 4.

2.2.5 Time-constant of thermo-optical phase shifters

One characteristics of thermo-optical phase shifters is its very high time-constant. As such devices rely on the process of heating-up and cooling-down the waveguide, its reaction time depends on the thermal mass of the device (therefore, its size and fabrication material). Due its slow nature, phase shifters are often used as phase tuners, but seldom as modulators [1].

Fig. 2.25 shows the response of the an optical switch using a thermo-optical

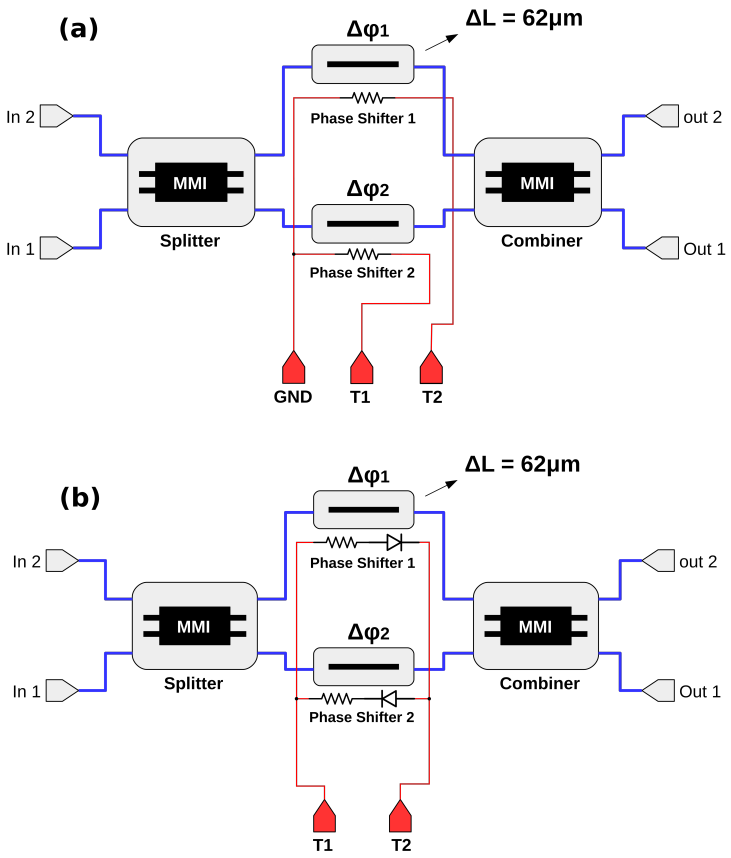

Figure 2.23: (a) MZI filter with two phase shifters to operate induce a red/blu shift in the spectrum response of the device. (b) Same circuit, but with diode heaters, using only two contact pads to operate the circuit.

phase shifter for a square wave driving signal of 2.4 KHz, with 50% duty cycle. We recorded a raising time (from 10% to 90%) in the order of 180 μs, which is equivalent of a time-constant[2] $\tau \approx 80\ \mu s$. This value gives us an indication about the order of magnitude of the time-constant of a thermo-optical based phase shifter. We are coming back to this subject in section 4.3.1 where we do a more in-depth analysis of the time constant of the thermal phase shifters and discuss how to exploit it to provide time-shared actuation for phase shifters.

[2]For a signal to rise from 10% to 90% we assume $t_{raise} \approx 2.2\tau$.

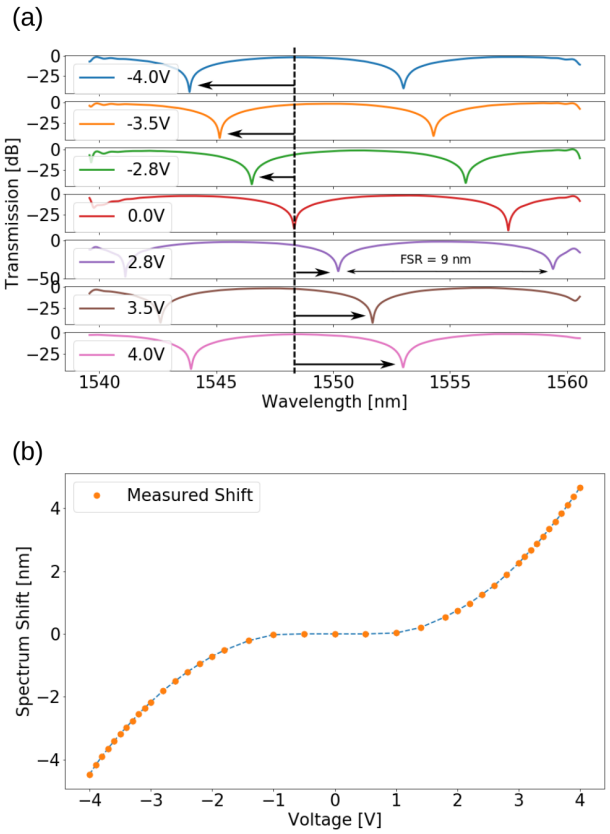

Figure 2.24: (a) Spectrum of the MZI filter for different values of voltage V applied to the phase shifters. (b) Spectrum shift in function of the voltage applied to the device.

2.3 Summary

In this chapter we discussed multiple ways to implement phase shifters by exploring the thermo-optical effect of silicon. We demonstrated that it is possible to postprocess heater onto a fabricated chip by depositing a metal-strip based resistor above the waveguide. We also showed that we can directly implement resistors using the doped silicon layer whenever it is available and, although initially it doesn't seems to perform as good as the titanium heaters, we can further improve the efficiency of the component by engineering the geometry of the phase shifter. Finally we demonstrated that it is possible to include a PN junction in the doped silicon heater to create a diode in series with the resistor. This breaks the symmetry of the resistor and allows polarity-dependent phase shift, which is used to drive multiple elements with fewer contact pads.

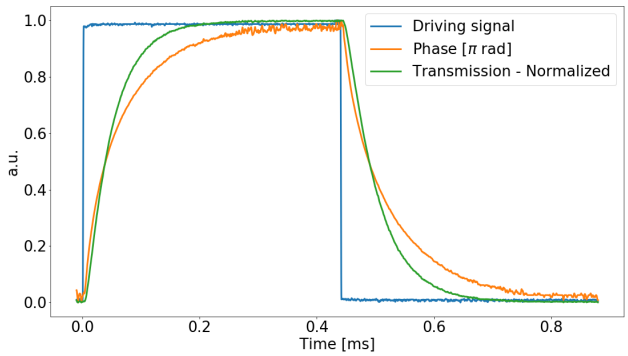

Figure 2.25: Time-domain response of a MZI-based optical switch using a doped silicon heater as a phase shifter.

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3
Optical Power Couplers

In silicon photonics, different applications emerge from splitting and combining light to implement resonators [1], interferometers [2], power distributions networks, among others [3, 4]. Optical power splitters and combiners are essential building blocks for the implementation of any photonics application.

In programmable photonics we extensively use tunable power couplers to add flexibility to the optical circuits [5]. As, by design, programmable photonics circuits requires a combination of a large number of components (hundreds or even thousands), it is key to employ building blocks that can yield good performance (low insertion loss, high extinction ratio) as the errors tend to accumulate along the circuit [6].

In this chapter we are going to discuss our design choices for both passive optical couplers (in particular, directional couplers) as well as the active tunable devices. We also are going to discuss how to implement a tunable coupler that can deliver good performance figures even when fabricated with imperfections.

3.1 Light manipulation: splitting and combining light

The simplest way to implement a power splitter in silicon photonics is by branching-out one waveguide to slowly divide it in two and split the guided mode between the two new waveguides (Fig. 3.1). This device is called a *Y-splitter*, and a reflectionless and lossless Y-splitter can be described by its S-matrix:

$$S_Y = \begin{bmatrix} 0 & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & 0 & 0 \\ \frac{\sqrt{2}}{2} & 0 & 0 \end{bmatrix} \tag{3.1}$$

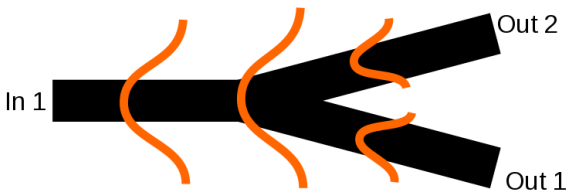

Figure 3.1: 3-port 1×2 splitter.

We can easily demonstrate that the power incident at port In_1 is divided between Out_1 and Out_2 from the S-matrix expression:

$$\begin{bmatrix} 0 & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & 0 & 0 \\ \frac{\sqrt{2}}{2} & 0 & 0 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} \end{bmatrix} \tag{3.2}$$

Therefore, $P_{out1} = P_{out_2} = |\sqrt{2}/2|^2 = 1/2$.

Although, if we excite port Out_1 instead, the sum of the power at the outputs is not equal to the input power:

$$\begin{bmatrix} 0 & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & 0 & 0 \\ \frac{\sqrt{2}}{2} & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{2}}{2} \\ 0 \\ 0 \end{bmatrix} \tag{3.3}$$

So, $P_{in} = |\sqrt{2}/2|^2 = 1/2$. This is a characteristic property of any symmetric 1×2 splitter[1]. Using such splitter in large circuits would result in losses when combining beams.

Because of that we implement the splitters and combiners as four-port devices instead (Fig. 3.2). Ideally a 4-port 2×2 optical coupler is described by the S-matrix:

$$S_{2\times2} = \begin{bmatrix} 0 & 0 & \sqrt{\tau} & -j\sqrt{\kappa} \\ 0 & 0 & -j\sqrt{\kappa} & \sqrt{\tau} \\ \sqrt{\tau} & -j\sqrt{\kappa} & 0 & 0 \\ -j\sqrt{\kappa} & \sqrt{\tau} & 0 & 0 \end{bmatrix} \tag{3.4}$$

[1]To be lossless, a passive device must have a S-matrix such that $S^\dagger S = I$. As S_Y is a singular matrix, the condition doesn't satisfy.

where κ is the *coupling coefficient* of the device. This value indicates the amount of light that couples from one input to its asymmetric output port (e.g., $In_1 \rightarrow Out_2$). For a lossless passive device, τ is the complement of κ, so: $\tau = 1 - \kappa$. This S-matrix representation holds for any passive implementation of 2×2 power splitters, such as *Multi-mode Interferometers* (MMI) and *Directional Couplers* (DC), although in real world implementations the reflection coefficient will mostly likely be different than zero.

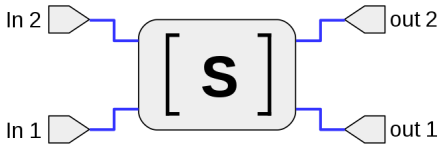

Figure 3.2: A generic 4-port 2×2 optical power coupler. The behavior of the component is given by its S-matrix.

3.1.1 Multi-mode interferometers

A multimode interferometer is essentially a multimode broad waveguide. Because the modes are eigenmodes, they propagate independently from one another, and at different rates. When an MMI is excited by an incident wave, the field profile is decomposed into the eigenmodes. Even though there is no exchange of energy between these eigenmodes, they propagate at a different velocity, and the result is an interference pattern that changes along the length fo the MMI.

The MMI has the advantage of being a broadband component [7–9] and very tolerant to fabrication [10]. On the downside, although possible, it is not trivial to design MMIs for arbitrary power split ratios [11, 12].

Because of the larger dimensions of the MMIs (when compared with a directional coupler), we preferred the use of directional couplers for the implementation of large scale PICs in this work, such as the mesh-based circuit, discussed in Chapter 6. The MMIs components used in circuits demonstrated during this work are standard components obtained from the imec PDK, and their design are not part of this work.

3.1.2 Directional Couplers

As discussed before, when light propagates in a waveguide the guided mode is not fully confined in the waveguide core, as the evanescent tail of the guided mode sits in the cladding of the waveguide. If we have two waveguides close together, the propagating mode of one waveguide will feel the second one. This will cause the power to couple from the first waveguide to the second one. This effect can

be used to create power distribution between waveguides, and it is the base of the operation of the directional coupler [13].

We can verify this coupling effect by simulating a pair of close waveguides, as illustrated in Fig. 3.3(a). In this arrangement the waveguides are 220 nm thick, 450 nm wide, Si core on SiO_2 cladding, and the separation gap between them is 250 nm. The simulation is performed for $\lambda = 1.55 \times 10^{-6}$ nm wavelength.

If we use a mode solver, we can calculate the guided modes of this pair of waveguides. The first thing we notice from simulation is that it gives us two guided supermodes: one with even symmetry (the *ground mode*) and a second mode with odd symmetry (the *first-order mode*) (Fig. 3.3(b)).

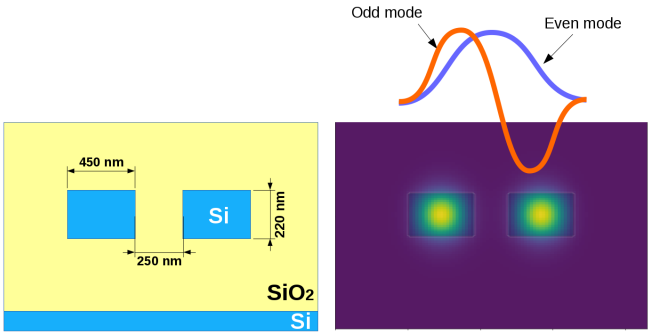

Figure 3.3: (a) Cross section of the simulated directional coupler. (b) Representation of the supermodes in the coupled waveguide pair.

From the simulation we obtain an effective index $n_e = 2.36596$ for the even (ground) mode and $n_o = 2.34508$ for the odd (first-order) mode. One important characteristics of these two supermodes is that, as they have different effective indexes, they will propagate at different speed. The interference between these two supermodes propagating at different speed will make the power couple back and forth between the waveguides in the system (Fig 3.4).

We can use *coupled mode theory* (CMT) [14] to infer the length L_c, where all the power will couple from the first waveguide to the second one (Fig 3.4). This value is given by the expression:

$$L_c = \frac{\lambda}{2 \cdot (n_e - n_o)} \tag{3.5}$$

where n_e and n_o are, respectively, the effective index for the even and odd supermodes. By plugging the simulated values in Eq. 3.5 we obtain:

$$L_c = \frac{1.55 \times 10^{-6}}{2 \cdot (2.36596 - 2.34508)} = 37.12\ \mu m \tag{3.6}$$

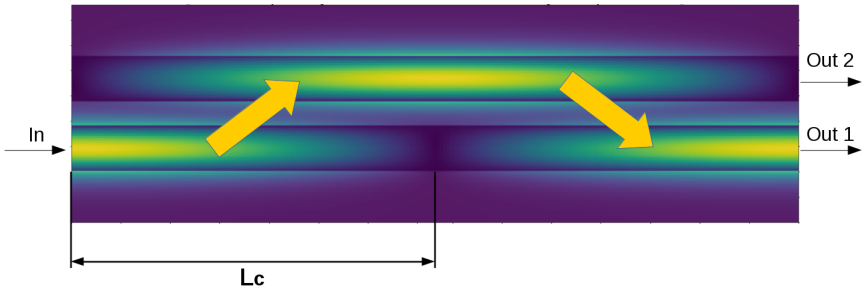

Figure 3.4: Simulated coupling between two waveguides.

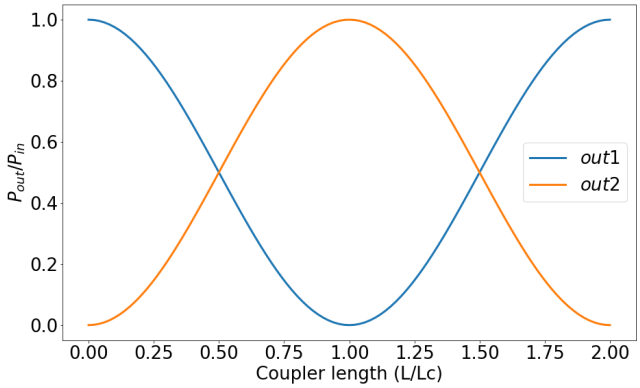

Figure 3.5: Coupling in function of the length of the coupler region.

If our coupling length L is smaller than L_c, we couple only a fraction of the light to the second waveguide. By choosing this coupling length L we can design the component to perform any arbitrary power coupling ratio. The optical power at each output of the directional coupler can be obtained from:

$$P_{out\_1} = \sin^2 \frac{\pi L}{2L_c} \tag{3.7}$$

and

$$P_{out\_2} = \cos^2 \frac{\pi L}{2L_c} \tag{3.8}$$

The plot from Fig. 3.5 shows the power split ratio between the two outputs of the directional coupler.

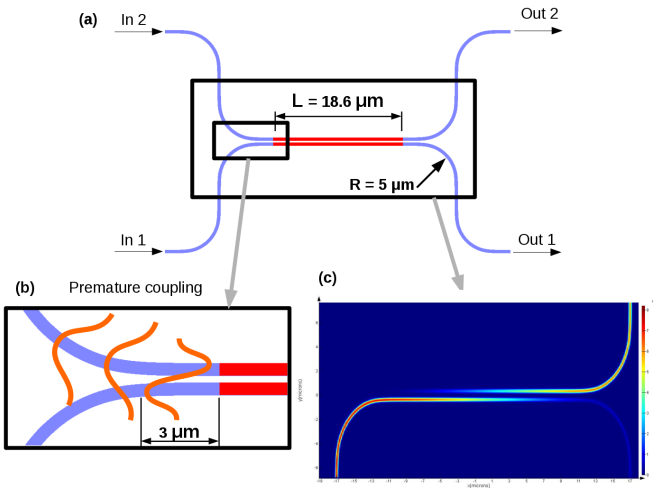

Figure 3.6: (a) Directional coupler with adiabatic bend transition waveguides. Notice that the straight section (in red) is the designed $L = 18.6\ \mu m$. (b) As the waveguides come closer to connect with the directional coupler we have premature coupling (which also happens in the right part of the coupler). Such coupling is not negligible, and have a big impact in the final coupling value. (c) FDTD simulation of the directional coupler. Notice that we have a hugh over-coupling and the device, designed to be a 50% splitter, falls out of the targeted region.

3.1.2.1 Design and optimization of directional couplers

To be made into an useful component, the ports of the directional coupler need to be connected to the rest of the optical circuit. For this it is important to fan-out the ports of the directional coupler to stop optical coupling outside the defined coupling length. Fig. 3.6(a) shows a directional coupler with four *S-shaped* bent waveguides used to define the ports of the device. The spacing between the ports guarantees that the only place where we have coupling is the designed coupling region. However, to make this fan-out, we create a non-straight transition region (Fig. 3.6(b)) that is not part of the originally designed coupling length where premature coupling may occurs. This results in a non-negligible additional coupling between the waveguides and will impact the final coupling ratio of the final device. This is particularly true for directional couplers designed using adiabatic transitions bends (as discussed earlier in Section 2.1.1). The spline curves used to define the geometry of the adiabatic bends increase the length of the transition region of the directional coupler, therefore increasing the premature coupling when compared to standard circular bends.

Fig. 3.6(c) shows the FDTD simulation of a directional coupler whose length L was designed to yield a 50% coupling ratio (therefore $L = L_c/2 = 18.6\ \mu m$).

As expected, we obtained a very high overcoupling, which makes almost all the power to be coupled to Out_2, completely invalidating the purpose of the device. Fig. 3.6(c) shows us that the transition section adds up to 6 μm of close waveguides[2] in the design (input and output transitions). This extra length, although not being completely straight, are close enough for premature coupling.

We can compensate for this premature coupling when designing the device by making the coupler length slightly shorter to balance out the extra coupling. To design a balanced $50/50$ directional coupler, our design approach was to calculate the coupling distance using Eq. 3.8 and, using FDTD simulation, refine the coupling length of the device by performing a length sweep around the original value of L. Fig. 3.7 shows the power coupling ratio for both outputs of the directional coupler in function of the length of the straight section of the device. This result was obtained from a FDTD simulation where we started with the calculated $L = 18.6\ \mu m$ and performed a six-steps sweep, decreasing the value of L at each step. Notice that the required length for a 50% splitter was obtained at $L = 13.47\ \mu m$, instead of the calculated $18.6\ \mu m$. This difference can be attributed to the long transition section (Fig. 3.6(b)) of the device.

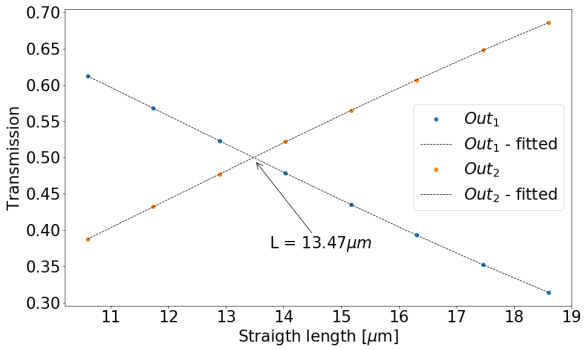

Figure 3.7: Output power at Out_1 and Out_2 of the directional coupler for different coupling lengths, operating at wavelength $\lambda = 1.55 \times 10^{-6}$. The value is from a FDTD simulation and includes premature coupling from the bend regions.

3.1.3 Wavelength dependency

One important characteristic that has to be discussed about directional couplers is its wavelength dependency. The wavelength dependency of a directional coupler can be deduced from Eq.3.5, derived from the coupled mode theory, which express

[2]It is worth mentioning that the fact that we use spline curves to perform the bends of our waveguides makes the transitions longer than they would be if we used simple circular bend.

the necessary length to couple the light between two coupled waveguides. As the effective index of the waveguide is wavelength dependent, this propagates to the final length required to implement a directional coupler to perform a given coupling ratio. As the fabricated directional coupler has a fixed length value, the result is a change in the coupling ratio in function of the wavelength.

Fig. 3.8 shows the transmission of the $50/50$ directional coupler designed in this work. The device shows a ± 0.1 change in the coupling coefficient over a transmission range of $50\ nm$, centered at $\lambda = 1.55 \mu m$. The simulation was realized using a FDTD simulation tool for a wavelength range $1.5\ \mu m < \lambda < 1.6\ \mu m$.

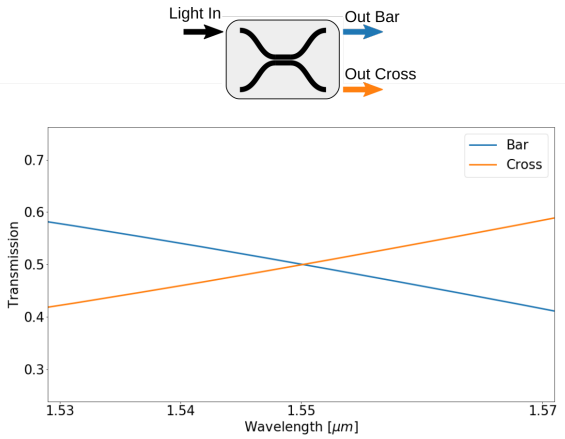

Figure 3.8: Simulated transmission of the designed directional coupler in function of the wavelength.

It is possible to reduce the impact of the wavelength dependency on the coupling coefficient of the directional coupler by introducing a phase compensation element in the device [15]. The same technique can be implemented in tunable couplers [16], which allows the optimization of the device for broadband operation after fabrication.

3.2 Tunable optical couplers

Programmable circuits largely rely on routing and combining light in a flexible way to perform different functions. Tunable power couplers are an essential part of programmable circuits, and its use in large scale circuits demands extra attention to its performance figures (i.e., low insertion loss, high extinction error, small footprint, high tolerance, etc.) as the imperfections accumulate over the circuit. In this section we discuss how we implement the tunable power couplers used in different implementations of programmable circuits.

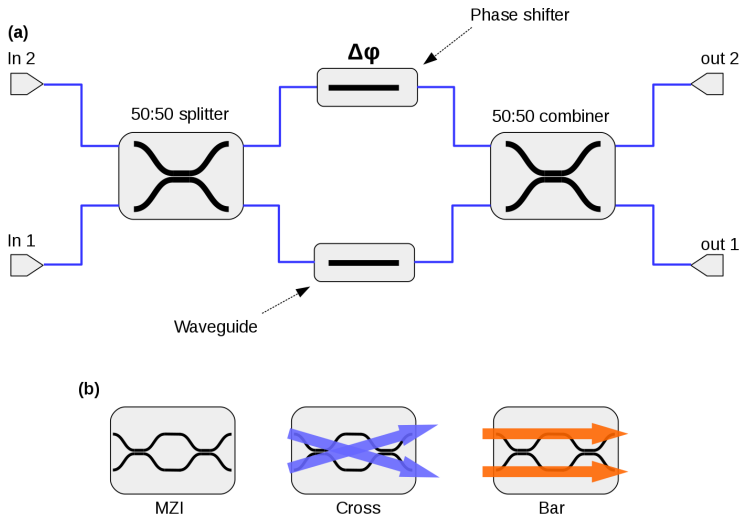

Figure 3.9: (a) Schematic of a typical 2×2 MZI with directional couplers as splitters/combiners. The directional couplers are designed to have 50% power split ratio. The device can have phase shifters in one or both arms, as long as the optical path are the same for both arms to keep the symmetry of the device. (b) MZIs, when operating as switches, can stay in two states regarding its transmission paths: cross and bar.

3.2.1 The Mach-Zehnder Interferometer

The Mach-Zehnder interferometer (MZI) is a device that can be employed as a modulator, wavelength filter, optical switch, and tunable power coupler [16–18]. The MZI is implemented using a pair of splitter and combiners, connected by waveguides (Fig. 3.9(a)). The waveguides connecting the splitter/combiners are called the arms of the MZI. A tunable power coupler is achieved using a symmetric MZI, where both its arms have the same optical length. Tunability is achieved by adding a phase shifter to one of the arms of the device. The 2×2 MZI (meaning two inputs, two outputs) used in this work are implemented with directional couplers as splitter/combiners and usually have two phase shifters, one on each arm of the device. For simplicity we are going to consider, for the moment, a MZI with only one phase shifter, as this is enough to operate it as a tunable power coupler.

When operating as a switch, a 2×2 MZI is in one of two states: a bar-state or a cross-state (Fig. 3.9(b)). That indicates the light path between the inputs/outputs of the system. However, when operating as a tunable power coupler, the state of the MZI is a linear combination of the cross and bar states, meaning that we can choose, by tuning the value of $\Delta\phi$, what percentage of light goes to each output of the device. This characteristic is an important feature for the implementation of programmable circuits, which relies on splitting and combining light by an arbi-

trary amount.

A 2×2 MZI can be seen as a three components circuit, each having four ports: a splitter, a pair of waveguides (for the arms), and a combiner. For a perfect, reflection-less device, we can represent it using the Transfer matrix (*T-matrix*). The *T-matrix* representation of the circuit is given by:

$$T_{MZI} = T_{combiner} \times T_{arms} \times T_{splitter} \tag{3.9}$$

The *T-matrix* of the pair of waveguides, including one phase shifter on the top arm (Fig. 3.9(a)), is given by:

$$T_{arms} = \begin{bmatrix} 1 & 0 \\ 0 & e^{j\phi} \end{bmatrix} \tag{3.10}$$

where ϕ is the phase induced by the phase shifter. By plugging together Eq. 3.4 and Eq. 3.10 into Eq. 3.9 we obtain:

$$T_{MZI} = \begin{bmatrix} (1-\kappa) + \kappa e^{-j\phi} & \kappa(1-\kappa)(1+e^{-j\phi}) \\ \kappa(1-\kappa)(1+e^{-j\phi}) & \kappa + (1-\kappa)e^{-j\phi} \end{bmatrix} \tag{3.11}$$

as the expression that governs the behaviour of the symmetric MZI with one phase shifter. The transmission of the MZI depends on the coupling coefficient κ of the directional coupler and on the phase shift ϕ applied to its arm (Fig.3.9(a)).

3.2.1.1 Design and optimization of MZIs

To implement tunable power coupler with symmetrical MZIs we use splitters and combiners with 50% power split ratio (we are going to discuss the impact of having $\kappa \neq 0.5$ in Section 3.3). By plugging $\kappa = 0.5$ in Eq. 3.11 we obtain:

$$T_{cross} = \cos^2 \frac{\phi}{2} \tag{3.12}$$

and:

$$T_{bar} = \sin^2 \frac{\phi}{2} \tag{3.13}$$

Fig. 3.10 shows the expected transmission of the device in function of the applied phase shift ϕ. The power output in the two ports of the device is symmetrical (e.g., for $\phi = \pi$, $T_{bar} = 1$ and $T_{cross} = 0$). One important aspect of this device is that it is a normal-cross MZI, meaning that when in its passive state (i.e., $\phi = 0$), it will remain in cross-state. This behavior can be manipulated in the design of the device by increasing the optical length of one of its arms using the expression:

$$\Delta\theta = \frac{\Delta L}{\lambda} \cdot 2\pi \cdot n_{eff} \tag{3.14}$$

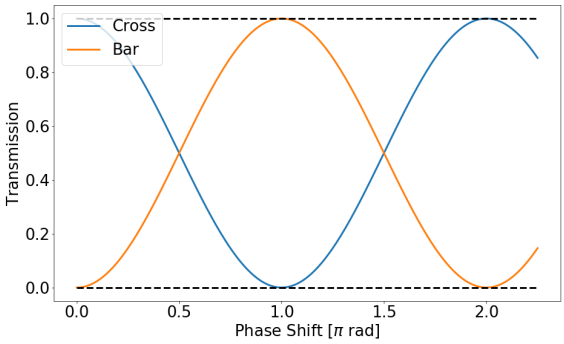

Figure 3.10: Theoretical transmission of a symmetric MZI in function of the phase shift applied to one of the arms of the device. Notice that both transmission path (bar and cross) cover the whole range of 0% *to* 100% *transmission. This situation only occurs when the splitter and the combiner have* $\tau = 0.5$.

where $\Delta\theta$ is the extra phase shift we want to introduce in the arm. The extra length will act as a permanent phase shift, changing the behavior of the device in passive mode. The MZIs implemented in this work were all normal-cross devices though, meaning that no extra length was added to the arms of the device.

We fabricated our MZI using the ISIPP50G platform from imec. The device was implemented using $50:50$ directional couplers as splitters/combiners and the arms are phase shifters implemented with doped silicon heaters. Fig. 3.11 shows the GDSII layout of the circuit (a) and the fabricated device (b).

3.2.1.2 Device characterization

To characterize the fabricated device we measured its transmission using a fiber-in/fiber-out approach (Fig. 3.12). We couple light into and from the chip using vertical coupling via grating couplers. The optical source is a laser at fixed wavelength ($\lambda = 1.55\ \mu m$) with optical power $P = 0\ dBm$. The output optical power is measured using an external power meter, and the heaters are driven using a variable power source operating as current source.

We characterized the fabricated MZI by measuring its transmission in both bar and cross states while driving the phase shifter in one of its arms. Fig. 3.13 shows the measured transmission of the device in function of the electrical power in the phase shifter. We can notice a very high extinction ratio $E.R. > 35\ dB$ for both bar and cross states. The insertion loss is below $-1\ dB$ for both cross and bar configuration. Table 3.1 shows the summary of the measurement results of this device. The results show that the fabricated MZI is a good candidate to operate as a tunable coupler in programmable circuits due its low insertion loss and high

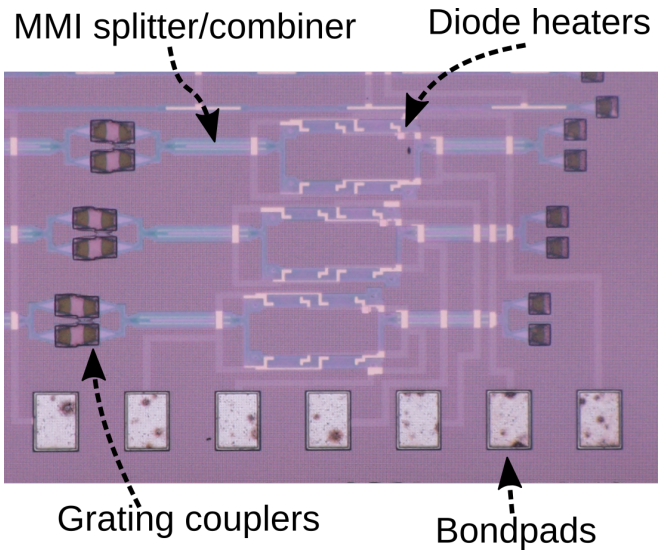

Figure 3.11: Microscope figure of the designed 2×2 *MZI.*

κ:	0.5
λ:	1.55 μm
I_{loss}:	$< 1\ dB$
E.R.:	$> 35\ dB$
Efficiency:	$18\ mW/\pi$

Table 3.1: Summary of the measurement results of the 2×2 *MZI implemented with directional couplers with* $\kappa = 0.5$.

extinction ratio in both cross and bar states.

3.2.2 Differential-mode and common-mode operation of MZIs

The MZI-based tunable coupler can be implemented with phase shifter in both arms, as illustrated in Fig. 3.14. In this configuration the transmission of the MZI is given by expression:

$$T_{cross} = \cos^2 \frac{\Delta\phi_{1,2}}{2} \tag{3.15}$$

and:

$$T_{bar} = \sin^2 \frac{\Delta\phi_{1,2}}{2} \tag{3.16}$$

where $\Delta\phi_{1,2}$ is the phase difference between the two phase shifters $\Delta\phi_{1,2} =$

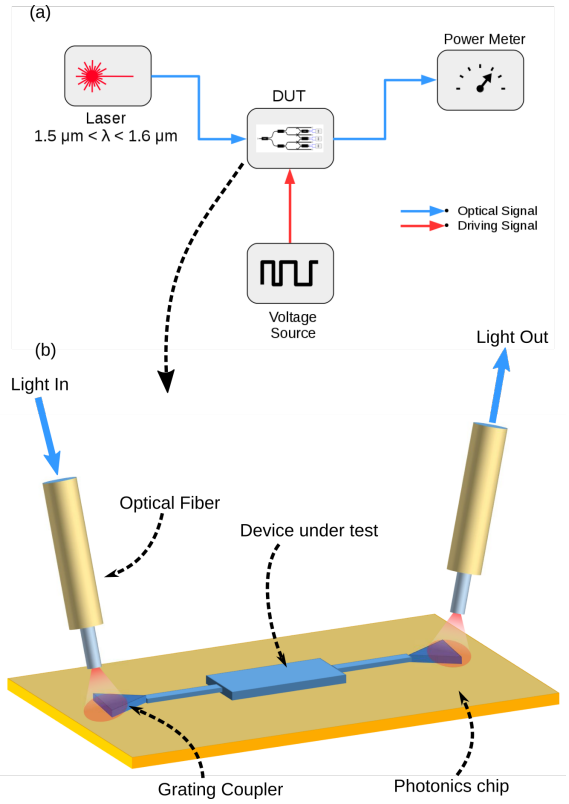

Figure 3.12: (a) Block diagram of the measurement set-up. (b) Illustration of the optical fiber coupling to the PIC via a grating coupler.

$\Delta\phi_2 - \Delta\phi_1$ (Fig. 3.14). This allows the device to be operated in two mode: differential-mode and common-mode driving.

In differential-mode we operate the phase difference $\Delta\phi_{1,2}$ to change the coupling coefficient of the tunable coupler. In this mode the MZI is operating as a standard tunable coupler as already discussed earlier.

The common-mode driving happens when we change both phases $\Delta\phi_1$ and $\Delta\phi_2$ by the same value. This doesn't affect the value of $\Delta\phi_{1,2}$, therefore doesn't change the coupling ratio of the tunable coupler, but allows the MZI, as a whole, to operate as a phase shifter, as a total phase change $\Delta\phi_{1,2}$ is applied to both outputs of the MZI. This construction is used in large scale programmable circuits as we can minimize the number of components in the circuit by using the same MZI to realize two functions: tunable coupling and phase shifting.

To operate the MZI in common mode we need a fine control over the values $\Delta\phi_1$ and $\Delta\phi_2$ applied to the phase shifters of the MZI, as we don't want to induce

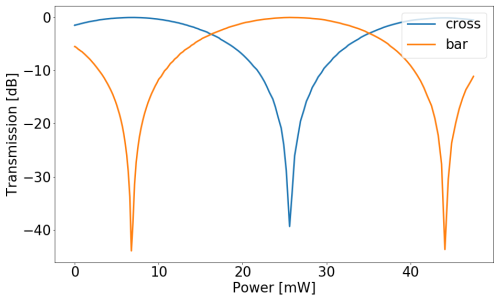

Figure 3.13: Experimental result of a tunable MZI. The device shows a good extinction ratio ($> 35dB$) and low insertion loss ($I_{loss} < 1dB$). The measurement was performed for a wavelength $\lambda = 1.55\ \mu m$

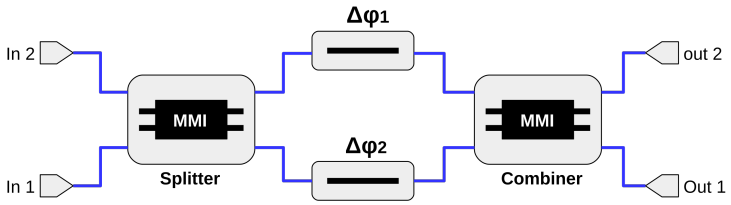

Figure 3.14: Schematic of the 2×2 MZI with phase shifter in both arms, implemented with MMIs as splitter/combiner.

any change in $\Delta\phi_{1,2}$ as well, which would change the coupling coefficient of the tunable coupler. As discussed earlier in Chapter 2.2.1.1, the phase shifter heater presents a non-linear resistance over the driving voltage applied to it, which can introduce challenges for a fine control of the phase delivered by the phase shifter. We will come back to this subject in Section 5.3.1.1, where we discuss control techniques to mitigate this issue and reduce the side-effects when operating the MZI in common-mode.

3.3 Tunable couplers with full extinction ratio

The transmission showed in Fig. 3.10 is only true for MZIs fabricated with perfectly balanced splitter/combiners ($\kappa = 0.5$). As directional couplers are highly sensitive to fabrication [19], any MZI designed using directional couplers will be directly impacted by the fabrication variation experienced by the directional coupler, therefore affecting the MZI performance. In this section we evaluate the impact of the transmission of a MZI for different values of κ and explore alternative

architectures of tunable couplers using cascaded MZIs.

3.3.1 Impact of κ in the construction of the MZI

The transmission of an MZI with imbalanced directional couplers will suffer an impact in its transmission. The plot in Fig. 3.15 shows the theoretical transmission of a MZI built with directional couplers whose coupling coefficient are $\kappa = 0.4$. It is possible to see that the maximum transmission in cross state doesn't reach 100%, while the minimum transmission in bar state doesn't get all the way to zero. That translates to a higher insertion loss in cross state and smaller extinction ratio in bar state. For $\kappa = 0.4$ we calculated a maximum transmission of 0.96 in cross state and a minimum transmission of 0.04 in bar-state. Although these figures might not look too threatening when looking onto one isolated device, in a circuit with a large number of MZIs (hundreds or thousands) the accumulation of this effect can have a huge impact.

Fig. 3.16 shows the theoretical maximum and minimum transmission values for cross and bar states for a MZI built with power coupler with different values of κ. Notice that we don't have a flat top/ceil in the plots, which means that only a perfectly balanced coupler would be able to implement a MZI that covers the $0\% - 100\%$ transmission range.

3.3.2 Tunable couplers with imperfect components

One way to address this issue is by concatenating two MZIs together (Fig. 3.17(a)), as proposed in [20], to achieve a more tolerant device. It has been reported that such arrangement can yield a tunable coupler that is able to cover the whole range of 0% to 100% transmission in both cross and bar state using any coupler with coupling coefficient $0.15 \leq \kappa \leq 0.85$ [20].

However, it is also possible to obtain an increase in the tolerance of the device regarding variations of κ with a reduced version of the cascaded MZIs [21]. Fig. 3.17(b) shows a MZI implemented with three splitter/combiners and two pairs of arms. This device, here named $2 \times 2 \times 2$ *MZI* (due the fact it is built with three couplers), makes use of the higher degree of freedom given by the extra coupler and phase shifter to increase its tolerance, while keeping a lower footprint and lower complexity when compared with the cascaded MZI from Fig. 3.17(a).

The transmission of the $2 \times 2 \times 2$ MZI is given by the *T-matrix* expression:

$$T_{2\times2\times2} = T_{DC3} \times T_{arms_2} \times T_{DC2} \times T_{arms_1} \times T_{DC1} \tag{3.17}$$

where, as before, T_{arms} is the transfer matrix of each group of two arms connecting the directional couplers and T_{DC} is the transfer matrix of the power couplers used to implement the device (in this specific implementation, DC stands for *Directional Coupler*).

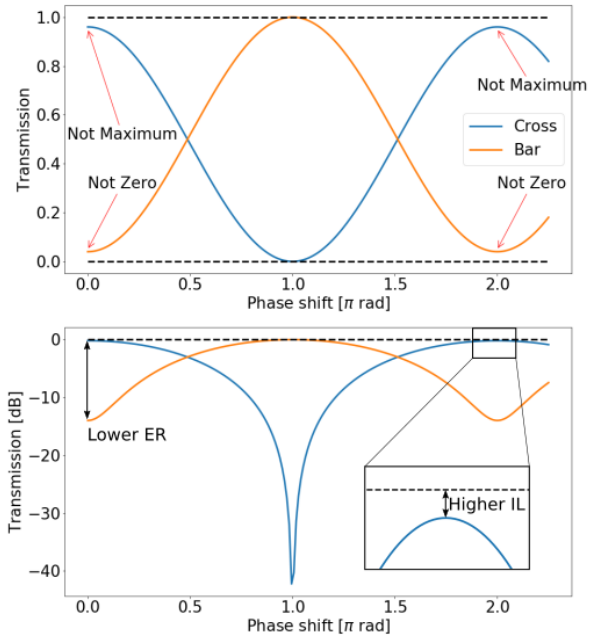

Figure 3.15: Cross and bar transmission of a MZI switch constructed with directional coupler with $\kappa = 0.4, \tau = 0.6$. The imbalanced coupler impact in the transmission response of the switch, increasing the insertion loss for cross state and reducing the extinction ratio for bar state.

In contrast with the simple MZI, where we need only one phase shifter to operate the device as a tunable coupler, this device offers two degrees of freedom, therefore now we have to drive two phase shifters (Ps_1 and Ps_2, Fig.3.17(b)), and it is the combination of these two phases that will set the device state.

Fig. 3.18 shows the simulated transmission of the $2 \times 2 \times 2$ MZI with $\kappa = 0.5$, evaluated for the phase space $0 \leq \phi_1 \leq 2\pi$ and $0 \leq \phi_1 \leq 2\pi$. We can see that the plot has clear peaks and valleys (in red and blue, respectively) where the transmission are at maximum and at minimum. Fig. 3.19 shows the simulated transmission of another $2 \times 2 \times 2$ MZI, but now with $\kappa = 0.27$. Notice that we still have the prominent peaks and valleys as before, but their position are shifted. Fig. 3.18 and Fig. 3.19 are in the same color grading scale.

If we evaluate the $2 \times 2 \times 2$ MZI for different values of κ ($0 < \kappa < 1$) and record the maximum and minimum theoretical possible values for cross and bar

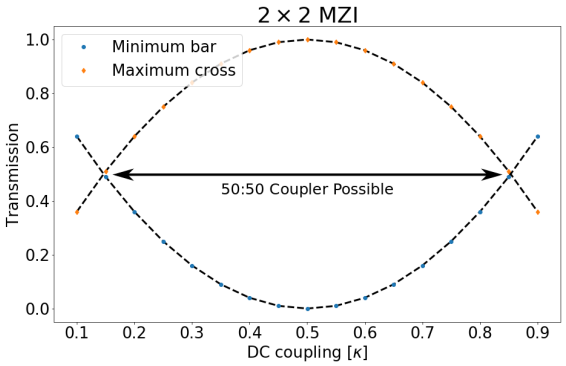

Figure 3.16: Theoretical maximum cross transmission and minimum bar transmission for a MZI constructed with directional couplers with different coupling coefficient κ. Notice that as soon as the coupling coefficient is not 50% we have an increase in the insertion loss of the device in cross-state and a reduction of the extinction ratio of the device in bar-state.

transmission of the device using Eq. 3.17 we can show that we can achieve full range transmission (0% to 100%) for a device constructed with any directional coupler with $0.25 \leq \kappa \leq 0.75$ (Fig. 3.20). When compared to the single MZI (Fig. 3.16) we notice that the $2\times2\times2$ MZI is highly tolerant regarding the coupling coefficient of its splitters/combiners. That shows that this architecture can be used to implement tunable couplers with very large operation range, minimizing the impact of fabrication variation of its components.

3.3.2.1 Design and Fabrication

We implemented the $2 \times 2 \times 2$ MZI using directional couplers as splitters/combiners and paperclip phase shifters for the arms of the device. Fig. 3.21(a) shows the GDSII layout of the fabricated device, while Fig. 3.21(b) shows the actual fabricated device from a microscope picture. The device was fabricated using the ISIPP50G platform from imec, which gave us the possibility to use doped silicon heaters and germanium photodetectors to monitor the circuit. The circuit was designed using the framework IPKISS, which enabled integration between design a circuit simulation.

The directional coupler used in this implementation has a coupling coefficient $\kappa = 0.27$. If used in a standard MZI, a directional coupler with this power split ratio would yield a maximum transmission of 80% in cross state and a minimum transmission of 20% if operated in bar state (see Fig. 3.20). Such values could invalidate its use in any application where a large operation range is needed, and would definitely invalidate its use in programmable photonics circuits. However, according to the theoretical analyses of the $2 \times 2 \times 2$ version of the de-

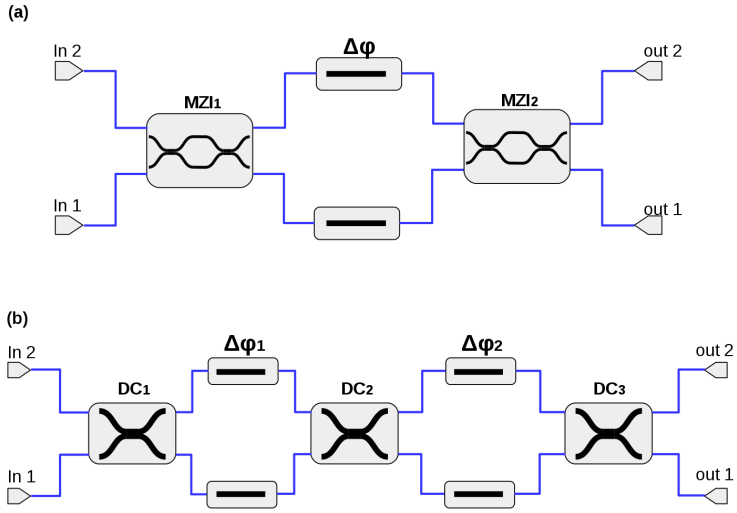

Figure 3.17: (a) Cascaded MZIs. This device requires four directional couplers and three phase shifters for its operation. (b) Reduced version, with three directional couplers and 2 phase shifters.

vice (Fig. 3.20), we should be able to cover the whole range of transmission in both cross and bar states for a device fabricated using directional couplers with $\kappa = 0.27$.

3.3.2.2 Characterization of the $2 \times 2 \times 2$ MZI

We measured the device operating as a tunable coupler for the wavelength of $\lambda = 1.616\ \mu m$. The reason to operate at this wavelength instead of the nominal $1.55\ \mu m$ is due to an error in the design of the device that led all the directional couplers to be fabricated with a shorter coupling length than the calculated value. This resulted in directional couplers with a coupling ratio exceptionally lower than expected. However, due to the wavelength dependency of the directional coupler, it was possible to operate the device at a higher wavelength, as the coupling coefficient of the directional coupler increases for longer wavelength values. A thorough analyses of this design error, as well as suggested measures to avoid this issue in the future is found in Appendix A.

The circuit was measured using a fiber-in-fiber-out setup, as illustrated in Fig. 3.12. We measured the transmission of the device for different power applied at Ps_1 and Ps_2, while recording the transmission of the device. We performed the measurement in both bar and a cross states.

In Fig. 3.22(a) we show the expected transmission of the device for different values of ϕ_1 and ϕ_2 obtained from simulation (the plot is done in logarithmic

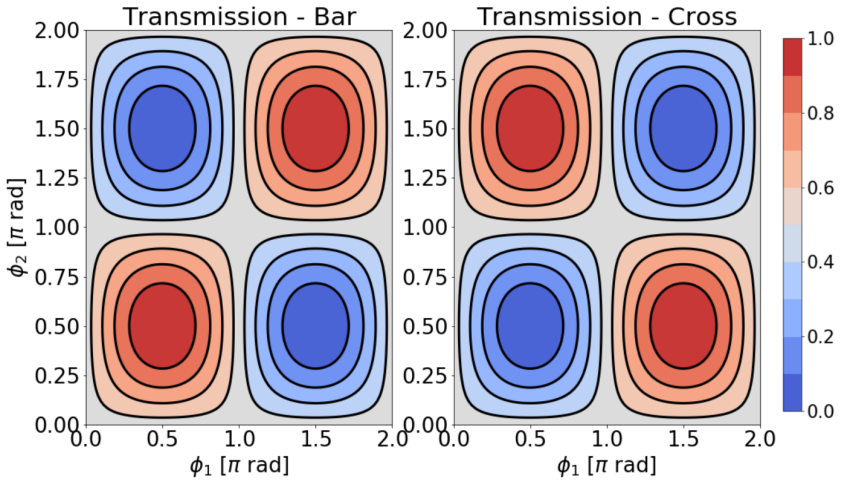

Figure 3.18: Bar and Cross transmission of a $2 \times 2 \times 2$ coupler with $\kappa = 0.5$, for different combinations of ϕ_1 and ϕ_2.

κ:	0.27
λ:	1.61 μm
I_{loss} bar:	1.1 dB
I_{loss} cross:	1.2 dB
E.R. bar:	> 20 dB
E.R. cross:	> 60 dB

Table 3.2: Summary of the measurement results of the $2 \times 2 \times 2$ MZI.

scale for easy comparison with the measurement results). Fig. 3.22(b) shows the actual measured transmission. We can notice a very strong qualitative agreement between simulation and measurement from these plots, which indicates that the device operates as expected.

Fig. 3.23(b) shows the transmission of the device across the scan line illustrated in Fig. 3.23(a). From this plot we can see a extinction ratio $E.R. > 20dB$ in the bar state. This result shows that the $2 \times 2 \times 2$ MZI, even when operating with very unbalanced directional couplers with coupling coefficient as low as $\kappa = 0.27$ can perform as well as single MZIs with perfect components. The recorded insertion loss in bar state is $I_{loss} = -1.1$ dB. Table 3.2 sums up the obtained results for this device. The results demonstrate that we can use this architecture to implement tolerant power splitters/couplers to be used in large scale silicon photonics circuits and, in special, in programmable photonics. We are going to discuss how to control the $2 \times 2 \times 2$ MZIs in section 5.3.2.

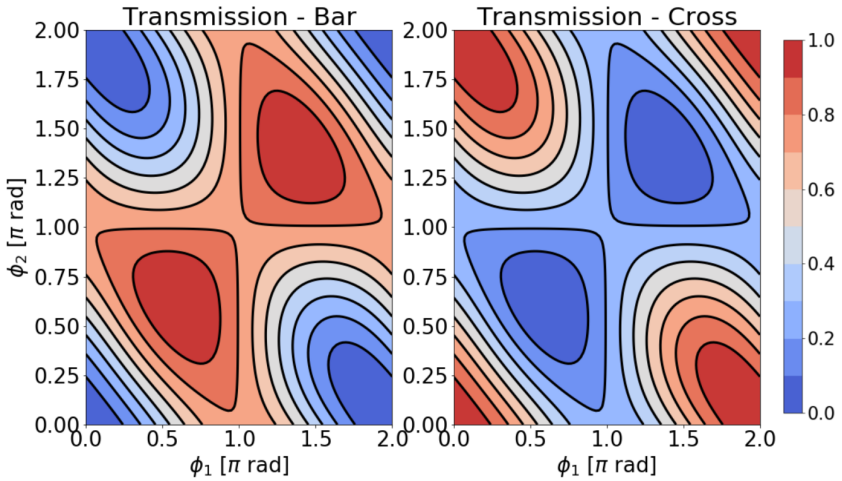

Figure 3.19: Bar and Cross transmission of a $2 \times 2 \times 2$ coupler with $\kappa = 0.27$, for different combinations of ϕ_1 and ϕ_2. Notice that the position of the maximum and minimum shifted related to Fig. 3.18, but the device still have pronounced maxima and minima.

3.3.3 Use and other considerations

The $2 \times 2 \times 2$ tunable coupler solves the issue of having imperfect components (due to errors intrinsic to the fabrication), while keeping a relative small footprint and a simpler control (only two degrees of freedom) when compared to the larger $2 \times 2 \times 2 \times 2$ version discussed earlier [20].

The device is a possible solution for implementation of high quality optical switches and tunable couplers in silicon photonics due its tolerance against variations in the fabricated device due to fabrication imperfections. For large scale circuits and specially programmable circuits, where error accumulation plays a big role in the final performance of the device, this architecture of tunable coupler is more robust against fabrication variability.

3.4 Summary

In this chapter we discussed how to split and combine light in a photonics circuit. We presented options for passive power coupling, such as MMIs and directional couplers. We explained our rationale to choose the directional coupler as our device of choice for mostly applications, as it allows the implementation of arbitrary power coupling ratio. We discussed how we use MZIs as tunable couplers, and introduced a lager version, the $2 \times 2 \times 2$ coupler, which is more tolerant to variation

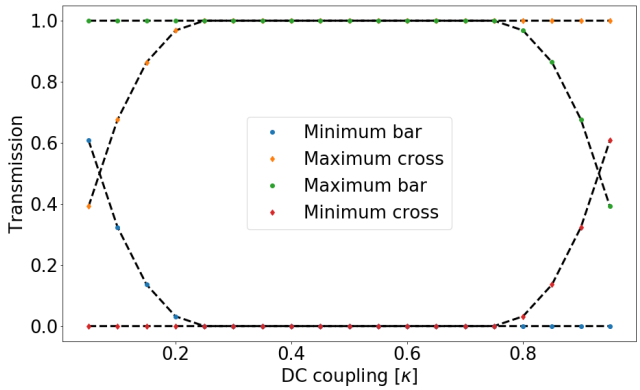

Figure 3.20: Theoretical maximum cross transmission and minimum bar transmission for a $2 \times 2 \times 2$ *MZI constructed with directional couplers with different coupling coefficient* κ*. Notice that when comparing to a simple MZI (Fig. 3.16) this device can be constructed with directional coupler from a broad range of* κ *while still cover the whole range of* 0% *to* 100% *transmission.*

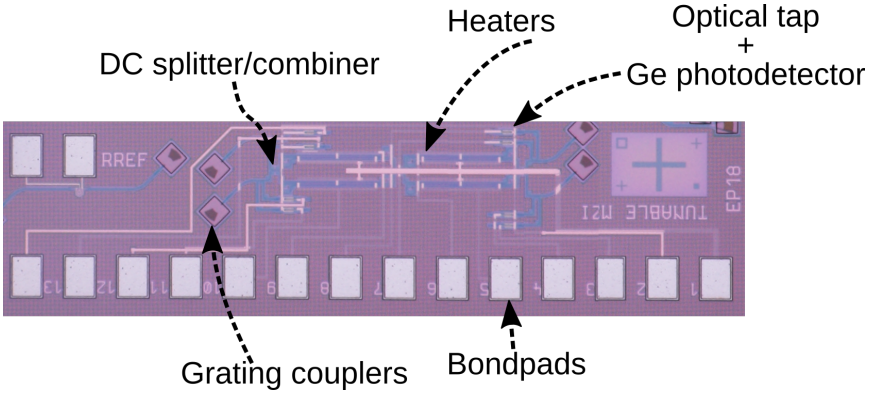

Figure 3.21: Microscope figure of the designed $2 \times 2 \times 2$ *MZI.*

in the fabrication process.

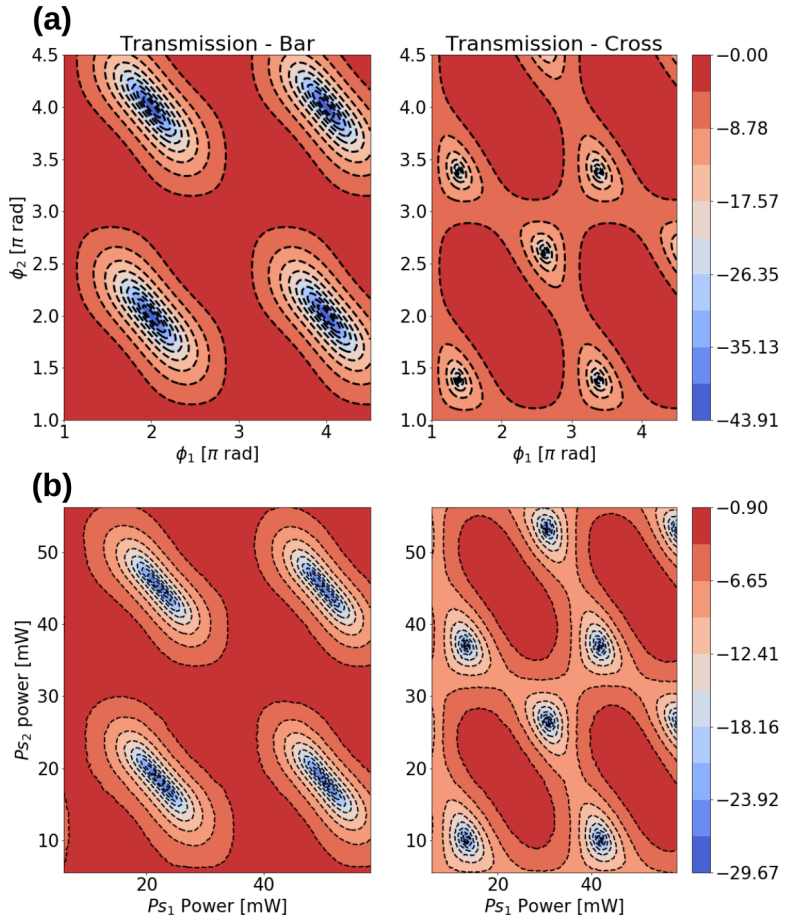

Figure 3.22: (a) Simulated result for the $2 \times 2 \times 2$ tunable coupler with $\kappa = 0.27$. This is the same plot from Fig. 3.19, but shown in logarithmic scale. (b) Measured transmission of the fabricated device. We have a strong qualitative agreement between simulation and experiment.

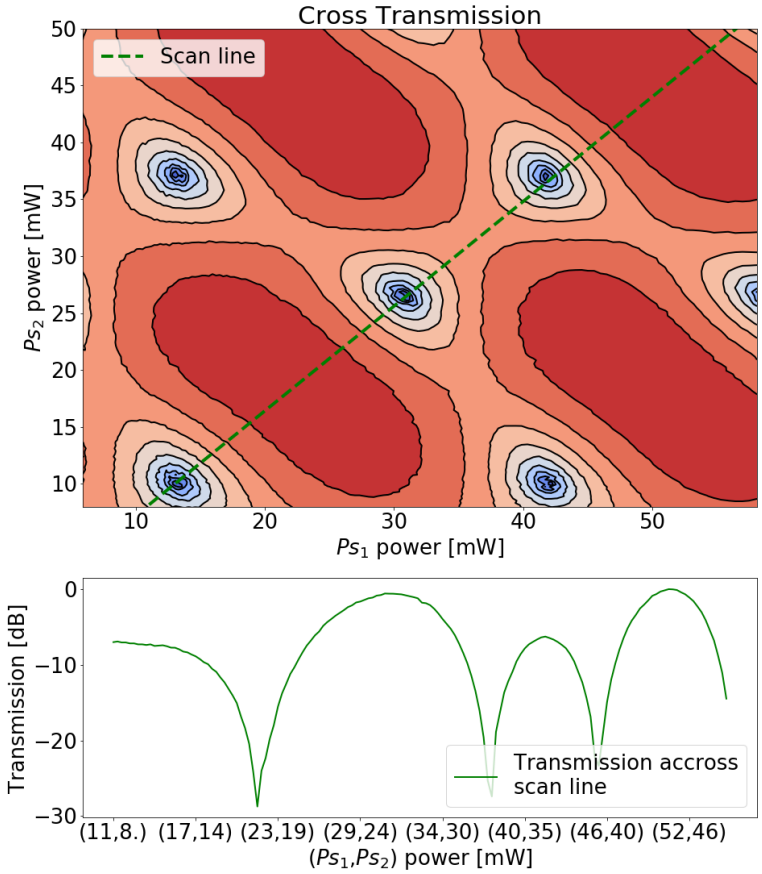

Figure 3.23: (Top) Bar-state transmission of the measured $2 \times 2 \times 2$ *MZI (*κ*=0.27) in function of the power at the phase shifters. (Bottom) Device transmission across the scan line. We recorded a insertion loss* $I_{loss} = -1.1\ dB$ *and an extinction ratio* $E.R. > 28\ dB$.

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4

Driving and Multiplexing Techniques

As the complexity of large scale PICs increase and the number of tunable elements in the circuit grows, more electronics is needed for driving the photonics circuits and enhance the photonics applications. More active elements means more electrical sources to drive the circuit, and more elements to control. This is even more pronounced in programmable photonics circuits, where the functionality emerges from the large number of controllable components [1]. To scale properly, a PIC with hundreds of controllable photonics components should not depend on having thousands of voltages source to actuate the circuit. Because of that it is necessary to employ specific techniques to make an efficient use of voltage sources for driving photonics circuits [2].

In this chapter we are going to discuss some driving techniques used to power large scale photonics circuits, with special focus on digital driving (using *Pulse Width Modulation* - PWM) to improve the linear response of the phase shifter and enable multiplexing access to the phase shifters, allowing us to drive multiple heaters with fewer contact pads and also reducing the number of voltage sources. Digital driving also reduces the complexity of the voltage sources, as we can use one stable source and avoid the use of *digital-to-analog converters* (DACs).

4.1 Heaters and parasitic resistances

The most straightforward way to drive a phase shifter is by using a controllable voltage source. In this approach we use one dedicate voltage source to drive the

heater, and the desired phase shift is obtained by controlling the voltage delivered by the voltage source.

Although existing [3, 4], monolithic photonics-electronics integration is not the most common approach used to integrate photonics and electronics elements. Alternatives such as 3D stacking [5] and flip-chip [6–8] can offer a tight integration with separated fabricated photonics and electronics chips. In this work we focus on off-chip electronics integration, where the electronics used to drive the optical chip is implemented outside the photonics environment (either using discrete electronics components or off-the shelf laboratory equipment), and the electronics signals are delivered to the PICs via its contacts pads interface.

Although in the final application we want to have the PIC bondpads wirebonded [9, 10] or flip-chipped to a *printed circuit board* (PCB) (Fig 4.1(b)), it is usual to use a multi-contact wedge probe (Fig. 4.1(a)) to perform temporary connection between the PIC and the exterior electronics. The advantage of using a multi-contact wedge probe is that it can be be used to perform quick experiments and tests in the PICs without committing to a wirebonding solution, which demands a dedicated PCB to be designed. Also wirebonding is a one-time process, as once a PIC is wirebonded to a PCB it typically cannot be used in a different setup. The downside of using a multi-contact wedge probe is that its performance is highly dependent on the mechanical stability of the setup, and minimal variations in the setup can have significant influence in the electrical resistance experienced by the electrical contacts.

When driving a phase shifter with a controllable voltage source we have to pay special attention to the parasitic resistances that might emerge in the circuit. Fig. 4.2 shows the equivalent circuit of a thermo-optical phase shifter with its series parasitic resistances. When driving such heater-based phase shifter, the effective power used to induce the phase shift in the waveguide is the power dissipated by the heater itself, therefore $P_{heater} = I_{heater} \cdot V_{heater}$. But due to parasitic resistances, such as the intrinsic resistance of the copper wires, the contact pads, and the tungsten plugs (R_{wires}, $R_{contact}$, and R_{plug}, respectively), we cannot guarantee that the voltage V applied to the circuit will be the same voltage V_{heater} experienced by the phase shifter heater.

Both R_{wire} and R_{plug} are intrinsic to the fabrication of the PIC and, therefore, controlled by the chip manufacturer. Their values are usually disclosed through the fabrication handbooks, and can easily be incorporated into the circuit model. The typical order of magnitude of a single tungsten contact plug[1] falls in the range of $100\ \Omega < R_{single\_plug} < 200\ \Omega$. As we usually use multiple contact plugs to ensure redundancy and reduce the current flow at each individual plug, we can

[1]The R_{plug} value includes: 1) the resistance of the pug itself, 2) the contact resistance between the copper layer and the tungsten plug, and 3) the contact resistance between the tungsten plug and the doped silicon strip.

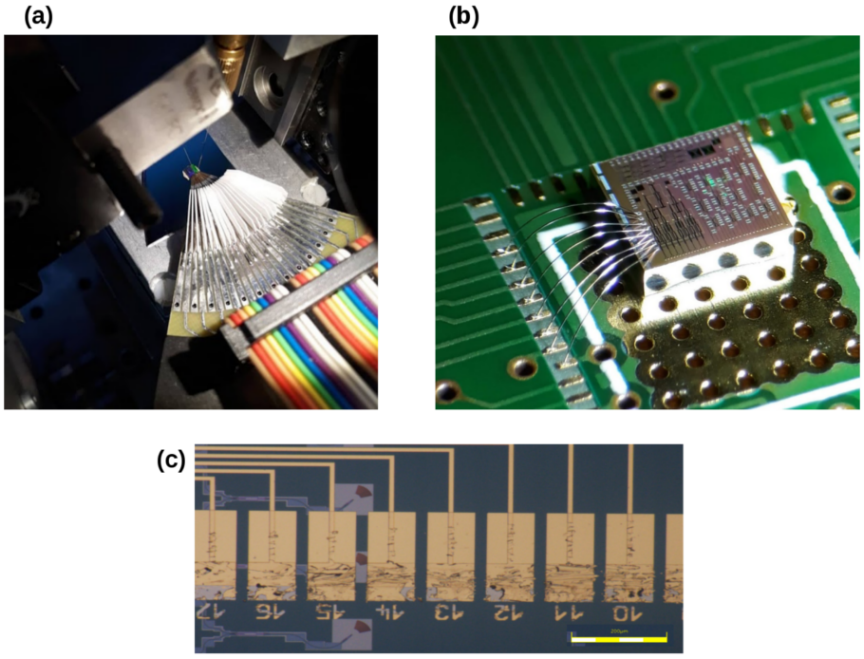

Figure 4.1: (a) Picture of a PIC under test contacted using a multi-contact wedge probe. (b) PIC wirebonded to a PCB. (c) Microscope picture of the contact pads of a PIC after using a multi-contact wedge probe.

assume $R_{plugs} \approx 20\ \Omega$.

The typical order of magnitude of a $10\ \mu m$ wide copper wire ranges between $2\ \Omega/mm$ and $5\ \Omega/mm$. As a typical doped-silicon heater resistance is in the order of kiloohms (see Chapter 2), the contribution of R_{wire} and R_{plug} can be disregarded in a first approach as the resistance of the heater is much higher than the value of R_{wire} and R_{plug}.

On the other hand, the value of $R_{contact}$ depends not only on the fabrication of the PIC, but also the mechanical contact between the PIC and the external electronics used to drive the optical chip. This value is low and can be equally neglected on stable wirebonded PICs, but whenever using a multi-contact wedge probe this is a serious source of uncertainty in the circuit. Fig 4.1(c) shows the contact pads of a PIC after being used with a multi-contact wedge probe (Fig. 4.1(a)) for a series of experiments. As the pads deteriorate with the mechanical contact, the resistance $R_{contact}$ can widely vary between iterations of use. Pad deterioration can increase the value of R_{pad}, but its value is hard to quantify due to the random nature of the process.

One solution to avoid dealing with the uncertainties of the parasitics introduced

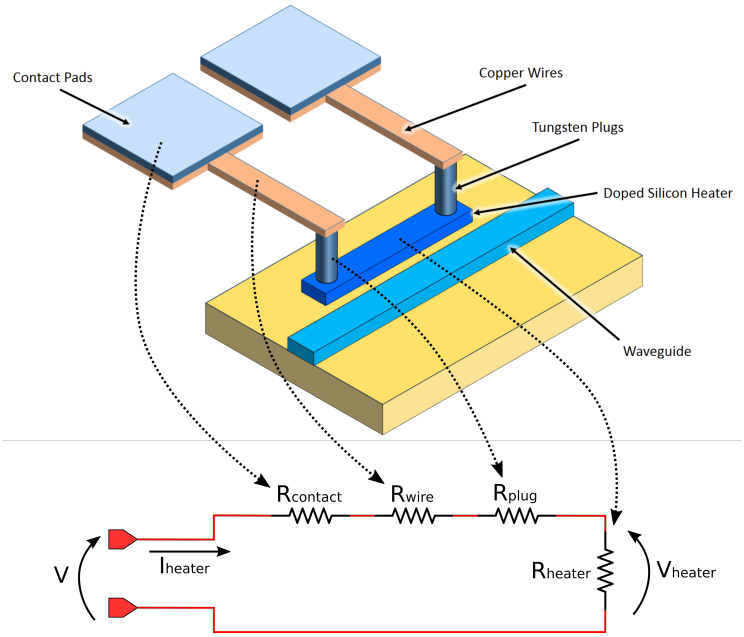

Figure 4.2: (top) 3D representation of the geometry of a doped-silicon heater based phase shifter and its wires and contact pads. (bottom) Equivalent electric circuit of the phase shifter, including parasitic resistances for the contact pads, wiring and tungsten plugs.

by the deterioration of the contact pad is to drive the heater with a current source instead. By applying a controlled current I_{heater} in the circuit, we have automatic control on the power dissipated by the phase shifter heater, regardless of the parasitic resistances. This approach is especially advantageous when contacting the circuit using multi-contact wedges (Fig. 4.1(a)), as the value of $R_{contact}$ might fluctuate at each use iteration.

It should be pointed though that current-based driving cannot be used with diode heaters, once a reverse-biased diode driven with a current source will be forced to operate in the *breakdown* region. Diode heaters have necessarily to be driven with a voltage sources. Because of that we recommend always wirebonding the PIC when driving diode-loaded heaters. For pure resistive heaters, whenever wirebonding is not a practical option and multi-contact wedge may be necessary, we should drive the heaters, preferentially, with a controllable current source.

4.2 Analog driving and non-linearity

Driving a heater with a *direct current* (DC) signal, although the most straightforward approach, comes with some drawbacks. The phase shift response of the

heater grows proportional to the silicon temperature, which is proportional to the power dissipated by the heater. A perfect heater has a power-vs-voltage response that grows quadratically with the increase of the applied voltage. Therefore we can express the phase shift in function of the applied voltage by:

$$\Delta\phi = A \cdot P = A \cdot \frac{V^2}{R} \tag{4.1}$$

where P is the power power dissipated by the phase shifter, R is the resistance of the heater, and A is a constant that relates to the efficiency of the phase shifter.

The biggest drawback from this quadratic behavior comes from the fact that the phase shift induced by a change ΔV in the driving signal depends on the current operating point of the phase shifter. Fig. 4.3(a) illustrates this effect. Notice that to induce the same phase shift $\Delta\phi = 0.87\ rad$ we need a $\Delta V = 2$ if the initial value of $V = 0$, while only $\Delta V = 0.6$ is necessary if the initial operating point is $V = 3$.

This behavior have a direct impact in applications where we have to induce the same $\Delta\phi$ in different phase shifters at different operating points, such as operating an MZI in common mode. In addition to that we have the fact that the heaters have a non-linear resistance (see Section 2.2.1.1), which increases the challenge of inducing equal phase shift on multiple phase shifter at once. We discuss our approach to mitigate this problem and control MZIs in common-mode with DC driving and Section 5.3.1.1.

In addition to that, this quadratic response translates into a non-linear error propagation from the voltage source to the phase shift. Any intrinsic precision error in the voltage level output from the driving source (such as DAC precision limitation) causes a phase error that is proportional to the square of the driving voltage (Fig. 4.3(b)).

Ideally we want to control our phase shifter using a function whose driving variable is directly proportional to the induced phase shift, as it facilitates the operation of the circuit. For our thermo-optical phase shifter that would mean driving the circuit with a variable source where the electrical power is the input variable. Although possible, such controllable power source are not practical to implement and would increase the complexity of the driving mechanisms. For that reason, whenever driving our circuit with a DC signal source we restrain to use a simple controllable voltage (or current) sources and compensate the quadratic behavior of the phase shifter by adjusting the voltage (or current) applied to the phase shifter.

We can compensate for this non-linearity driving issue by using a look-up table that correlates driving voltage and phase change for a given phase shifter. This is done by precalibrating the phase shifter to extract the transfer function of the heater. This function can be used to quickly retrieve the voltage level necessary to apply a given phase shift in the device. The disadvantage of this approach is that

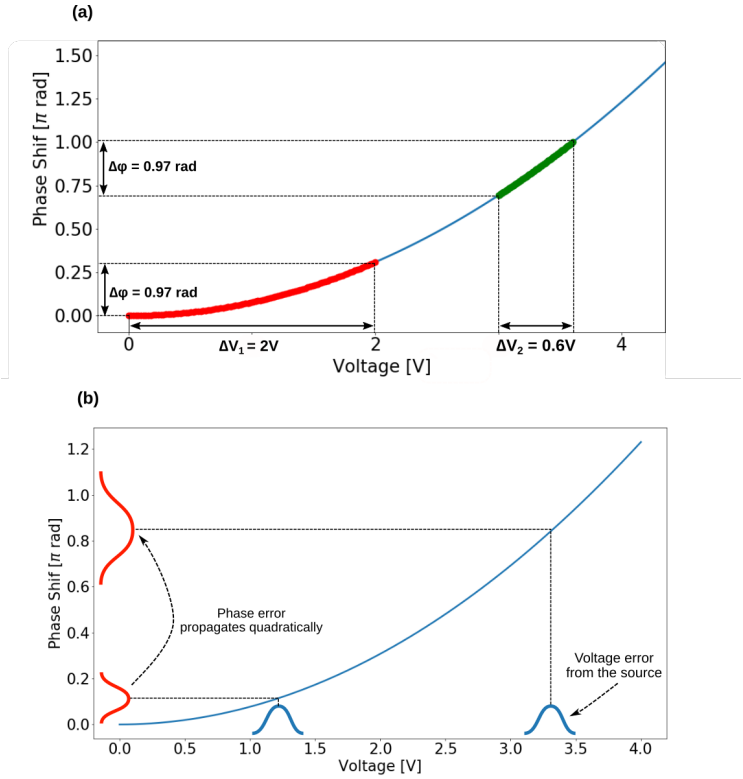

Figure 4.3: (a) Due to the quadratic response of the phase shifter when operating with a DC driving signal, we need different increments of ΔV to obtain the same $\Delta\phi$, depending on the operating point of the phase shifter. (b) Any error in the input driving signal coming from the voltage source will propagate quadratically to the induced phase shift.

we need to create one individual table for each element in the circuit and perform the calibration process for every phase shifter in the circuit before its use.

4.3 Digital driving

An alternative solution to avoid the non-linearity issues caused by the DC driving scheme is to power the phase shifter with a signal whose driving variable correlates linearly with the electrical power dissipated by the heater. One candidate for this is the use of a pulse-width modulated (PWM) signal [11, 12] (Fig. 4.4) to power the phase shifter, as the power delivered by a PWM signal is proportional to the duty cycle of such signal [2]. That means that a linear increase in the duty cycle of the PWM signal will result in an equally linear phase shift induced by the heater.

An additional advantage of using PWM signal to drive the phase shifters is that a PWM voltage source can be easier to construct than variable DC sources [13, 14].

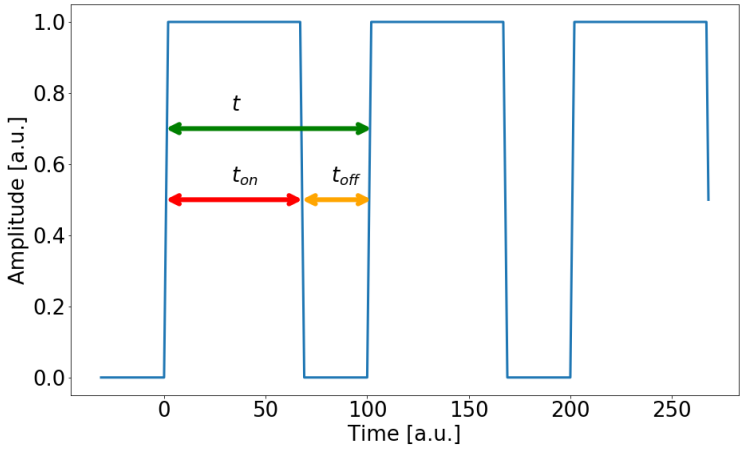

Figure 4.4: Pulse-width modulated (PWM) signal. The duty cycle (D.C.) of the signal is given by the ratio $D.C. = t_{on}/t$.

The reason we can use a digital signal to drive a thermo-optical phase shifter is due the very high time constant of heater-based phase shifter. As the phase shift induced by a heater is proportional to the temperature of the targeted waveguide, if we are able to drive the heater with a PWM signal that changes much faster than the thermal reaction time of the circuit, the resulting heat experienced by the waveguide will be averaged over the driving period. That means that the phase shift induced by the PWM driving wave will be constant over time, and proportional to the duty cycle of the PWM signal.

To be able to drive our phase shifter with a PWM signal we have to identify the minimum frequency f that can be used in the PWM signal that will only result in a constant phase shift over time, and not induce fluctuation ripples in the optical phase along with the PWM signal.

4.3.1 Frequency-domain analysis

We can model the thermal behavior of our thermo-optical phase shifter as an equivalent RC circuit to better understand the dynamics of the system. Fig. 4.5 shows a cross-section of a typical implementation of a doped-silicon heater based phase shifter and its equivalent thermal circuit.

For this simplified equivalent model we assume that all the heat is injected in the system through the heat source (Fig. 4.5), and will sink into the silicon

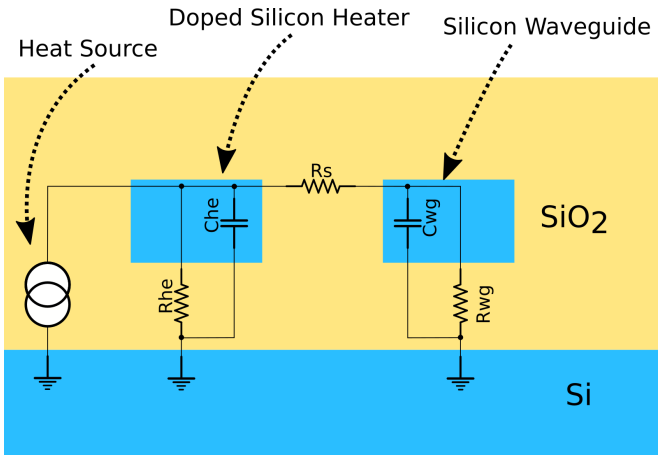

Figure 4.5: Cross-section of a thermo-optical phase shifter and its equivalent thermal RC model.

substrate of the PIC, which represents our ground level. The heat injected in the system through the doped-silicon heater is conducted to both the waveguide (via R_s) and to the substrate (via R_{he}). The heat from the waveguide flows to the substrate via R_{wg}. Both the heater and the waveguide have capacitor-equivalent elements (C_{he} and C_{wg}) that models the stored heat in each element. The RC constant given by the capacitor and the resistor dictates the heat-up and cool-down time of the system.

One characteristic of the RC equivalent circuit shown in Fig. 4.5 is that it behaves as a low pass filter. That means that our phase shifter will not be able to react fast enough for a driving signal whose frequency is above the cut-off frequency of the equivalent RC circuit, and it will only see the low frequency component of the driving signal[2]. We can predict this cut-off frequency if we treat the response of the thermo-optic phase shifter as a low-pass RC circuit, and plug the actual measured time constant value of the phase shifter in the RC circuit to realize a frequency-domain simulation.

4.3.1.1 Time constant extraction

To extract the time constant of the phase shifter we used it in an MZI circuit operating as a switch (Fig. 4.6(a)) and applied an electric signal to switch the MZI from a bar to a cross configuration while measuring its transient response (Fig. 4.6(b)).

The transmission of a MZI in function of the phase shift ϕ is given by the expression:

[2]For a single-polarity signal such as the one shown in Fig. 4.4, the low-frequency component is proportional to the average of the signal over time.

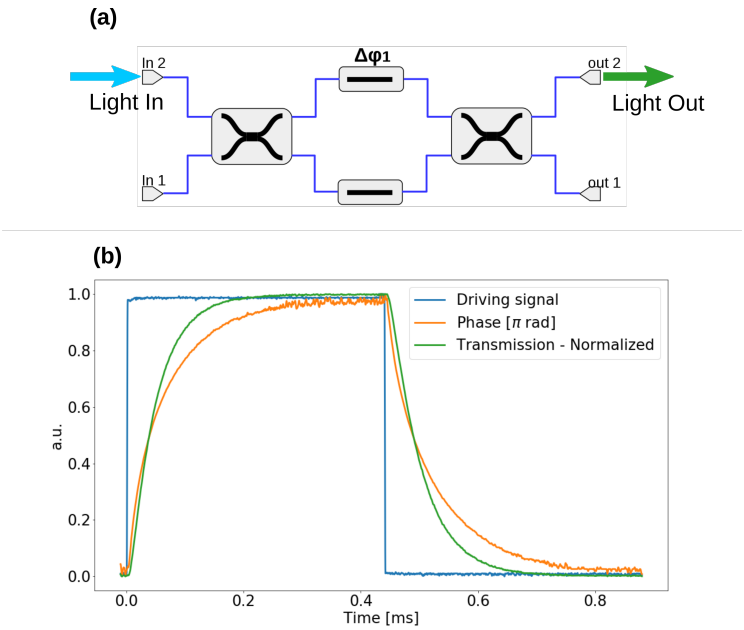

Figure 4.6: (a) MZI circuit used to extract the RC constant of the phase shift. (b) Transmission of the MZI and phase response of the phase shifter in function of time.

$$T = \cos^2 \frac{\phi}{2} \tag{4.2}$$

Rearranging Eq. 4.2, we can express the phase of the phase shifter in function of the MZI transmission:

$$\phi = 2 \cdot \arccos \sqrt{T} \tag{4.3}$$

By applying Eq. 4.3 to the transmission response of the MZI we can extract the phase induced by the phase shifter. Fig. 4.6(b) shows the measured response of the MZI and the extracted phase shift in function of time for a step driving signal.

We recorded the time constant τ by measuring the time it takes to the phase signal to reach 63.2% of the rising value (or the inverse 36.8% of fall value), as shown in Fig.4.7. We can observe a slightly different RC constant for the heat-up and cool-down phases ($\tau_{charging} = 77.5\ \mu s$ and $\tau_{discharging} = 97.5\ \mu s$), but as we want the determine the minimum signal frequency needed to drive the circuit we assume that the RC constant of the circuit is the result for the worst-case scenario, so $RC = \tau_{charging} = 77.5\ \mu s$.

Even though the heat transfer is a linear process, which means that the actual heat-up and cool-down of the waveguide is also a linear process, we registered

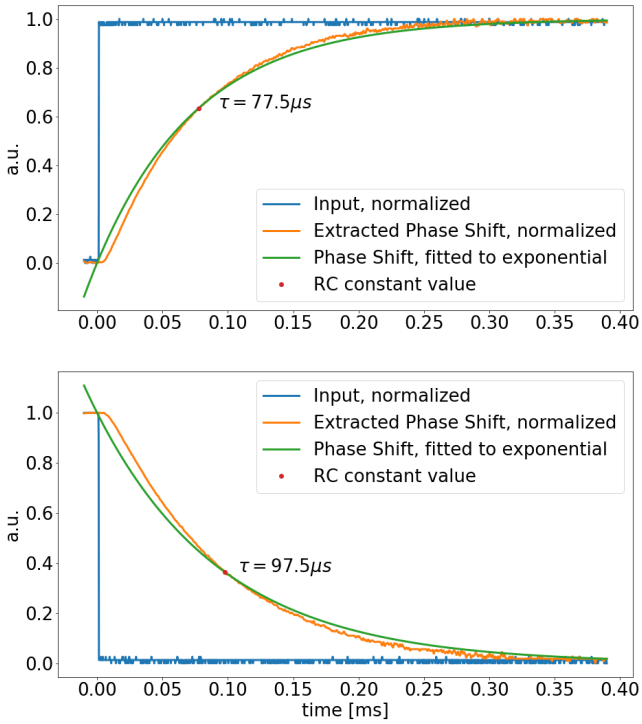

Figure 4.7: Measured time constant for a paperclip-shaped phase shifter with doped-silicon heaters.

different values for the rise and fall time constants of the phase shifters. The reason why it is possible is because we are not directly measuring the heat transfer, but a change in the phase shift induced by the change in the temperature of the device. This process includes other factors such as the non-linearity of resistivity of the heater (as discussed earlier in Chapter 2), the electronics used in the experiment, and the thermo-optical effect of the silicon.

4.3.1.2 Simplified RC model simulation

With the obtained value for the RC constant we recreate our circuit model in a SPICE simulation to extract the frequency-domain response of the circuit. For this we approximate the response of the phase shifter to a RC low-pass filter where $R \cdot C = \tau = 77.5\ \mu s$.

The resulting simulation can be seen in Fig. 4.8, where we plot the attenuation in the amplitude of V_{out} as a function of the frequency of the driving signal. According to this model, a driving signal whose frequency $f > 500\ KHz$ should meet the requirements to power our phase shifter without introducing phase shift fluctuations over the time.

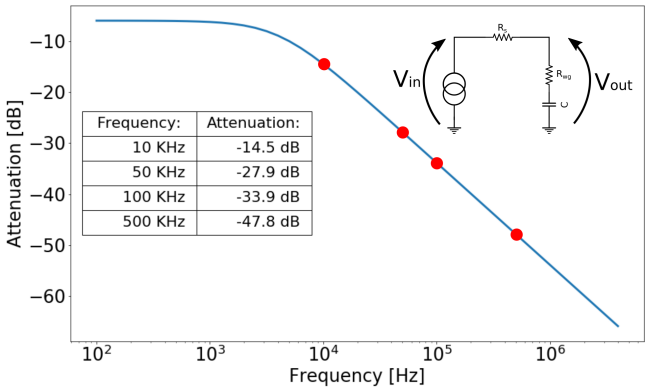

Figure 4.8: Amplitude attenuation (V_{out}/V_{in}) of the thermal equivalent circuit (inset) for a RC constant $\tau = 77.5\ \mu s$.

4.3.1.3 Experimental verification

We can confirm the prediction shown in Fig. 4.8 by driving the MZI with a square wave signal with different frequencies. From that we extract the induced phase shift for the different signals. Fig. 4.9 shows the extracted relative phase fluctuation (how much the phase of the optical signal changes relative to its average value) for

four different driving signals of same amplitude but different frequencies. We can notice that for signals of low frequencies (such as $f = 10\ KHz$ and $f = 50\ KHz$) we can clearly see that the phase of the optical signal vary over time. For a driving signal of slightly higher frequency of $f = 100\ KHz$ we can see that the phase fluctuation over time is drastically lower, although still noticeable. Finally, for a driving signal with frequency $f = 500\ KHz$ we can no longer notice a phase fluctuation over time, remaining only the average induced phase shift induced by the square wave. From this we conclude that we can use a square wave signal (such as a PWM signal) to drive our phase shifter if the signal has a frequency $f = 500\ KHz$ or higher.

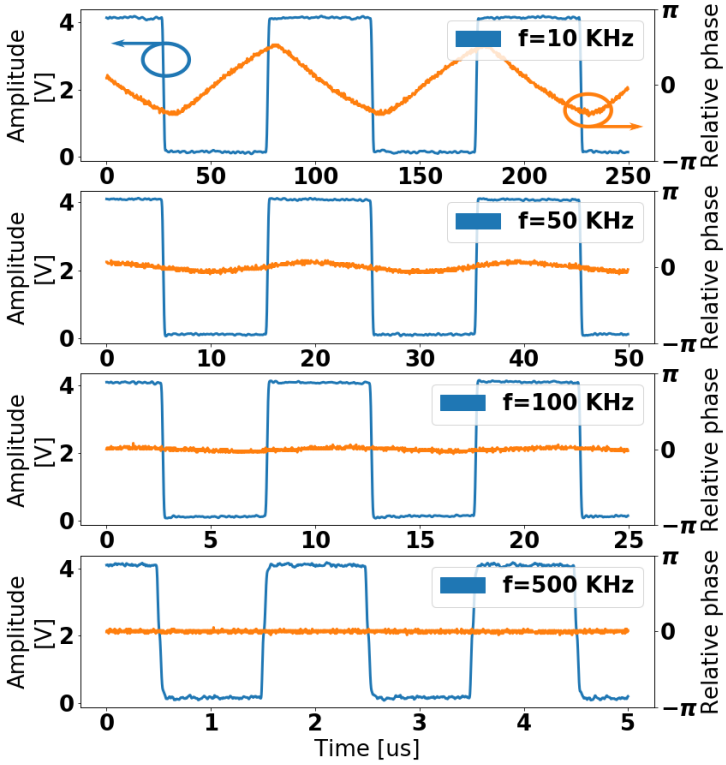

Figure 4.9: Measured relative phase shift fluctuation for different frequencies of the PWM signal shows a constant phase response for the signal frequency $f = 500\ KHz$. The expected attenuation for the plotted frequencies are marked in the diagram in Fig.4.8.

4.3.2 PWM-based driving

To validate the use of a PWM signal to drive thermo-optical phase shifter we used it to tune the spectrum response of an asymmetric MZI filter (Fig. 4.10). Our MZI filter is designed with phase shifters in both arms, which allows us to induce either a blue-shift or a red-shift in its spectrum, depending on which phase shifter we actuate. The phase shifters are implemented with diodes heaters, and are routed in parallel, but with opposite polarity. This allows us to define which heater is being actuated depending on the polarity of the driving signal.

To drive the MZI filter we used a PWM signal with an amplitude of $5\ V$, which is enough to induce a $\pi\ rad$ phase shift with a duty cycle $D.C. = 100\%$. That means that we are able to cover the whole *free spectral range* (FSR) of the MZI filter by performing either a blue-shift or a red-shift. The frequency of the PWM signal is $500\ KHz$.

Fig. 4.11(center row) shows the spectrum of the unpowered MZI filter (driving signal with 0% duty cycle) to be used as reference. On the bottom rows we can see a red-shift in the spectrum of the filter as we increase the duty cycle of the driving signal. The top three rows shows the spectrum of the same filter, but now driving with a PWM signal with an inverse polarity as before (thus the negative sign in the duty cycle value). In that case we can see that we have an increase in the blue-shift of the spectrum as we increase the negative duty cycle of the PWM driving signal. From the plots we can conclude that we can shift the spectrum of the MZI filter to cover the whole FSR by adjusting the duty cycle of the PWM signal (and its polarity).

Fig. 4.12(a) shows the induced spectrum shift in the MZI filter in function of the duty cycle of the PWM signal used to drive the circuit, measured for different values of the duty cycle. We can notice that the induced spectrum shift grows linear with the increment in the duty cycle of the PWM signal, which agrees with our predicted behavior. The gain in the linearity response of the phase shifter is clear when we plot together both the PWM and the DC driven results (Fig. 4.12(b)). From that plot we conclude that driving a thermo-optical phase shifter with a PWM signal is a possibility and that the technique increases the linearity of the response of the device.

4.3.3 Duobinary driving

When we introduced the diode heater in Chapter 2.2.4 we demonstrate its use to perform a red/blue-shift in a MZI filter, depending on the polarity of the driving signal. We argued that the technique allowed us to use fewer pads to drive more elements, therefore reducing the footprint needed for multiple contact pads. In that example we actuate either one phase shifter or other, but it doesn't allow us to use both phase shifters at the same time. In this section we are going to explore how to

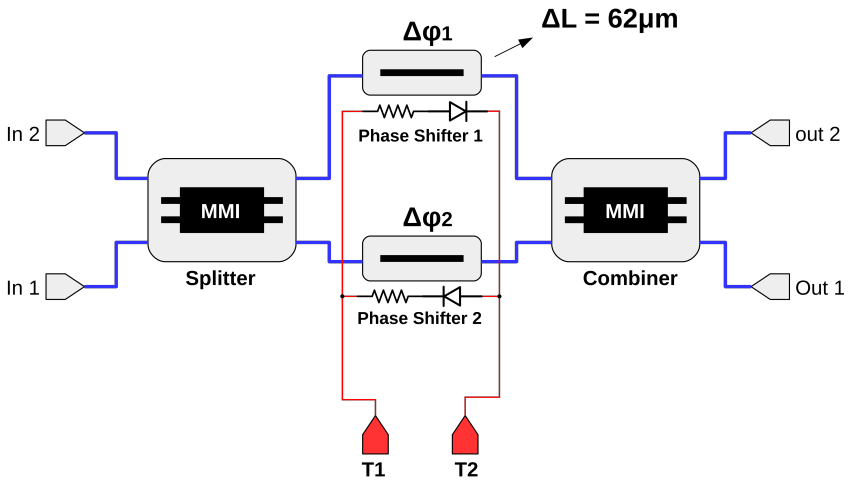

Figure 4.10: MZI filter with $FSR = 9\ nm$. The MZI is equipped with diode heaters in both of its arms arms. Notice that the diodes heaters are routed in parallel, but with opposite polarities.

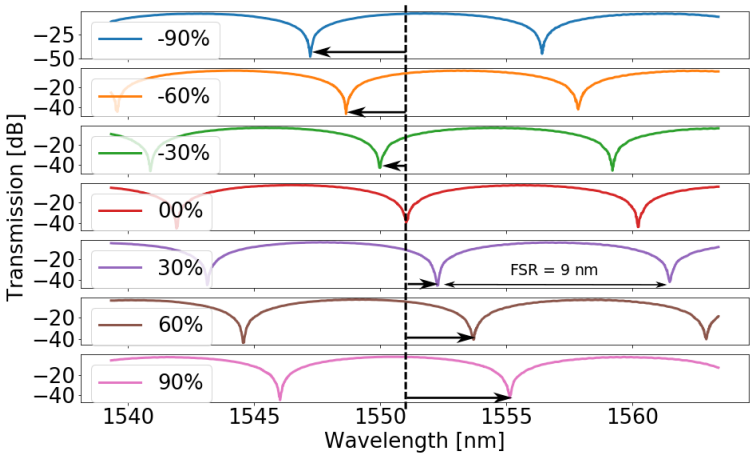

Figure 4.11: Spectrum of the MZI filter from Fig. 4.10 for PWM signals with different duty cycle values. A negative duty cycle represents a PWM signal with negative voltage polarity.

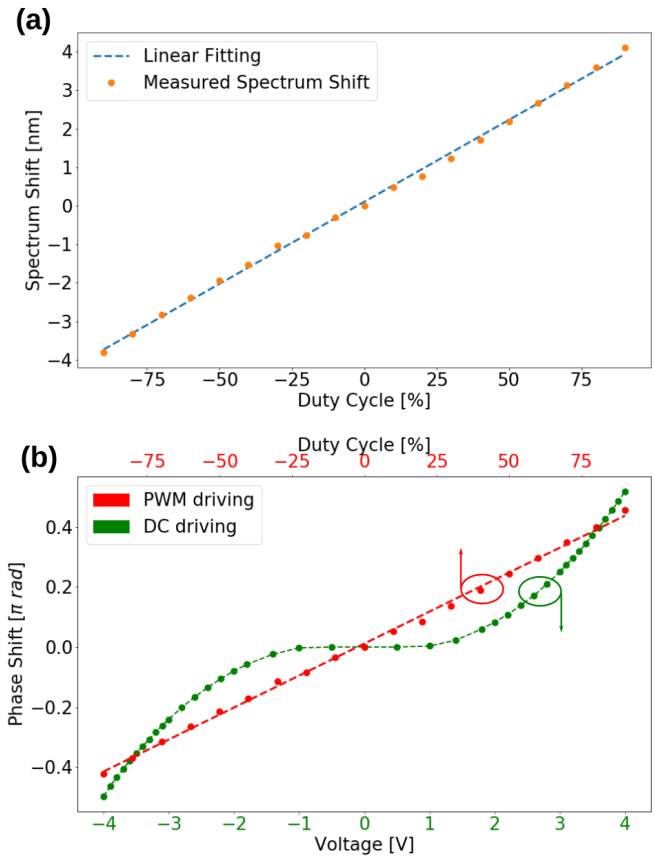

Figure 4.12: (a) Spectrum shift as function of duty cycle of the PWM driving signal. (b) Direct comparison between a PWM driven spectrum shift response and DC driving.

use a duobinary PWM signal to independently drive two phase shifters at the same time using a single pair of contact pads. This technique is based on time-sharing the access to the heaters, and will be further explored in the coming sections as the base of our solution for driving circuits with large number of active elements.

To demonstrate the technique we designed a circuit with two ring resonators (Fig. 4.13(a)) with slightly different round-trip length. The difference in the size of the rings results in a spectrum with two distinct resonance peaks close to each other, each resonance peak linked to a ring resonator (Fig. 4.13(b)). Each ring resonator has a diode-loaded thermo-optical phase shifter on it (Fig. 4.13(a)), which allows us to change the resonance frequency of the ring. The two phase shifters are routed in parallel, but with opposite polarities (Fig. 4.13(a)) in such way that

the polarity of the driving signal governs which phase shifter will be actuated. We can see this working effect in the plot in Fig. 4.13(b). In the top row we see a shift in the resonance of $RingA$, while at the bottom row, as we drive the circuit with a signal with inverse polarity, we clearly see a change in the resonance of $RingB$. In this first example we are actuating on only one heater at the time.

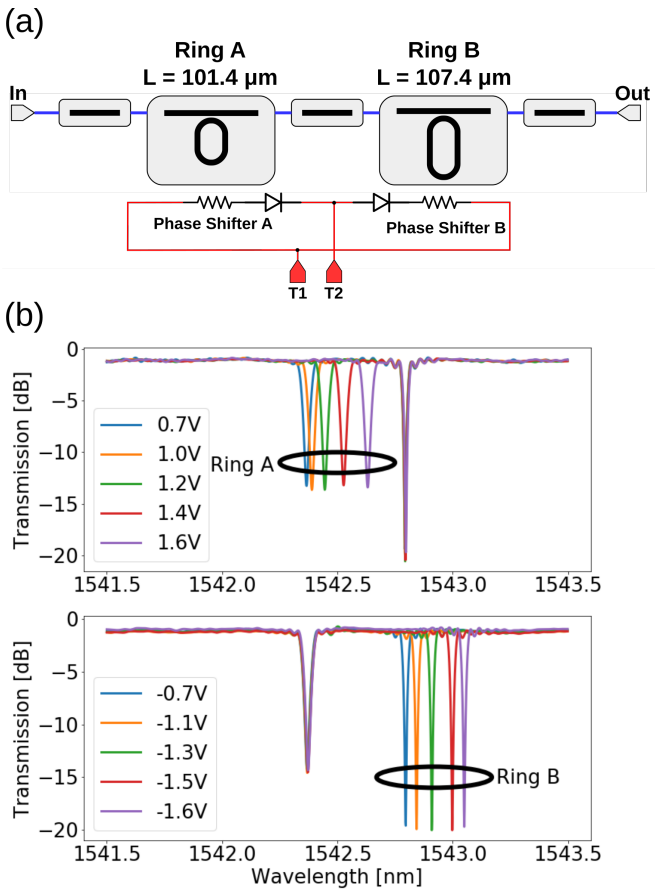

Figure 4.13: (a) Schematic representation of the fabricated test device containing two ring resonators with slightly different round-trip length. The purpose of this device is to be used to demonstrate the use of duobinary PWM signals to drive multiples heaters at the same time. Notice that both phase shifters are connected in parallel, but with opposite polarities for the diodes. (b)

To actuate on both heaters at the same time we can use a duobinary PWM signal (Fig. 4.14). The signal is analogous to a PWM signal, but divided in two parts in the time domain: the first half is a PWM signal with a positive polarity,

while the second half is an independent PWM signal, but with negative polarity. By individually controlling the duty cycle of the positive and negative cycle we control the average power in both the positive and the negative cycles of the signal.

If this signal is applied to a heater with integrated diode, the heater will see only the half of the signal that puts the diode in forward bias, while the remaining half of the signal is discarded. That means that for arrangements as the one in Fig. 4.13, each half of the duobinary PWM signal will be controlling one ring in the circuit. As in the case of a normal PWM signal, if the frequency of the driving signal is fast enough, the heater will only perceive the averaged power over time, and we can control two heaters at the same time with only one pair of contact pads.

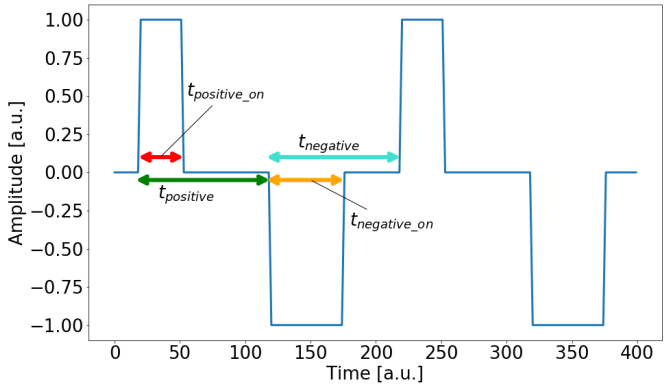

Figure 4.14: Representation of a duobinary PWM signal.

One important aspect that we have to consider here is that, as we are time-multiplexing the access to the heaters, each element will have, at most, 50% of the duty cycle available to perform its work, as the remaining half of the cycle is used by the second phase shifter. That means that a phase shifter designed to deliver $\pi\ rad$ phase shift at a voltage V will only induce $\pi/2\ rad$ phase shift when used in a duobinary arrangement if the same voltage level V is used. We can increase the power yield, and therefore the total induced phase shift, by operating the phase shift with a higher voltage level, but we have to keep in mind that we cannot go beyond the breakdown voltage of the diodes (see Section 2.2.4), as we rely on it to select which element is being actuated by the driving signal. Ultimately we decided to adopt a phase shifter with segmented heaters, with multiple heaters in parallel (see Section 2.2.3) as it increases to power output while operating at relative low voltage.

To validate our duobinary driving scheme we powered the circuit from Fig. 4.13(a) with a duobinary signal with $\pm 4\ V$ amplitude and frequency $f = 1\ MHz$. We

recorded the shift in the resonance of both rings while manipulating both positive and negative cycles of the duobinary PWM signal.

Fig. 4.15 shows a summary of the collected data. On the top two rows we show the duty cycle value of the positive half of the signal along with the measured spectrum shift in the resonance of $Ring\ B$. The bottom rows show the same data, but for $Ring\ A$ and the negative part of the duobinary signal. Notice that both heaters are being actuated at same time, but independently.

We can notice from the plot in Fig. 4.15 that there is a clear correlation between the spectrum shift of a particular ring and its correspondent duty cycle in the duobinary PWM signal. A change in the duty cycle of the positive part of the signal affects only the $Ring\ B$ while a change in the duty cycle of the negative part of the signal will result in a response of $Ring\ A$.

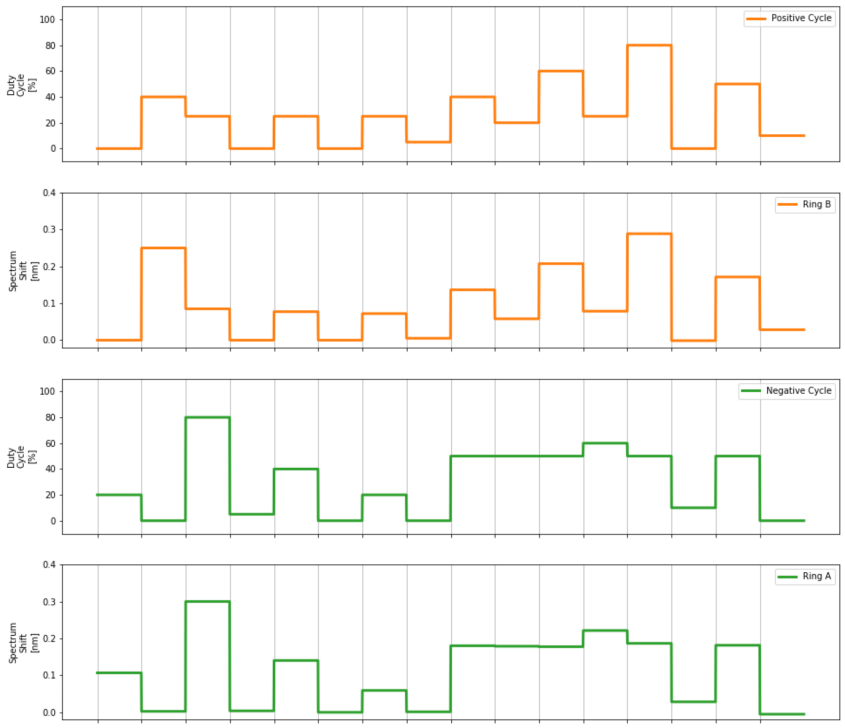

Figure 4.15: Shift in the resonance peak of the rings A and B in function of the positive and negative duty cycle values of the duobinary signal applied to the rings circuit.

From these results we conclude that it is possible to time-share the access to multiple thermo-optical phase shifters and drive multiple heaters with a single pair of contact pads. This is possible due to the very large time constant of the thermal phase shifters and the use of diode-loaded heaters to select the driving signal based

on its polarity.

4.4 Matrix Addressing[3]

We can further explore the time-multiplexing approach introduced earlier to drive a larger number of phase shifters using a small set of contact pads. In this section we are going to explain the foundations of matrix addressing and how to use it for driving silicon photonics circuits.

4.4.1 Rationale

To extend the multiplexing concept to larger circuits, and allow further exploration of time-sharing, it is possible to route the diode-based phase shifters in a matrix topology, grouping the heaters in sets of columns and rows, as shown in Fig. 4.16(a). In this arrangement we connect the anodes of the diode-heaters that are in a same row together, while the cathodes of the phase shifters that are in a same column are connected together. We call the rows of the matrix *control lines* and the columns *driving channels*.

To address one specific phase shifter in the matrix we have to set the voltage level at its correspondent control line at a low level (Gnd), while setting the voltage of its correspondent driving channel at high level ($V+$). That ensures that the selected phase shifter diode is forward biased. Because of this arrangement, the control lines acts as *enablers* in the circuit, and only a phase shifter that belongs to an enabled control line can be active. To guarantee that only the desired phase shifter is actuated when applying a signal to its correspondent driving channel, only one control line is enabled at a time, while the remaining control lines remain disabled. Notice that a row is enabled at low level (Gnd), and disabled at high level ($V+$)[4].

Once we enable a row in the matrix we can drive all the phase shifters in that row simultaneously, by powering their corresponding driving channels. To address a phase shifter in a different row we have to disable the current row and enable the new one. Once the next control line states are set, we use the driving channels to power the enabled phase shifters at the new row.

It is possible to implement time-sharing among the heaters by synchronizing the driving signal applied to the driving channel with the enabling of the control

[3] Part of this work was done in collaboration with Sibert Declercq, in the context of his thesis project.

[4] The circuit can be easily modified to be enabled at high level and disabled at low level by changing the polarity of the diodes. But this comes with the caveat that the driving signal will be reversed in polarity, as the diode will be in forward bias during the low level part of the driving signal. That means that a driving signal with 25% duty cycle would be seen by the phase shifter as a signal with 75% duty cycle (and vice-versa). For that reason we opt to illustrate the discussion with a circuit that is enabled with a low level signal.

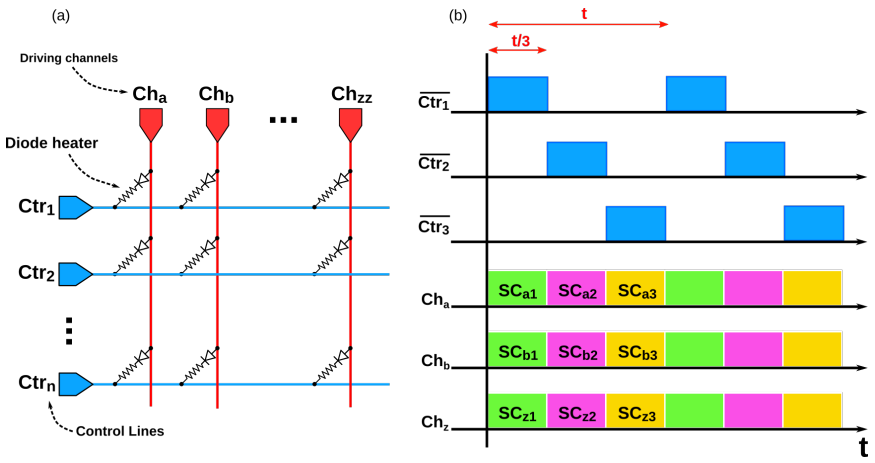

Figure 4.16: (a) Electric schematic of a matrix topology arrangement to drive multiple phase shifters with diode heaters. The rows are used as control lines, and only one control line is supposed to be active at the time. (b) Time diagram illustrating the synchronization between the control lines and the signal at the driving channel. In this example each channel Ch contains three subchannels, and each subchannel is synchronized with the actuation of one control line.

lines. Fig. 4.16(b) shows the time diagram of a circuit with three control lines and three channels. Notice that only one line is enabled at a time. That guarantees that only one phase shifter per channel will be addressed at a time. Now notice that a channel (e.g., Ch_a) is subdivided in three subchannels (SC_{a1}, SC_{a2}, and SC_{a3}), and each subchannel is synchronized with the enabling signal of one control line (SC_{a1} with Ctr_1, SC_{a2} with Ctr_2, and SC_{a3} with Ctr_3). This makes each phase shifter in the channel to be addressed only during the duration of its respective subchannel, allowing the driving signal to be time-shared to control three phase shifters. We can place many parallel channels (each with its own driving signal) and reuse the control lines to implement a $N \times M$ matrix-sized circuit, being N the number of control lines (rows) and M the number of channels (columns). This arrangement allows driving $N \times M$ phase shifters with $N + M$ contact pads (and digital power sources), as opposed to $N \cdot M$ contact pads and power sources needed if using traditional driving schemes.

Time-sharing means that each heater will be driven during the equivalent time of its correspondent subchannel. That means that, for a three-fold multiplexing (as illustrated in Fig. 4.16(b)), each phase shifter will be powered, at most, during one-third of the time, while the remaining period it stays idle. That's only possible if we rely on the large time-constant of the thermo-optical phase shifter to average-out the power in the phase shifter during the driving cycle. Therefore, our driving signal has to obey the specifications discussed in Section 4.3.1.

4.4.2 Subcircuit analysis

The matrix circuit can be divided in many identical subcircuits, each containing one driving channel and the necessary control lines to enable the phase shifters connected to the driving channel. The full circuit comprehends a collection of M subcircuits.

Fig. 4.17(a) shows an 1×16 multicast network implemented with 2×2 MZIs as tunable couplers (Fig. 4.17(d)). The optical power at the outputs of the circuit is determined by the coupling ratio of each MZI. The circuit is built with fifteen tunable couplers, and the phase shifters used to operate the circuits are connected in a 3×5 matrix topology (Fig. 4.17(b)), which requires eight contact pads (and power sources) to drive the sixteen phase shifters needed to operate the circuit.

As the matrix can be split in a set of M columns, one for each driving channel, we can operate each one of these sub-sets as an independent subcircuit as the one illustrated in Fig. 4.17(c). Each sub-circuit is formed by three tunable couplers, and are controlled by its designated driving channel.

To properly control the phase shifters arranged in a matrix topology we have to provide the enabling signals to control the matrix lines and, synchronized to that, the driving signals at the channels of the matrix circuit. The driving signal is assembled by concatenating the multiple subchannels that constitute the channel. Fig. 4.18(a) shows how the signal used to drive the subcircuit from Fig. 4.17(c) is constructed. The channel is divided in three subchannels, each corresponding to one of the three MZIs A, B, and C in the circuit. We use a PWM signal for driving the circuit, and each subchannel has it respective value for the duty cycle inside the subchannel. The signal of the three subchannels are then combined together to form the full driving signal.

As the signal is time-shared between three subchannels, and the MZI is only accessible during one-third of the time, the effective duty cycle seen by the MZI is the duty cycle of the subchannel divided by the total number of subchannels. That means that each MZI can be effectively driven by a PWM signal with a maximum duty cycle $D.C. = 100/3 = 33.3\%$. This property of time-sharing has to be taken in account when designing the heaters to be used in the phase shifter, and we will analyze these constraints in Section 4.4.2.1. Fig.4.18(c) shows the effective driving signal as seen by the heaters once they are properly addressed. The same process happens in parallel to all channels of the circuit.

4.4.2.1 Limitations and considerations

Time sharing actuation is only possible due to the very low time constant of the thermo-optical phase shifters, as we are driving the phase shifters with a non-constant signal. That means that the frequency of the enabling signal (used to select which row is enabled) has to satisfy the requirements imposed by reaction

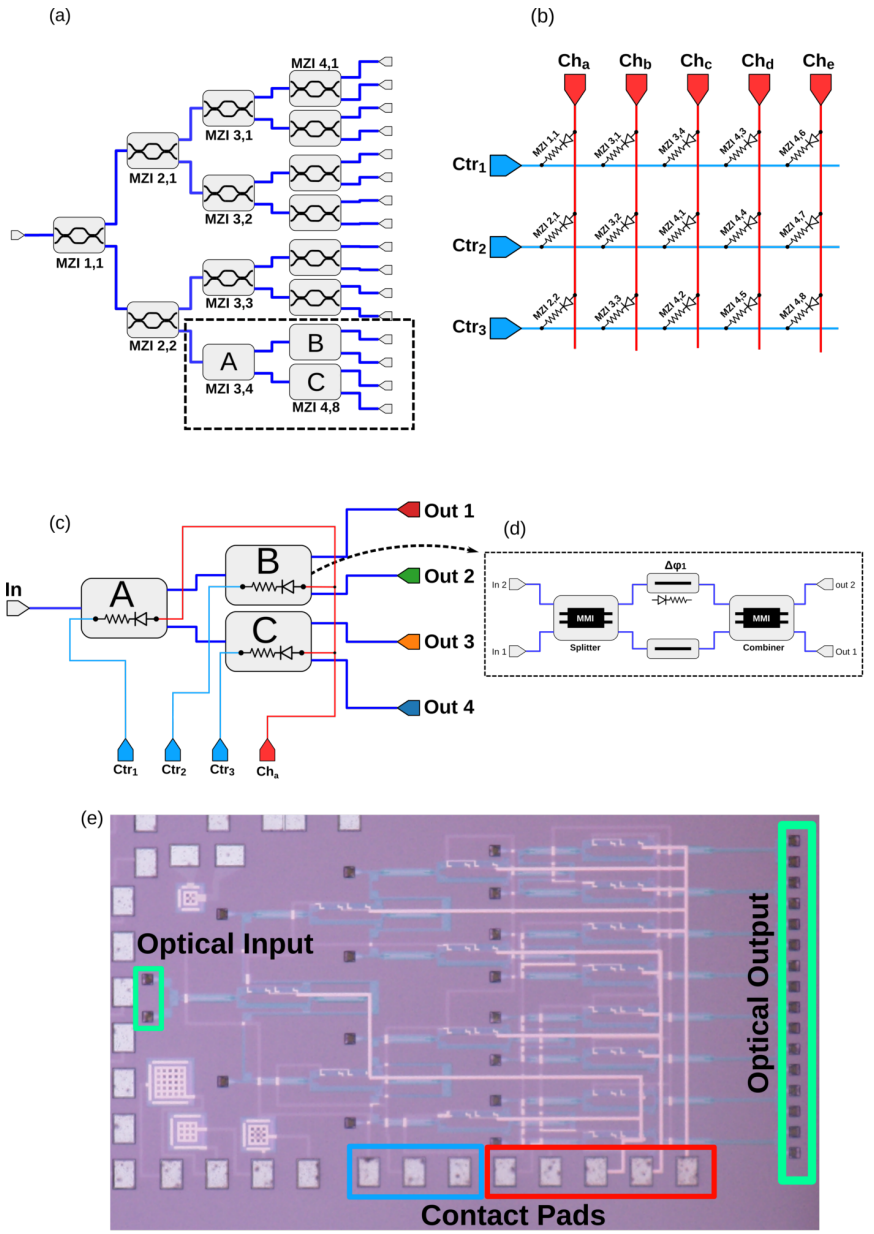

Figure 4.17: (a) A 1×16 *multicast network implemented with tunable couplers MZIs. (b) The schematic of the phase shifter of the circuit in a matrix addressing topology circuit. (c) Subcircuit from the multicast network that comprehends three MZIS (and its respective phase shifters). This subcircuit is arranged as one driving channel of the whole circuit. (d) The MZI used in the circuit. (e) Microscope picture of the fabricated* 1×16 *multicast network.*

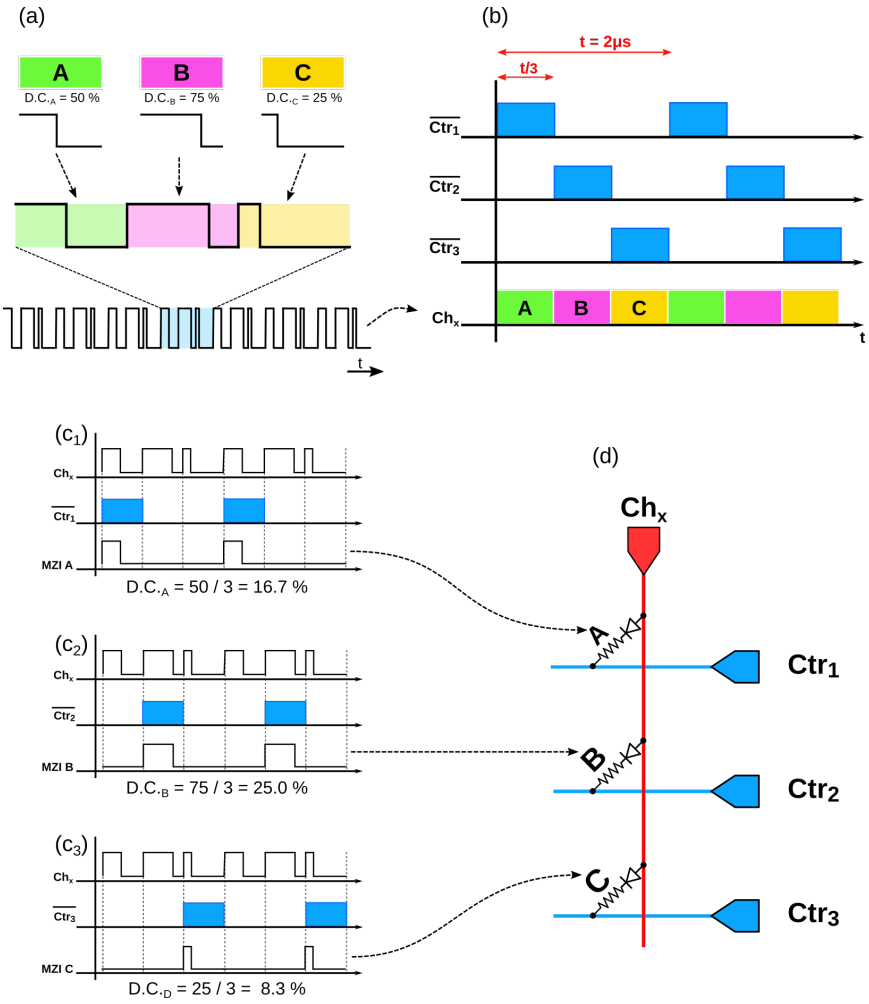

Figure 4.18: (a) Time-domain composition of the driving signal applied to channel Ch_x to drive the circuit. (b) Time diagram of the driving and control line signals. Notice that the subchannels A, B, and C are synchronized with their respective enablers signals in Ctr_1, Ctr_2, and Ctr_3, respectively. (c) Driving and control signals for each MZI. The diode heater can only be in forward bias when the control line is enabled (Gnd). The effective duty cycle applied to the MZI heater is the duty cycle of the subchannel divided by the number of subchannels. (d) Schematic representation of the subcircuit connections. The anodes of the diode heaters are connected to their respective control lines, while all cathodes are connected together to the driving channel.

time of the phase shifters, as discussed in Section 4.3.1. The same applies to the frequency of the PWM signal applied to the driving channels.

A second important characteristic of time-multiplexing access to the heaters is that only a fraction of the total cycle can be used by a phase shifter, as we can only enable one row at a time. For a matrix with three rows, as in the circuit in Fig. 4.17, each phase shifter in a given channel can be activated during one-third of the total time cycle at the most. That means that the phase shifter can yield at most 33% of the electrical power for a given voltage V of the PWM signal used to power it. To guarantee that this does not become a limiting factor we design the phase shifters to have a high power yield, allowing us to induce enough phase shift even for low duty cycle values.

In fact, the number of multiplexed elements in a same driving channel is directly dependent on the time constant of the phase shifters, the frequency of the driving signal and the power efficiency of the phase shifters. For multiplexed applications it is desired to have phase shifters that are slow enough, so low-frequency PWM signals can be used, avoiding the use of complex electronics for generating (and amplifying) high speed signals. At the same time it is desired to have phase shifter with high power efficiency, as an increase in the number of phase shifters sharing a driving channel leads to a reduction in the available time fraction that each phase shifter in this channel can be driven.

Fig. 4.17(e) shows a microscope picture of the fabricated 1×16 multicast network. The phase shifter used in this device is designed to operate in the voltage range of $\pm 7\ V$, and it is designed to induce a maximum phase shift $\Delta\phi = 6\pi\ rad$ at $7\ V$. This gives an effective phase shift $\Delta\phi = 2\pi$ at duty cycle $D.C. = 33.3\%$, for a signal amplitude of $7\ V$, which makes this phase shifter fit to be used in a time-sharing arrangement. The summary of the phase shifter parameters used in the circuit are listed in Table 4.1.

Resistance:	$410\ \Omega$
Efficiency:	$20\ mW/\pi\ rad$
Operating range:	$\pm 7\ V$
τ:	$80\ \mu s$

Table 4.1: Summary of the simulation parameters used in the phase shifter model.

4.4.2.2 Subcircuit simulation

We simulated the sub-circuit from Fig. 4.17(c) for different combinations of driving signals to modify the power distribution at the outputs of the circuit. The simulation was realized using a time-domain circuit simulation integrated with the design framework IPKISS [15, 16].

To build the simulation model we create the circuit from Fig. 4.17(c) an S-matrix based model for the MMI couplers and the waveguides to build the tunable coupler MZI. The phase shifter model was implemented using the parameters obtained from the characterization of the fabricated device. The summary of the phase shifter parameters can be found in Table 4.1.

Initially we simulated one isolated tunable coupler MZI (Fig. 4.17(d)) using the time-domain simulation tool. The device is designed to be a normal-cross coupler (the device stays in cross-state when the phase shifter is unpowered), and we measured its transmission between the ports In_1 and Out_2 (cross-transmission). Fig. 4.19(a) shows the transmission of the device for a pulse driving signal. The amplitude of the driving signal is set to switch the transmission of the device from 100% to 0%. As we populated the phase shifter model with the value for the time constant τ obtained from an experimental characterization of the device, we obtained a transient response in simulation equivalent to the one measured discussed in Section4.3.1. This indicates that we have an accurate simulation of the time-domain behavior of the phase shifter.

Following that, we simulated the same device, under the same conditions, but now using a PWM signal with amplitude of $7\ V$ and duty cycle $D.C. = 16.7\%$. this value of the duty cycle is set to induce a phase shift $\Delta\phi = \pi\ rad$, making the tunable coupler switches from cross-state to bar-state. Fig. 4.19 shows the PWM driving signal applied to the phase shifter and the transmission of the device over time. Notice that the device has an initial transition period at the beginning of the simulation. That exist because we are in fact switching the device from cross-state to bar-state. The transient time obeys the same time constant limits set by the thermo-optical constant of the phase shifter, and tells us what is the maximum switch time we can accomplish with this tunable coupler, even when operating with digital driving signal.

Fig. 4.19 shows the transmission of the MZI for different values of duty cycle. This shows that the device can be operated using a PWM signal, and that a duty cycle ranging from 0% to 16.7% is sufficient to operate the MZI as a tunable coupler, as it demand a maximum phase shift operating range of $\Delta\phi = \pi\ rad$ for a complete switch. This indicates that this tunable coupler, can be used in a matrix circuit with up to six subchannels (as $100/16.7 = 6$).

After validating the simulation on a single MZI, we simulate the subcircuit illustrated in Fig. 4.17(c) for different values of duty cycle $D.C._A$, $D.C._B$, and $D.C._C$ for driving the MZIs A, B, and C respectively. The schematic of the electrical circuit connecting the phase shifter of the three tunable couplers can be seen in Fig. 4.18(d). As the phase shifters are connected in a matrix topology and the driving signal is time-shared among the phase shifters, the effective duty cycle as seen by the MZIs phase shifters is divided by the number of heaters in the driving channel, as illustrated in Fig. 4.18(c). We recorded the power at the four

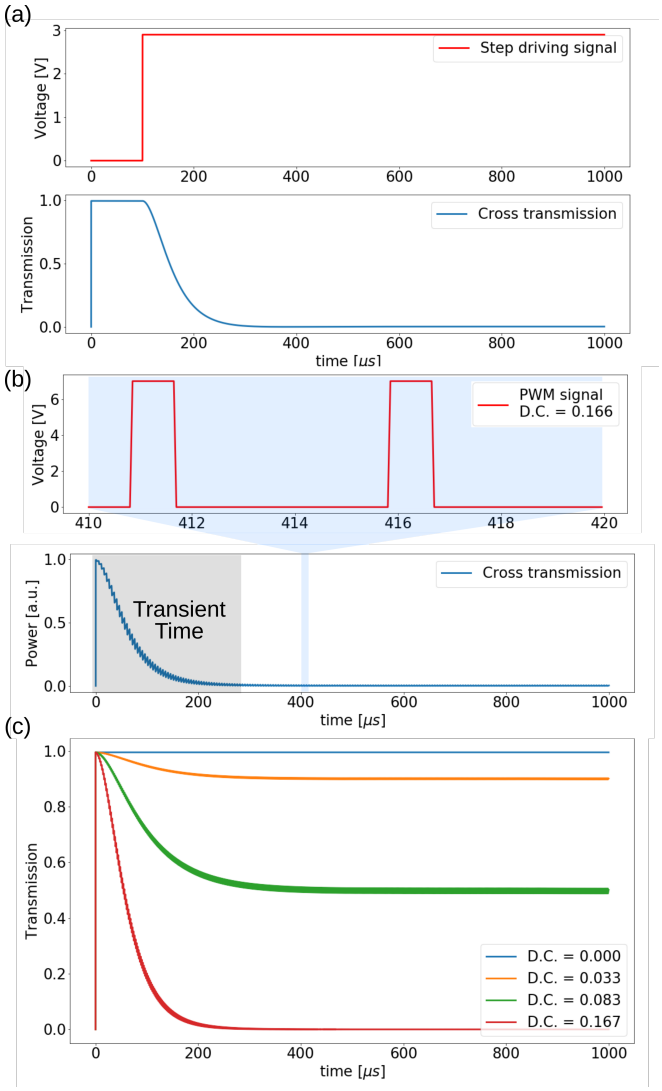

Figure 4.19: (a) Simulated transmission of a MZI for a step driving signal for a phase shifter with $\tau = 80\ \mu s$. (b) Simulation of the same MZI, but for a PWM driving signal. The frequency of the PWM signal is $f = 500\ KHz$. The transient time at the beginning of the simulation is due to the change of state of the MZI, as it starts with 100% transmission and the PWM driving signal switches it to 0% transmission. (c) Transmission of the MZI for PWM driving signal with different duty cycles.

outputs of the circuit for different combinations of duty cycle values.

Fig. 4.20 shows the circuit configured to route all the light to one output of the circuit (top two rows) and to split the light equally among two arbitrary outputs (bottom rows). Fig. 4.21 shows in the first plot a configuration that splits the light equally among all the outputs of the circuit. Following we show a number of different combination of parameters for the duty cycle values, resulting in different configurations of power split among the outputs of the multicast network. This simulation shows that we can use a matrix addressing topology to drive multiple phase shifters by sharing the same driving signal. The subcircuit shown in Fig. 4.17(c) can be expanded into the full version (Fig. 4.17(a,b)) by including new channels and reusing the same control lines. From the simulation results we conclude that it is possible to use this technique to enable the actuation of very large photonics circuits with fewer contact pads and fewer voltage sources. This is essential to ensure scalability of complex programmable photonics circuits.

4.5 Summary

In this chapter we introduced a number of techniques used to improve the driving of thermo-optical phase shifters in silicon photonics circuits. We discussed the impact of the parasitic resistances in the circuit and how the use of current-based driving can relief the issues caused by them. Following we introduced the digital driving concept, which uses a PWM signal to drive a phase shifter, taking advantage of the high time constant of thermo-optical phase shifters ($\tau \approx 80\ \mu s$). The use of digital signal has advantages such as the simplification of the power source (as we can use a fixed-voltage source instead of a variable one) and the increase in the linear response of the phase shifter, as the induced power grows linear to the duty cycle of the signal.

We expanded the use of PWM signal to implement multiplexed control, where we use one set of contact pads to drive multiple phase shifters using a duobinary PWM signal. Finally we extended the concept to a matrix arrangement that enables the driving of $N \cdot M$ phase shifter with only $N + M$ bondpads and power sources. This is, again, only possible due to the use of time-multiplexing in the driving signal, thanks to the very high time constant of the thermo-optical phase shifter.

In the next chapter we are going to discuss how to perform optical monitoring (power and phase) in photonics circuits, and how to use this information, combined with the driving techniques introduced in this chapter, to implement a closed feedback loop to control photonics integrated circuits.

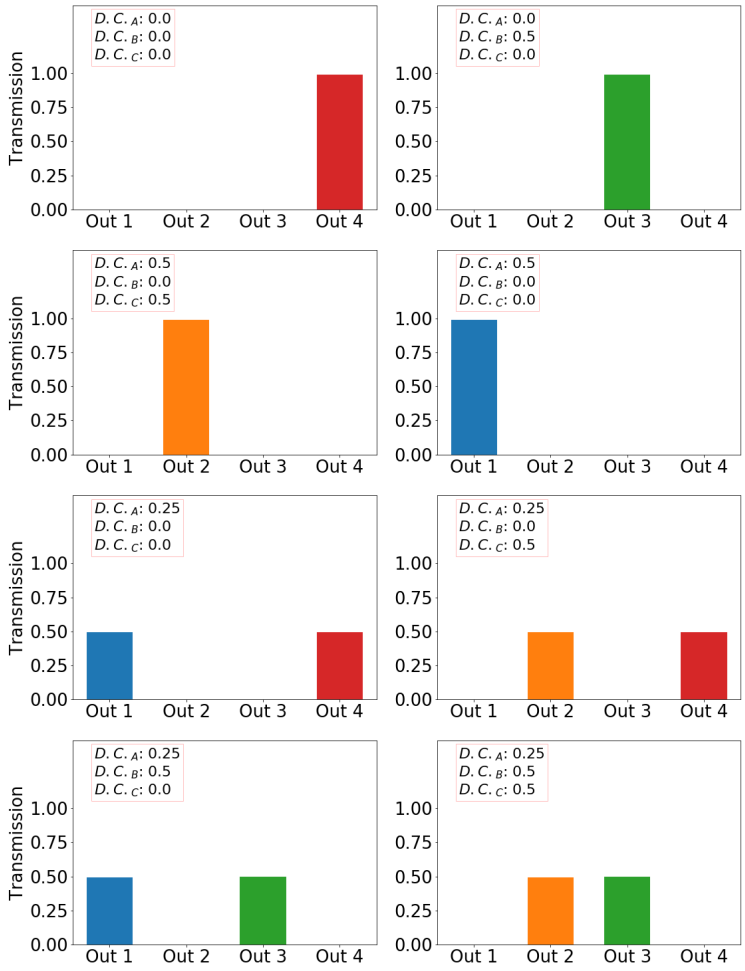

Figure 4.20: Simulated output of the 1×4 *broadcast network for different combinations of duty cycle values for MZIs* A*,* B*, and* C*. Each combination sets the circuit to a distinct configuration.*

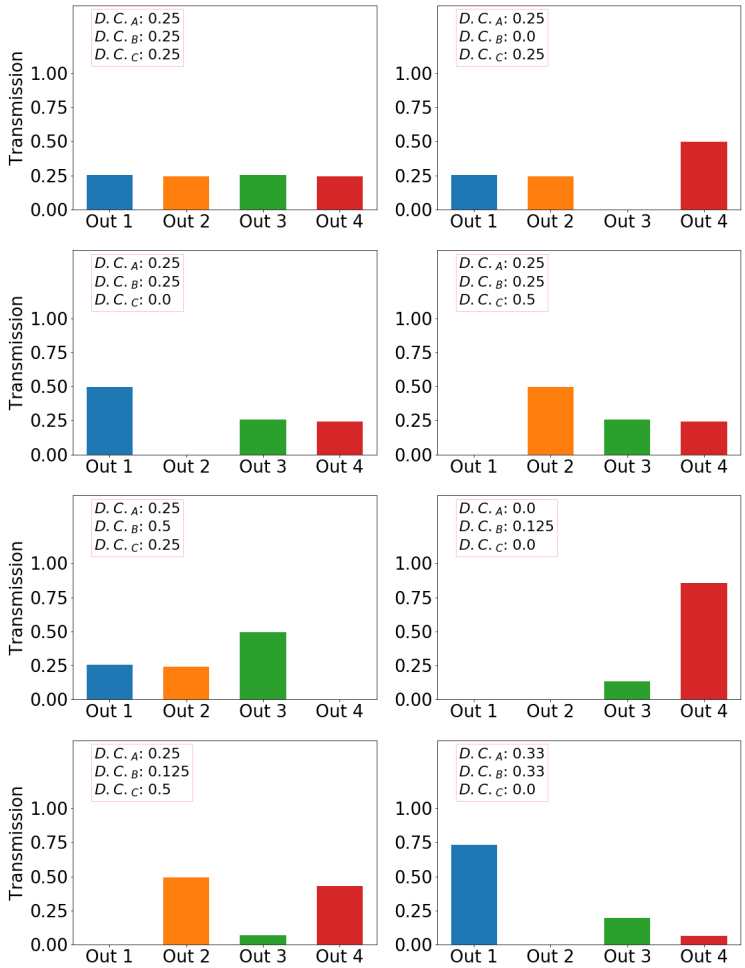

Figure 4.21: simulated output of the 1×4 *broadcast network for different combinations of duty cycle values for MZIs* A*,* B*, and* C*. Each combination sets the circuit to a distinct configuration.*

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5

Monitoring and Control

In the previous chapter we focused on the techniques developed for driving thermo-optical phase shifters and the components implemented using it. As result we developed techniques that make use of digital signal driving to improve the linearity of the phase-shifter response in function of the driving variable, as well as reducing the number of voltage source and bondpads needed to drive the circuit.

In this chapter we are going to focus on the implementation of active control on photonics components used in programmable circuits, with emphasis on controlling the tunable couplers introduced in Chapter 3. We introduce a control scheme (Fig. 5.1) that implements a closed feedback loop, used to monitor the behavior of the circuit and control the driving signal applied to the photonics components.

We start this chapter introducing the building blocks used to implement power monitoring in the optical circuit and we detail the implementation of a simple optical tap, a component used as a probe to measure the optical power in a waveguide. We then introduce a method to measure phase difference using an integrated interferometer and balanced photodiodes. Following we introduce the control techniques used to operate the tunable couplers used in our programmable circuits, with emphasis on common-mode driving, which faces bigger challenges due to the non-linearity of the phase shifters. We conclude this chapter by introducing the control loop used to optimize the $2 \times 2 \times 2$ tunable coupler.

It is worth mentioning that most of these control techniques were developed before the introduction of digital driving in our work, and that DC driving was used as the driving method of choice. Nevertheless, such techniques can be implemented using digital driving schemes, as they are agnostic to the driving techniques.

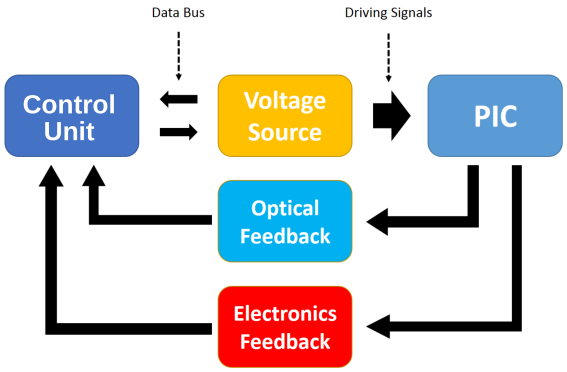

Figure 5.1: Control loop used to operate the optical system.

5.1 Power monitors

As the PICs evolve from device-scale applications to complex circuits, a larger number of control and monitoring routines are necessary to ensure that the photonics circuit works properly. Circuit monitoring and feedback control operations are required to compensate for fabrication imperfections and variability, temperature fluctuations, and parasitic effects [1], especially when many photonic devices are aggregated into complex PICs. This need is even more pronounced in programmable circuits, where the functionality of the circuit emerges from its tunability. Optical power monitors are an essential building block for large scale photonics circuits, and especially in programmable circuits, for the implementation of feedback control loops in the circuit.

Advances on integrated optical power monitoring includes the development of components such as the *In-Resonator Photoconductive Heaters* (IRPHs) [2, 3] by *University of British Columbia*, which relies on measurement of the photoconductivity of the heater used tune the optical component, and the *Contactless Integrated Photonic Probe* (CLIPP) [4, 5] by *Polytechnic University of Milan*, which works by measuring the same change in the electric conductance of the waveguide core in function of the optical power, but uses an RF signal to access the waveguide via capacitive electrodes applied on top of the waveguide, offering the possibility of implementation on passive optical chips, as its doesn't requires doped silicon, and the electrodes can be be implemented via postprocessing through simple metal deposition on the optical chip. One drawback of the CLIPP device is its need of specialized RF electronics, which can increase the complexity of the read-out circuitry needed to operate the PIC.

In this work we implement power monitoring using a tap-based optical probe, where we tap a fraction of light from a waveguide to infer its total optical power.

This approach requires the implementation of low-loss and low-reflection optical taps to be placed in the circuit in strategic locations and, although having some drawbacks (such as slightly increasing the optical losses in the circuit, and increasing complexity to the circuit design) allows the implementation of power monitoring across different platforms (such as passive PICs and iSiPP50G).

Optical taps allow a more deep analyses of the light, as they can be combined with other elements (e.g., spectrometers) to perform wavelength-dependent measurements. Also power taps allow to discriminate between forward and backward propagation, which is not possible with CLIPPs and IRPHs. Optical taps also allow the use of alternative power monitoring schemes, such as infrared camera imaging, which can be used to for circuit development as tests and experiments without committing with a complete electronics circuitry. In this section we discuss the development of the optical taps used in our circuits for readout, as well as its use for off-chip monitoring (e.g., using an infrared camera) and on-chip monitoring (e.g., using photodetectors).

5.1.1 Optical taps

To monitor the optical power in a photonic circuit using a simple optical tap we couple out a small fraction of light from a waveguide and measure its power. It is possible to infer the total optical power in the waveguide if the coupling coefficient of the optical tap is accurately know, but for most applications where we only need to either maximize or minimize the optical power at some point in the circuit (e.g., to operate a tunable coupler as an optical switch) we don't need to know the absolute value of optical power in the monitored waveguide.

Ideally the optical tap couples as little light as possible from the waveguide, just enough to make detection possible, to avoid introducing excessive loss in the circuit. An optical tap can be constructed using a directional coupler with very low coupling coefficient κ (Fig. 5.2). The light captured by the power tap is then directed either to a on-chip photodetector or to a grating coupler, to be used in off-chip monitoring.

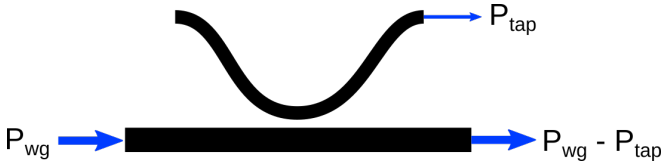

Figure 5.2: Directional coupler used as an optical tap

To define the coupling coefficient of the optical tap we need to observe two parameters: the power budget of the circuit to be monitored and the sensitivity of the detector used to monitor the output of the power tap. The sensitivity of the

detector tells us the minimum amount of light that needs to be used to perform a proper measurement, while the power budget of the circuit dictates the maximum power that can be tapped off from the circuit without affecting its operation.

5.1.1.1 Design and optimization of optical taps

To choose the coupling coefficient κ of our optical tap we start from the maximum expected extra loss that can be introduced by the optical tap. The extra loss introduced in the circuit by an optical tap can be expressed by:

$$T_{loss} = 10 \cdot \log\left(1 - \kappa\right) \tag{5.1}$$

Therefore, if we want a power tap to introduce an extra loss in the circuit of $T_{loss} = -0.1dB$, we can calculate back the coupling coefficient $kappa$ by rearranging Eq. 5.1:

$$\kappa = 1 - 10^{-0.01/10} = 0.0228 \tag{5.2}$$

This gives us a coupling coefficient $\kappa = 0.0228$ (or 2.28%).

Next, we calculate what is the minimum optical power that our photodetector (for on-chip monitoring) or our power meter (for off-chip monitoring) can measure. A typical integrated photodetector has a dark current value in the order of $I_{dark} = 10\ nA$ and a responsivity in the order of $R_{esp} = 0.5\ A/W$ [6]. We can calculate its operational floor (as in the optical power whose photodetector response is equal to its dark current) from:

$$P_{dark} = \frac{I_{dark}}{R_{esp}} = \frac{10\ [nA]}{0.5\ [A/W]} = 20\ nW = -47.0\ dBm \tag{5.3}$$

This is the minimum optical power that has to be delivered to the photodetector in order to realize any meaningful measurement.

Finally, with the information obtained from Eq. 5.3 and Eq. 5.2 we can calculate the minimum optical power P_{wg} in the waveguide that can be detected by the photodetector in our optical tap. From the point of view of the photodetector, the power P_{tap} is given by:

$$P_{tap} = P_{wg} \cdot \kappa \tag{5.4}$$

Therefore, for $P_{tap} = P_{dark}$ (minimum detectable power), we have:

$$P_{wg} = \frac{P_{dark}}{\kappa} = -30.6\ dBm \tag{5.5}$$

which gives us the minimum detectable power at the waveguide for an optical tap with $\kappa = 0.0228$. We use this set of parameters (summarized in Table 5.1) as our input for the directional coupler design.

T_{loss}	$-0.1\ dB$
κ:	0.0228
P_{dark}:	$-47.0\ dBm$
Minimum P_{wg}	$-30.6\ dBm$

Table 5.1: Summary of the input design parameters for the optical tap.

We designed the optical power tap used in this work to have a coupling ratio $\kappa = 0.02$, to reduce further more the impact of the introduced loss in the circuit as we intend to use multiple optical taps per circuit. The new theoretical extra loss introduced per optical tap in the circuit is $T_{loss} = -0.088\ dB$. Although this figure is relatively low, we have to account for extra losses and reflections introduced by imperfection in the fabrication of the device, for instance. Because of that we limit its use to parts of the circuit where monitoring is indispensable.

We designed our optical tap using the directional coupler method discussed earlier in Chapter 3. In our design we use a directional coupler with asymmetric bends to avoid introducing bends in the circuit waveguide (Fig. 5.3). To reduce reflections and back-coupling problems we use a large adiabatic angle ($20°$) to implement the bend of the circuit. Table 5.2 has a summary of the parameters used to implement the 2% optical tap.

Bend radius:	$5\ \mu m$
Straight section:	$0.8\ \mu m$
Gap:	$0.25\ \mu m$
Adiabatic angle:	$20°$

Table 5.2: Summary of the design parameters of the 2% optical tap.

We simulated the optical tap using the FDTD method (Fig. 5.3). The simulation indicated a transmission of 97.88% with low back-reflection ($< 0.01\%$). Fig. 5.4 shows a microscope figure of a fabricated power tap with grating couplers for off-chip monitoring. The device is bidirectional (hence the two grating couplers), allowing to monitor the light traveling in both directions through the waveguide.

5.1.2 Experimental results and wavelength dependency

Once the light is tapped out of the circuit we can monitor its power either by routing it to a photodetector in the photonics chip (on-chip monitoring) or using an external detection method (off-chip monitoring), such as an external power meter or an infrared camera.

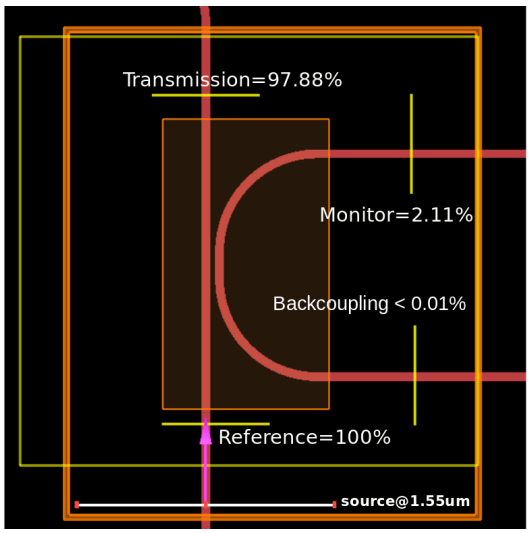

Figure 5.3: Result of the FDTD simulation of the optical tap designed for a 2% coupling ratio. Notice that the coupler presents very low reflection level.

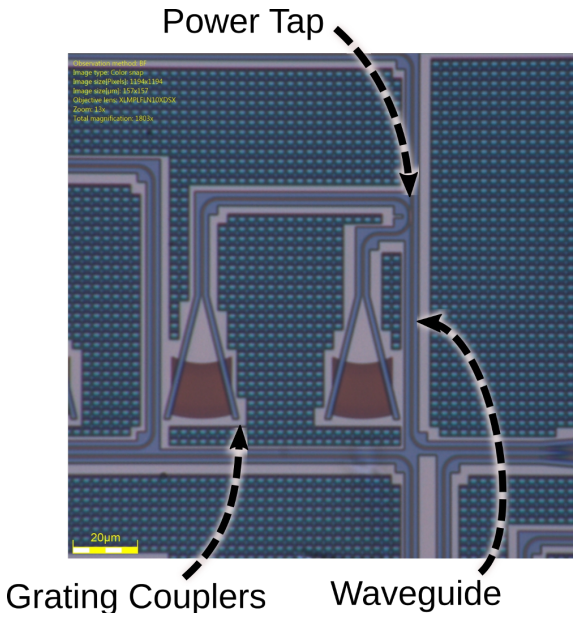

Figure 5.4: Fabricated power tap with grating couplers.

5.1.3 On-chip monitoring

On-chip monitoring is done when we integrate photodetectors directly in the PIC and use it to perform the power readout in the circuit. The photodetectors can be directly integrated in the PIC fabrication when the technology allows it (such as the iSiPP50G platform from imec) or can be added by postprocessing a passive chip, using techniques such as transfer printing [7].

Fig. 5.5 shows the GDSII layout of a $2 \times 2 \times 2$ tunable coupler with power tap monitors in its ports. The power taps were added to allow the optimization of the component via a closed feedback loop (as we will show in Section 5.3.2), but with proper calibration of the response of the power tap we can infer the absolute power at the output of the circuit using the response of the photodetector.

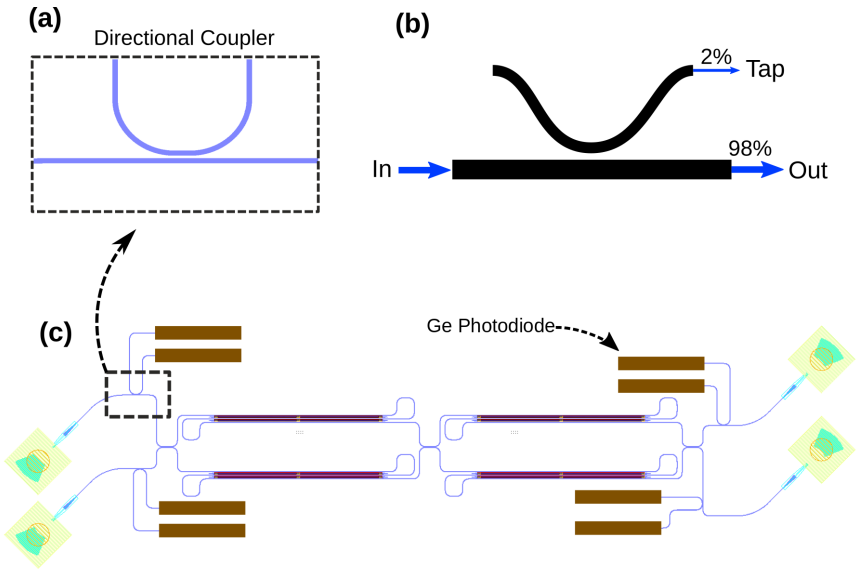

Figure 5.5: (a) Directional coupler used as an optical tap (b) Basic concept of an optical tap implemented with a directional coupler. (c) GDSII layout of a $2 \times 2 \times 2$ tunable coupler with integrated taps for monitoring the power in its ports. Notice that the taps are bidirectional, so it is possible to use it to monitor both the forwarding optical signal as well as reflections.

To validate the power tap with on-chip monitor we compared the response of the $2 \times 2 \times 2$ tunable coupler from Fig. 5.5(c) using a fiber-to-fiber measurement to the readout of the on-chip photodetector attached to the power tap. Fig. 5.6(a) shows the response of the device using a fiber-to-fiber measurement, while Fig. 5.6(b) shows the same measurement using a power tap with on-chip photodetector. The experiment was done using a monochromatic optical source at $\lambda = 1.616\ \mu m$.

A first thing we notice is a good qualitative agreement between the two measurements. Both read-outs are consistent regarding the position of peaks and valleys, indicating that both the optical tap with on-chip photodetector and the fiber-to-fiber measurement have a fair representation of the transmission power at the output of the device.

To verify the quantitative agreement between the two measurements we calculate the difference between the two read-outs. This is done by first normalizing the two read-out (in linear scale) and calculating the difference between the two results. Fig. 5.6(c) shows the distribution of the difference between the normalized response of both measurements, in linear scale. This shows us that, for most of the measurement, the difference between the normalized on-chip and the fiber-to-fiber results stayed below 2%. We will discuss how to use the on-chip photodetector to implement a closed feedback loop between the readout of the tunable coupler and its control algorithm in Section 5.3.2.

5.1.4 Off-chip monitoring

Off-chip monitoring can be performed by connecting the output of the power tap to a grating coupler and monitoring the power at the grating coupler using a power meter or infrared camera. This approach allows us to perform power monitoring in passive chips, where an integrated photodetector is not an option. When using off-chip monitoring with external power meters we can have an accurate indication of the power at the monitored grating coupler and, assuming that the grating coupler and the optical tap are accurately characterized, we can infer the optical power in the monitored waveguide.

However, multiple applications in programmable circuits can be performed using only relative power measurement [2, 8, 9]. For this, the associated control loop uses the readout of the power monitor to either maximize or minimize the power in the monitored waveguide, regardless its absolute value. Programmable circuits that operate based on this principle include the self-adapting beam coupler implemented using the 4×4-port universal linear circuit [10] and the $2 \times 2 \times 2$ tunable coupler (Section 5.3.2).

5.1.4.1 Off-chip monitoring using IR camera imaging

Infrared cameras can be used to monitor the power at multiple grating couplers at same time. Fig. 5.7(a) shows the schematic of the set-up arrangement to use an IR camera to monitor the power at the grating coupler outputs. The frame captured by the camera can be divided in arbitrary regions (sub-frame), each associated to one grating coupler in the circuit (Fig. 5.7(b)). We can extract the relative power at a grating coupler by integrating the image intensity of its associated sub-frame.

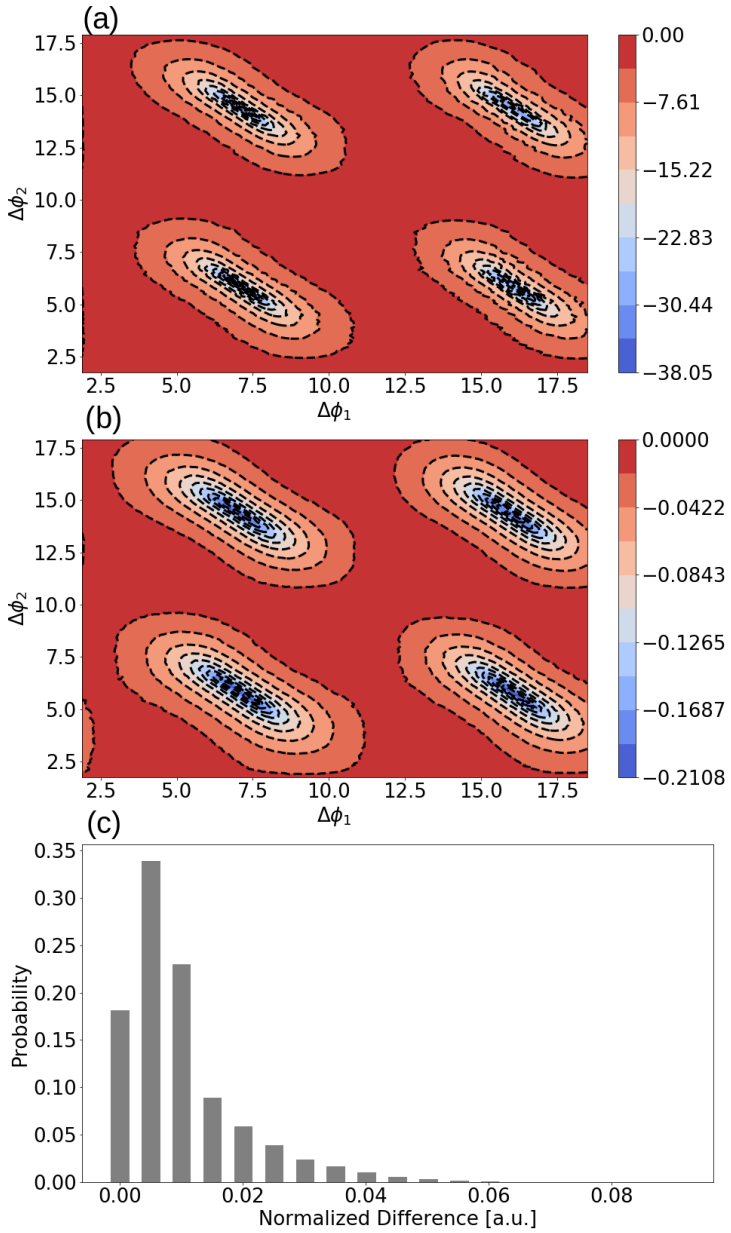

Figure 5.6: (a) $2 \times 2 \times 2$ tunable coupler transmission in function of $\Delta\phi_1$ and $\Delta\phi_2$, measured using a fiber-to-fiber set-up for a wavelength of $\lambda = 1.616\ \mu m$, expressed in dBm. (b) Same measurement, but using a power tap with on-chip photodetector, expressed by the photocurrent in the photodetector. (c) Distribution of the difference between the normalized measurements, in linear scale.

Fig. 5.7(c) shows a typical set-up used to monitor a large number of optical taps using an infrared camera mounted on top of the optical circuit.

Fig. 5.8(a) shows the GDSII layout of a circuit that uses multiple optical taps connected to grating couplers to monitor the power in the circuit. This circuit was designed to be monitored using a camera imaging set-up, so we group the grating couplers together to fit them in a single camera frame. As the optical taps are bidirectional, we have two grating couplers per tap, one monitoring the forward transmission and one monitoring the backward transmission. Fig. 5.8(b) shows the grating couplers as seem from the infrared camera. Notice how the brightness of detectors $D11$ and $D21$ changes between the frames, indicating the change in the power monitored by the optical taps. We implemented our circuit using standard grating couplers for off-chip monitoring, but dedicated grating couplers of smaller dimensions could be used to fit more monitors in a smaller area, allowing the monitoring of more power taps using the same camera frame.

Off-chip monitoring using camera imaging has the advantage of enabling multiple optical taps monitoring at a same time, limited only by the size of the imaging frame of the camera. However, camera monitoring is used only during the development phase of the PIC, or for tests and experiments. Once the chip and its systems has been fully developed it is necessary to migrate to a different approach to monitor the power taps. For passive chips, this can be done by postprocessing the PIC to add photodetectors. This can be done using several integration techniques, such as transfer printing [7].

5.1.4.2 Absolute power measurement using IR camera

Fig. 5.9 shows the output power from a MZI in function of the voltage applied to its phase shifter, measured by a power meter (via fiber-coupling) and via camera imaging. We notice that the two results have a qualitative agreement (peaks and valleys match), but the two readouts have slight different responses. That indicates that, if we want to measure the actual power emitted by the grating coupler we need to guarantee that the function that correlates the intensity read by the camera sensor and the optical power is properly calibrated. This calibration process is not necessary when using the camera imaging system to measure relative power.

5.2 Phase monitoring

Several applications in PICs requires not only power, but also phase control. We cannot measure the absolute phase of an optical signal, but it is possible to extract the relative phase between two monochromatic optical signals.

A *phase difference monitor* (PDM) is a on-chip component that can be used to measure the phase difference between two optical signals of same wavelength in

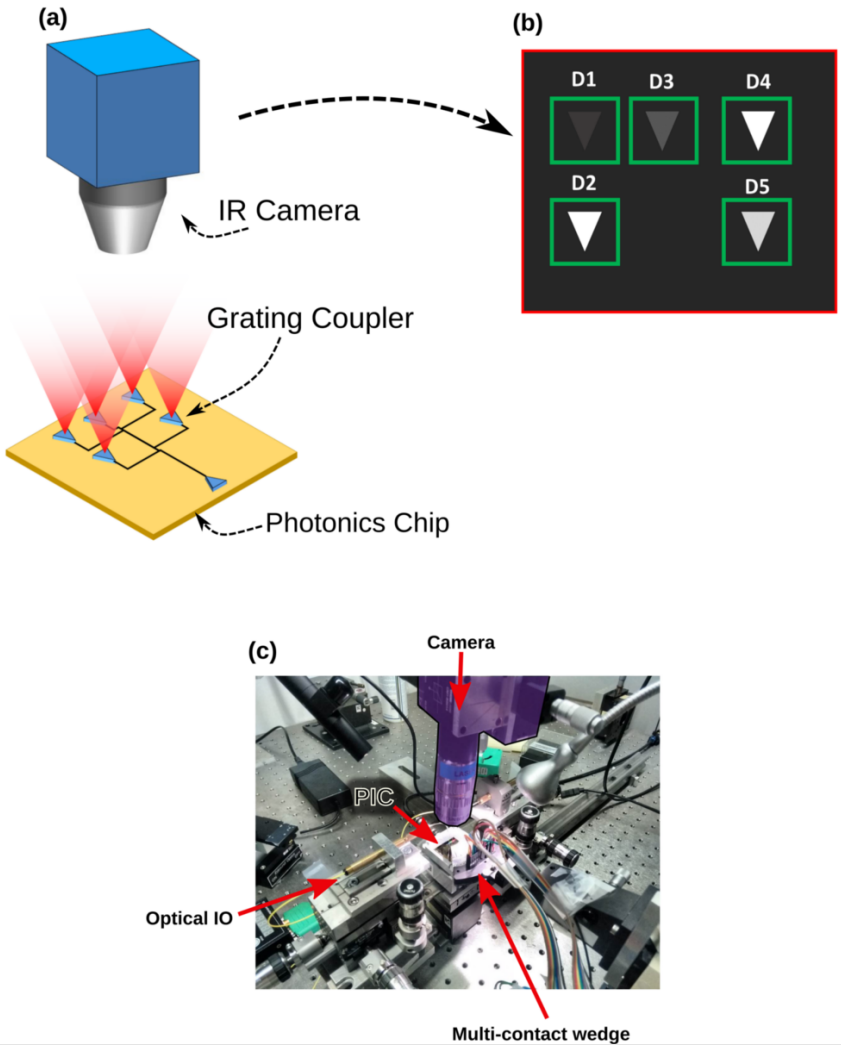

Figure 5.7: (a) Schematic of the measurement setup. (b) The grating couplers as seen by the camera. (c) Measurement set-up used to characterize a PIC using off-chip camera monitoring. The infrared camera is mounted on top of the optical chip and has a frame size sufficient to monitor a matrix of up to 5×5 *grating couplers.*

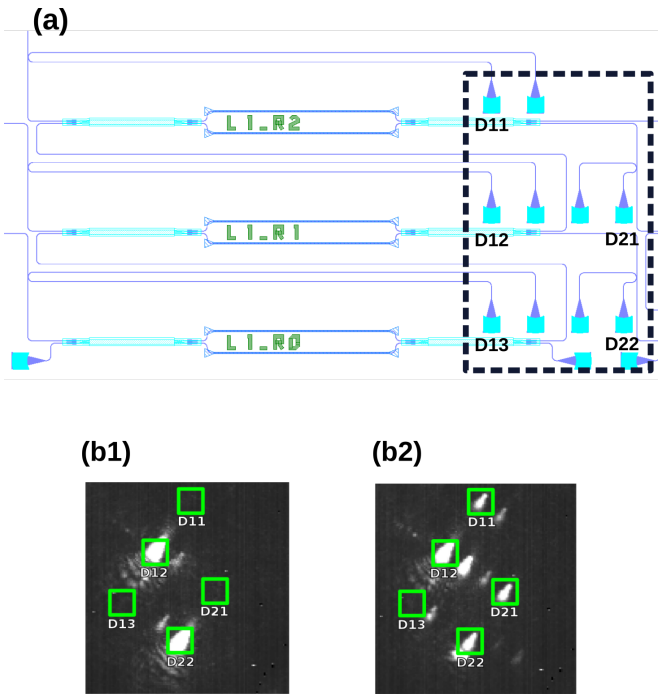

Figure 5.8: (a) GDSII layout of a circuit designed with optical taps for off-chip camera monitoring. (b) Image obtained from the infrared camera during an experiment. Notice the change of brightness in detectors $D11$ and $D21$.

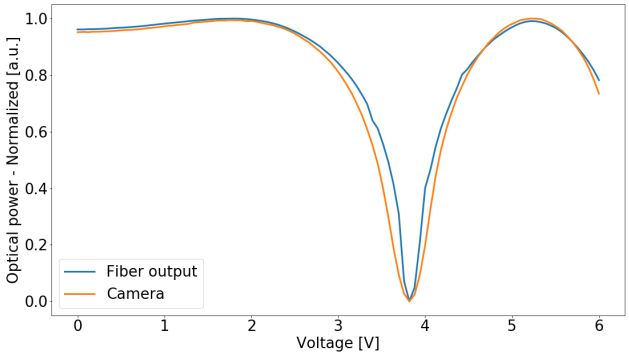

Figure 5.9: Normalized response of the transmission of a MZI in function of the voltage applied to one of its phase shifters. The same measurement was realized using a fiber-to-fiber approach and a camera imaging approach. The use of camera imaging for absolute power measurement requires a calibration step, which is not necessary when using this method for maximizing/minimizing the power at the monitor.

the circuit. Fig 5.10 shows the basic concept of a tap-based PDM. The optical taps collect the light from the waveguides and send them to the PDM device for phase comparison.

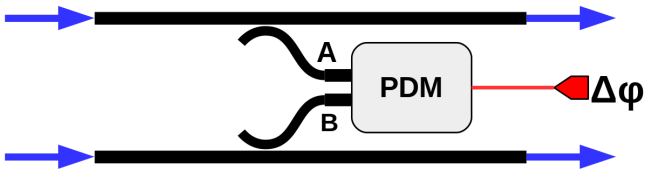

Figure 5.10: Basic concept of a phase difference monitor. The device use two optical taps to tap-out a fraction of light from the waveguides and measure the phase difference between the signals.

5.2.1 Rationale

We can use an interferometer device, such as an MMI, to extract the phase difference between two optical signals. Fig. 5.11 shows a phase difference monitor implemented with a 2×2 MMI which acts as a $50/50$ beam splitter and a pair of *balanced photodiodes* (BPD), to convert the phase difference into an electrical signal.

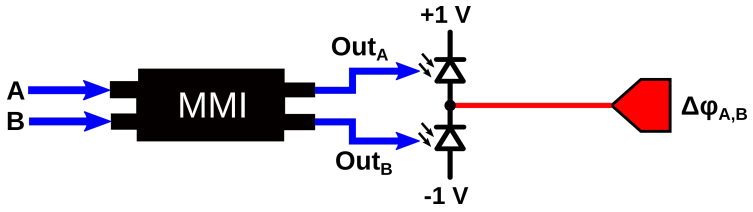

Figure 5.11: The phase difference monitor with balanced photodiodes. This circuit uses an MMI as an interferometer to extract the phase difference between points A and B. The output of the MMI excites the photodiodes of the circuit, which translates into a signal output in the circuit that correlates with the phase difference between points A and B.

The transfer function of an ideal 2×2 MMI is given by:

$$T_{MMI} = \begin{bmatrix} j \cdot \sqrt{2}/2 & \sqrt{2}/2 \\ \sqrt{2}/2 & j \cdot \sqrt{2}/2 \end{bmatrix} \tag{5.6}$$

The inputs A and B, as illustrate in Fig. 5.11, can be described as:

$$\begin{bmatrix} A \\ B \end{bmatrix} = \begin{bmatrix} a \cdot e^{-j\phi_a} \\ b \cdot e^{-j\phi_b} \end{bmatrix} \tag{5.7}$$

where a and b are the amplitude of the optical signals, and ϕ_a and ϕ_b their respective phases. For signals of equivalent amplitude ($a = b$), the output of the interferometer can be expressed in function of the phase difference $\Delta\phi_{a,b} = \phi_b - \phi_a$, and is given by the expression:

$$\begin{bmatrix} Out_A \\ Out_B \end{bmatrix} = T_{MMI} \cdot \begin{bmatrix} A \\ B \end{bmatrix} = \begin{bmatrix} \sqrt{2}/2 \cdot (e^{-j\Delta\phi_{a,b}} + j) \\ \sqrt{2}/2 \cdot (e^{-j\Delta\phi_{a,b}} - j) \end{bmatrix} \tag{5.8}$$

This allows us to extract the relative phase difference $\Delta\phi_{a,b}$ between the two optical signals in function of the values of the MMI outputs Out_A and Out_B.

Fig. 5.12(top) shows the output of the interferometer in function of the phase difference between signals A and B. We notice that when the phases are equal ($\Delta\phi_{a,b} = 0$) we have equal power distribution among the outputs of the MMI, while for phase difference multiples of $\pi/2$ we guide all the light to either one of the two MMI outputs. To perform the readout of the interferometer we use a pair of balanced photodiodes to convert the optical signal into electrical (Fig. 5.11). The BPD encodes the phase difference in a symmetric electric signal, which can be used by external electronics to recover the relative phase difference between the monitored signals.

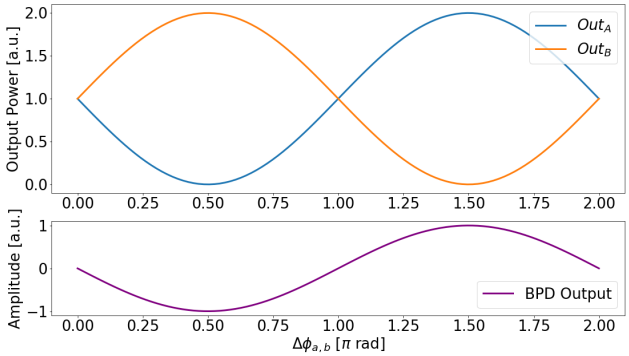

Figure 5.12: (top) Output of the MMI in function of a phase difference between signal A and B, assuming the signals have equal amplitude. (bottom) Theoretical balanced photodiode response in function of the phase difference $\Delta\phi_{a,b}$.

We extend the theoretical analyses for a PDM operating with input signals with different amplitude values in Appendix B.

5.2.2 Phase difference monitor implementation

Fig. 5.13 shows a microscope picture of the fabricated phase difference monitor. We implemented the PDM using a 2×2 MMI as an interferometer and a pair of

germanium photodiodes for the BPD. We use optical taps to couple light from the monitored waveguides to the PDM. To reduce phase error we make the waveguides connecting the optical taps to the MMI as short as possible. It is worth mentioning that this application relies on the maturity of the photodiodes. If the two photodiodes have different response the PDM output is compromised.

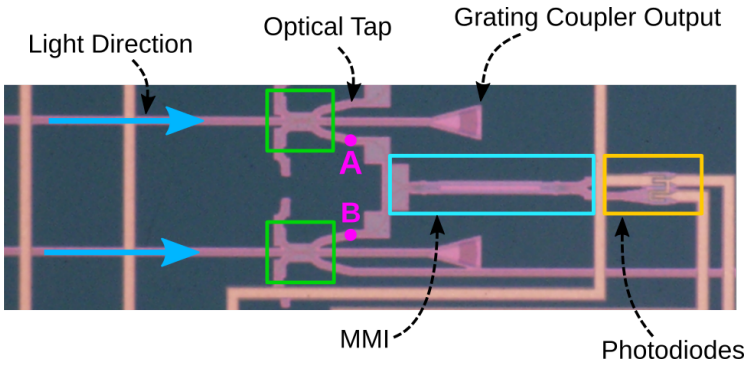

Figure 5.13: (a) Microscope picture of the implementation of the phase difference monitor using the iSiPP50G platform from imec. (b) close up picture showing the PDM used to monitor the phase difference between the optical signal in two waveguides.

The circuit is implemented using imec's iSiPP50G platform. Both the MMI and the germanium photodiodes are provided by the platform *process-development kit* (PDK), while the directional coupler used as optical tap is developed as discussed earlier in this chapter. The readout of the BPD circuit is done using a simple *transimpedance amplifier* (TIA).

5.2.3 Experimental validation

To validate our integrated phase difference monitor we compared it against an external (off-chip) interferometer to measure the phase shift induced by a heater in a photonics circuit. We integrated our PDM in a simple phased array circuit (Fig. 5.14(a)) to monitor the difference between the phases of the signals in the arms of the phased array. Each arm has a heater, used to induce a phase shift, and a phase difference monitor is placed at the end of each pair of arms, using an optical power tap. By comparing the two tapped signals we can extract the phase difference between the the two waveguides. Fig. 5.14(b) shows a microscope picture of the full device.

To test the phase difference monitor we operate a single heater in the circuit (Ps_1, Fig. 5.15(b)) to induce a phase shift in the first arm of the phased array circuit, while the second arm is used as a reference point. The PDM taps a fraction of light at the end of the phased array waveguide arm (points A and B in Fig. 5.15(b))

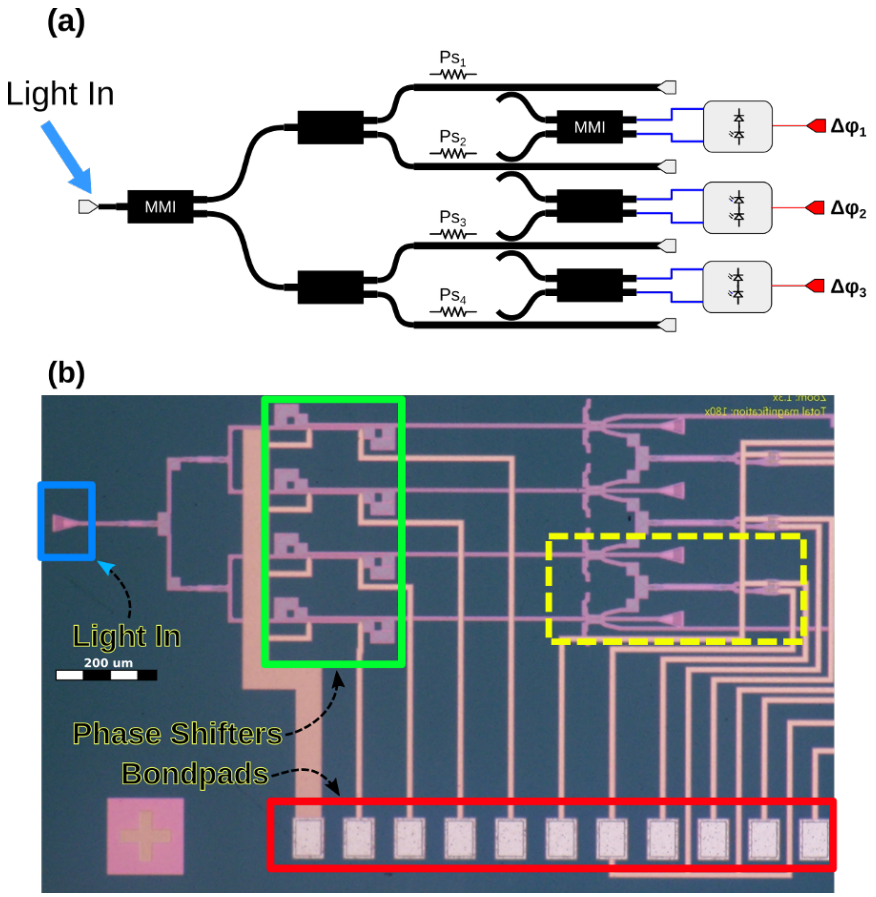

Figure 5.14: (a) Schematic of a phased array circuit with phase difference monitors and balanced photodetectors at the outputs. (b) Microscope picture of the fabricated device.

to perform the phase difference measurement. The phase difference $\Delta\phi_{A,B}$ can be read from the electrical signal of the BPD.

Light is injected in the circuit via its grating coupler input (Fig. 5.15(b)). We then apply a voltage signal in the heater PS_1 to induce a phase shift in one of the arms of the circuit (while the adjacent arm is used as reference). That creates a phase difference between points A and B that can be read from the balanced photodiode output. The measured output signal from the phase difference monitor can be seen in Fig. 5.16(top). From the plot it is possible to see that the readout of the PDM suggests that a phase shift is induced by the heater. An increase in the voltage in Ps_1 (and, therefore, in its dissipated power) causes the optical power at the output of the MMI of our PDM change from Out_A to Out_B (and back, as we keep increasing the power). This results in a voltage output in the

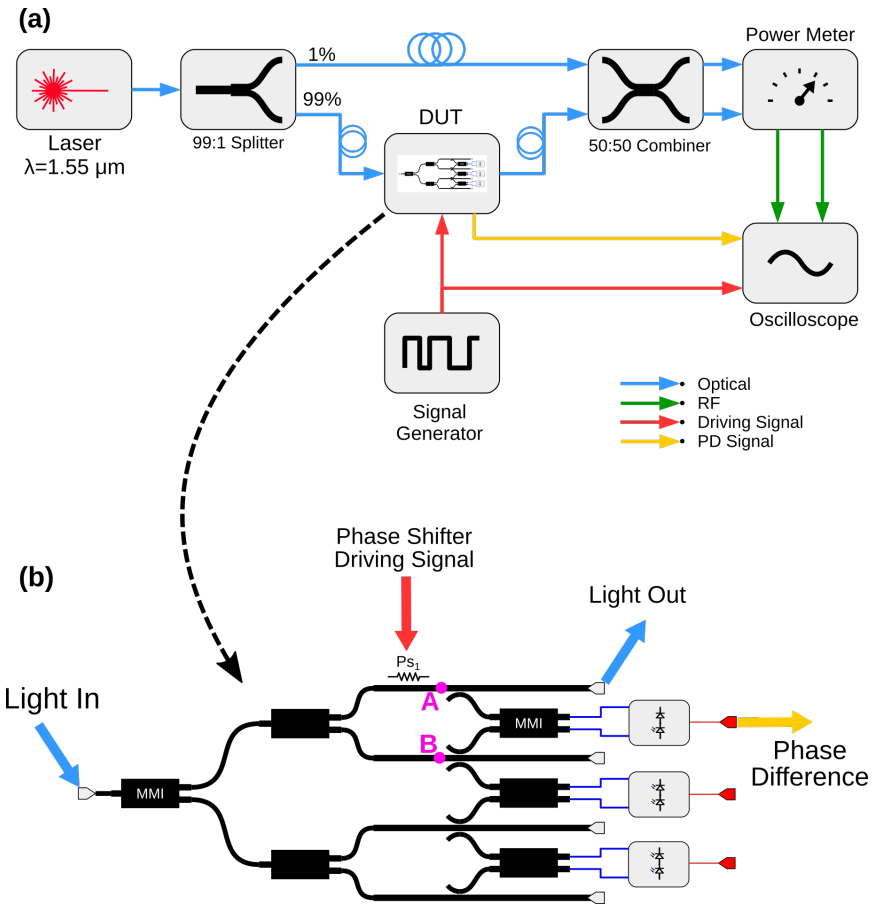

Figure 5.15: (a) Schematic of the measurement set-up used to test the phase-difference monitor. (b) 1×4 phased array circuit with integrated phase shifter used to test the phase difference monitor. Each pair of waveguide arms in the circuit is equipped with phase-difference monitors using balanced photodiodes.

BPD proportional to the induced phase shift. This result agrees with the predicted response shown in Fig. 5.12(bottom).

To confirm that the signal read from the PDM is indeed due to Ps_1 induced phase shift we compared the on-chip measurement with an external interferometer. To do so we split the optical signal before coupling it to the PIC (Fig. 5.15(a)) using a $99/1$ optical coupler. The 99% fraction of the optical power is coupled in the PIC while the remaining is used as reference. The light is then coupled out of the chip and combined with the 1% reference signal using a $50/50$ combiner. The phase shift induced by Ps_1 affects only the light coupled to the optical chip, while the 1% reference signal remains without phase change. This allows us to extract the

induced phase shift caused by Ps_1 from the interference between the two signals in the $50/50$ coupler.

Fig. 5.16(bottom) shows the measured signal from the external interferometer. We can notice an agreement between the two measurements (on-chip PDM and external interferometer), which indicates that both methods capture the same phenomenon. With this we conclude that the PDM can be used to infer phase difference between two waveguides with optical signals of same wavelength.

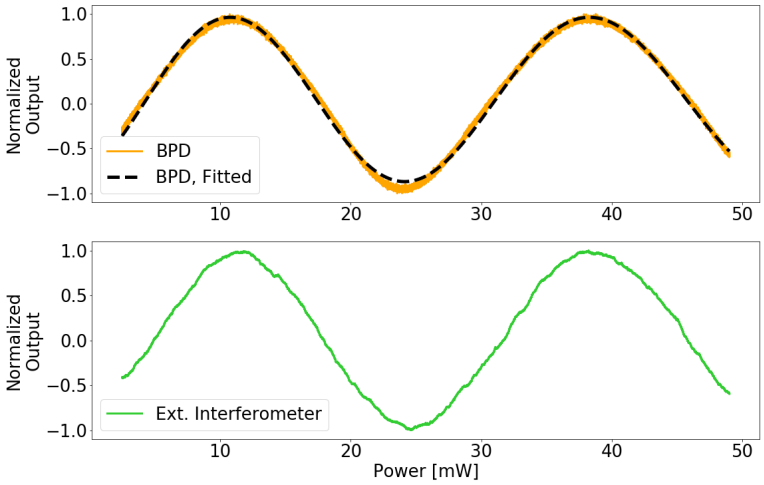

Figure 5.16: Phase difference measurement result from internal balanced-photodiode (top) and the external interferometer (bottom). We notice a visible agreement between the two measurements, indicating that the internal PDB circuit can be used as a reliable phase monitor. The reason we have less noise in the internal BPD measurement when compared to the external interferometer is that the internal circuit has to deal with less ambient variations, in special thermal fluctuation in the optical fibers of the interferometer.

Both measurements (on-chip PDM and external interferometer) were realized simultaneously to ensure that both methods experience the same conditions. We can notice that the signal obtained from the external interferometer presents a higher noise level than the on-chip PDM measurement and we attribute such noise to ambient variations in the measurement environment, in special due to temperature oscillation.

5.3 Control loops

To improve control on photonics components we introduce the use of closed feedback loops along the circuit [10, 11]. Control loops can be used for different purposes [12], such as power control, crosstalk minimization [13], real time monitoring [14], etc.

5.3.1 Tunable coupler control

As introduced earlier in Section 3.2.2, a symmetric MZI with phase shifter in both its arms (Fig. 5.17) operating as a tunable coupler can be operated in two ways: differential-mode, where we change the coupling ratio of the MZI by applying a phase difference between the two arms of the device, and common-mode, where we induce the same phase shift in both arms, therefore keeping the coupling ratio, but resulting in a net phase shift at the output of the device.

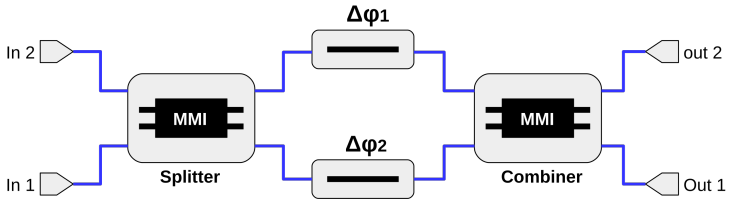

Figure 5.17: Schematic of a symmetric 2×2 MZI used as tunable coupler.

A MZI with two phase shifters ϕ_1 and ϕ_2 can be expressed by its transfer matrix:

$$\begin{bmatrix} T_{cross} \\ T_{bar} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} e^{j\phi_2} - e^{j\phi_1} \\ -j(e^{j\phi_2} + e^{j\phi_1}) \end{bmatrix} \tag{5.9}$$

We can express the transmission of the MZI by the difference between the two phase shifts in the mzi $\Delta\phi_{1,2} = \Delta\phi_2 - \Delta\phi_1$:

$$T_{cross} = \cos^2 \frac{\Delta\phi_{1,2}}{2} \tag{5.10}$$

and:

$$T_{bar} = \sin^2 \frac{\Delta\phi_{1,2}}{2} \tag{5.11}$$

Notice that the absolute value of $\Delta\phi_1$ and $\Delta\phi_2$ doesn't affect the power transmission of the device, unless it changes the phase difference $\Delta\phi_{1,2}$. That happens because any joint phase increase experienced by the two arms of the MZI will not

result in a net phase difference at the input of the combiner of the MZI, therefore not changing the output of the interferometer. As a consequence, the phase shift induced by the common-mode operation can be expressed by:

$$\Delta\phi = Min\{\Delta\phi_1, \Delta\phi_2\} \tag{5.12}$$

as it expresses the common phase shift induced in both arms of the MZI.

The two operation modes of the MZI require control algorithms to ensure proper operation, in special the common-mode driving, as it requires the manipulation of multiple phase shifters simultaneously. It is the role of the operating algorithm to properly choose the values of $\Delta\phi_1$ and $\Delta\phi_2$ to implement the functionality specified by the photonics circuit.

5.3.1.1 Common mode driving

As discussed earlier in Section 3.2.2, we can use an MZI-based tunable coupler to induce a pure phase shift by operating it in common mode. This is achieved by applying an equal phase shift $\Delta\phi_1$ and $\Delta\phi_2$ in both arms of the MZI in such way that $\Delta\phi_{1,2} = \Delta\phi_1 - \Delta\phi_2$ remains constant.

The challenge of operating an MZI in common-mode driving is that we have to ensure that we apply the same phase shift in both arms of the MZI, otherwise we end up changing its coupling ratio instead. For this we need to have a fine control over both phase shifters in the MZI. As common-mode and differential-mode driving can be used simultaneously, the voltage level values at Ps_1 and Ps_2 are not necessarily equal at the start of the common-mode operation. That means that, to induce the same $\Delta\phi$ in both phase shifters we might need distinct values of ΔV for each heater due to the quadratic response of the thermo-optic phase shifters (see Section 4.2).

Even though digital driving could help improving the linearity of the phase shifter response, we still have to deal with fabrication tolerances [15] and the non-linearity of the resistance of the heater in function of the dissipated power, as discussed earlier in Section 2.2.1.1. Fig. 5.18 shows a measured MZI response in function of the driving voltage at the phase shifter and compare it with the expected ideal response. It is possible to see that for low voltages (equivalent of $\Delta\phi < \pi\ rad$) we have a fair agreement between ideal and measured responses. However, as the voltage (and, as consequence, the dissipated power) increases, the value of the heater resistance increases as well (see Section 2.2.1.1), resulting in less power dissipation per increased voltage unit. The effect is clear in Fig. 5.18(bottom), where we can see an increase in the phase deviation between ideal and measured values as the driving voltage increases.

The trivial solution for this problem is to perform a pre-calibration step on each phase shifter in the circuit before operation and use a look-up table to correlate the

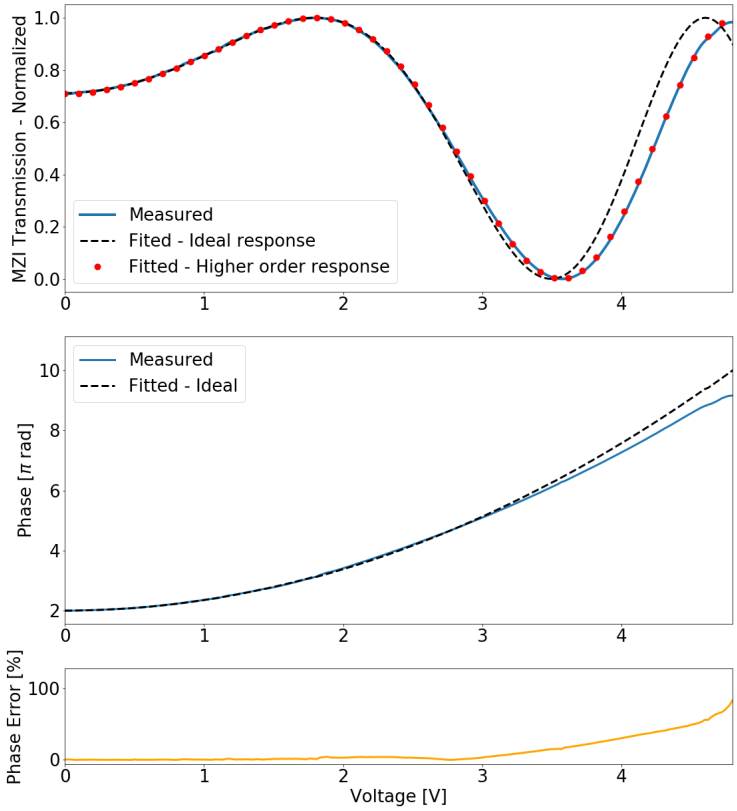

Figure 5.18: (top) Output power from MZI driven in differential mode. Due to imperfections in the phase shifter and its non-linear behavior, we see that there is a disagreement between the measured and the ideal response. (bottom) Accumulated phase shift over in function of the voltage applied to the phase shifter. We notice that the phase has a non-linear response in function of the applied voltage.

driving voltage value to the induced phase shift. Although this should circumvent the non-linearity issues of the phase shifter, we would still have to deal with thermal-crosstalk [16] issues and environmental variations (such as temperature fluctuations) [17] that cannot be addressed by this method.

Our approach to deal with this problem is to implement a feedback-loop that uses one of the outputs of the MZI as a reference point. This can be implemented

using an optical tap to monitor one of the outputs of MZI. Fig.5.19(a) shows the basic building blocks of the feedback loop system used to control the MZI. One of the outputs of the MZI is used as a reference point during the common-mode driving. If the optical power at the reference point starts deviating from its original value the algorithm is triggered to compensate for this error. This ensures that, during a common-mode driving operation, we keep the coupling ratio of the tunable coupler stable.

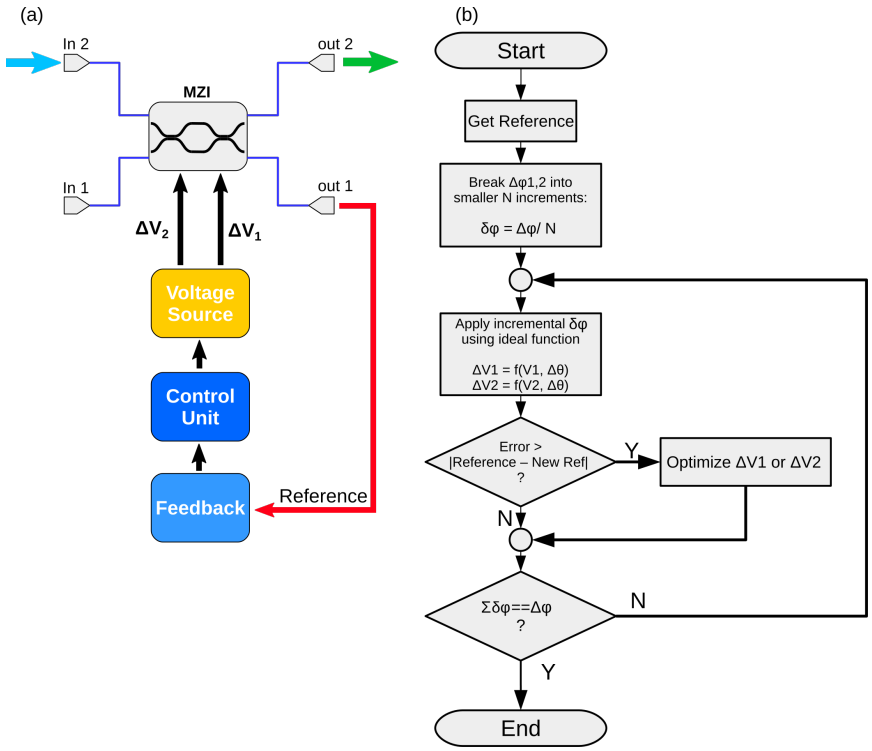

Figure 5.19: (a) Schematic of the MZI with a feedback control loop. (b) Flux diagram of the commom-mode driving algorithm.

The diagram flow of the algorithm used to implement common-mode driving is shown in Fig. 5.19(b). When we want to induce a common phase shift $\Delta\phi$ in our MZI the algorithm first records the value of the reference point, which will be used to keep the coupling ratio of the MZI fixed. Next we divide the value of the phase shift in N small increments ($\delta\phi = \Delta\phi/N$) and proceed, in a loop, to perform N-times $\delta\phi$ increments instead of one single larger increment. We do this for two reasons: first, to avoid sudden changes that might induce large fluctuations of the power level at the outputs of the MZI. Second, in many applications (such as adaptive algorithms) we don't know the exact desired phase shift to be applied

beforehand. These applications work by a constant increase (or decrease) in the phase shift until some condition is satisfied. The incremental approach adopted in our feedback algorithm automatically allows its use in such adaptive applications.

Once we have our minimum $\delta\phi$ incremental value we calculate, using the ideal response of the phase shifter, the incremental ΔV_1 and ΔV_2 to be applied to the phase shifters. This incremental values have inherent errors (as we calculate it from the ideal response of the phase shifters) but as we advance in small increments of $\delta\phi$, the error, per step, is minimized.

Our next step is to verify the total accumulated error after the incremental step. We do this by comparing the original reference value with a new read-out from the reference port. If the deviation is above the threshold we perform a fine tuning in one of the phase shifters to restore the power at the output to its original value. We will discuss the optimization function in Section 5.3.1.3.

We then repeat all the steps for the next increment of $\delta\phi$ until we cover the whole $\Delta\phi$ value, or until some external condition is satisfied.

It is important to point out that this algorithm, as it has been described, only works if the power at the input of the MZI remains stable during the common-mode operation, as it uses the output power as a reference value. If needed, the algorithm can easily be modified to operate with non-constant input power instead. This can be done by taking the two outputs of the MZI as reference, instead of only one, and using the ratio between the two output as the new reference value. The new goal of the stabilization step of the algorithm is to keep the ratio between the outputs stable during the common-mode operation.

5.3.1.2 Experimental validation of common-mode driving

Fig.5.20 shows the driving values and the response of the MZI operating under the described algorithm. We start by operating the MZI in differential mode to ensure that the starting voltage values for Ps_1 and Ps_2 are not equal. Once we start operating it in common mode we can see from Fig.5.20(center) that both phases $\Delta\phi_1$ and $\Delta\phi_2$ increase together, keeping the phase difference $\Delta\phi_{1,2}$ constant all the time. This results in no change in the coupling coefficient of the tunable coupler, which can be verified in Fig.5.20(bottom), as the power values at the outputs remain stable over the whole common-driving period. This shows that the common-driving algorithm employed to operate the MZI succeeds in keeping the output power stable while increasing the phase shift in both arms of the MZI at the same time.

To verify that the common-driving scheme is indeed inducing a phase change at the output of the MZI we used an on-chip interferometer to measure the phase difference between the input and output signals of the MZI during common-mode driving. Fig. 5.21 shows the schematic of the design. We used power taps to sample the signal at the input and output of the MZI. Both tapped signals are sent

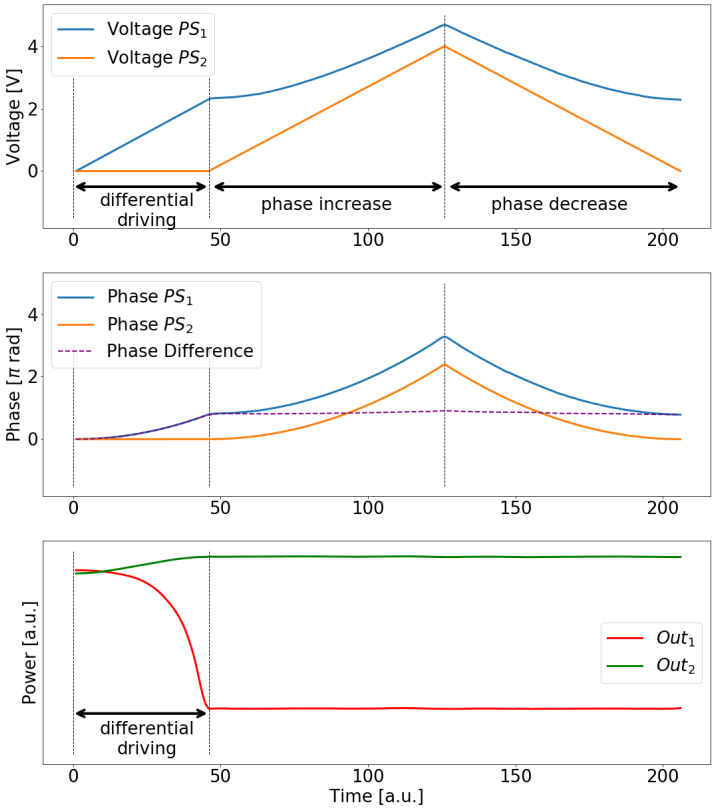

Figure 5.20: Phase shifter operating in differential and common mode. (top) The voltage applied to each phase shifter in the MZI. (bottom) Power at outputs Out_1 and Out_2 of the MZI. Notice that for the differential driving section we see a change in the power of both Out_1 and Out_2, indicating that the MZI is operating as a tunable coupler. For the second part of the plot, where we are driving the MZI in common mode, we see a stable power at the output of the MZI, meaning that we are inducing a phase change in the device without changing its coupling value.

to an MMI that operates as an interferometer. The output of the MMI depends on the phase of its two input signals. By applying phase shift in the MZI (in common-mode driving) we are changing the phase of one of the interferometers input while the other input acts as a reference point. We expect to see a change in

the interferometer outputs that correlates to the common phase of the MZI, while the power level at the output Out_2 should remain stable.

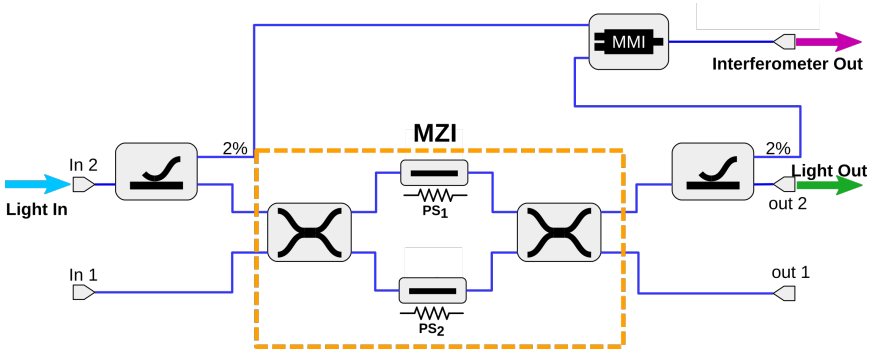

Figure 5.21: MZI with integrated interferometer to measure the relative phase change when operating the MZI in common mode.

Fig. 5.22(top) shows the voltage level at both phase shifters Ps_1 and Ps_2 of the MZI as we operate it in common mode, while Fig. 5.22(bottom) shows the measured values at MZI output Out_2 and the interferometer output. As expected, we have a stable readout at Out_2, indicating that both phase shifters were affected by the same $\Delta\phi$ during the common-mode driving period. Additionally to that, the output of the interferometer shows a power fluctuation as we increase the voltage level at the phase shifters. This is result of the interference between the two signals at the input of the MMI as we increase the total phase induced by the MZI in common-mode driving. From this we conclude that the common-mode driving induces a total phase change at the output of the device while keeping the power level stable at the output of the MZI.

5.3.1.3 Considerations on the optimization function

The common-mode driving algorithm can be split in two main blocks: the iterative increment of the phase shift by $\delta\phi$, and the optimization function, which kicks in when the accumulated error reaches a maximum allowed threshold.

The fine tuning optimization is done by performing a small voltage sweep in the targeted phase shifter, enough to restore the power at the reference point to its target value. The algorithm selects the phase shifter with highest voltage level to perform the fine tuning, as the phase error increases with the driving voltage value (Fig.5.18(bottom)). The new optimized value V at the phase shifter is used to re-calibrate its transfer function, minimizing the error in the next step of the algorithm.

Fig. 5.23 illustrates the optimization phase of the algorithm. Once the power at the reference output of the MZI is above the error threshold, the optimization

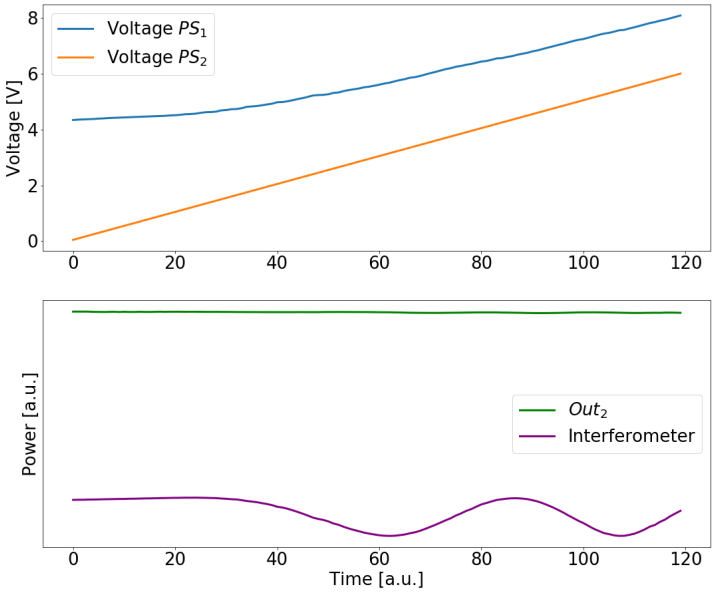

Figure 5.22: (top) Voltage applied at each phase shifter of the MZI to drive it in common mode. (bottom) Power level at the output of the MZI and at the interferometer. As the MZI is being driven in common mode, we see no fluctuation at the power at its output Out_2, meaning that there is no differential driving. The interferometer readout indicates that there is a phase change in the signal, confirming that the common mode driving is induce a pure phase modulation in the signal.

algorithm will start a sweep in the voltage level of the phase shifter with highest voltage level to decrease (or increase) the power level at the referred output and restore it to its target value.

The quality of the common-mode algorithm can be analysed from the ripple level at the reference signal of the MZI. Ideally the reference output should remain stable during the common-mode driving, but a poorly calibrated algorithm can introduce fluctuations on its power level. The parameter used to quantify the quality of the algorithm was the amplitude of the ripple at the reference signal and its deviation from the average value (Fig.5.24).

The step size (in radians) of this sweep is given by the parameter $\delta\phi_{opt}$ of the optimization algorithm. To calibrate the optimization algorithm we tested multiple values for the parameters $\delta\phi_{opt}$ while recording its influence in the ripple level at the output of the MZI. The plot in Fig. 5.25 shows how the recorded values at

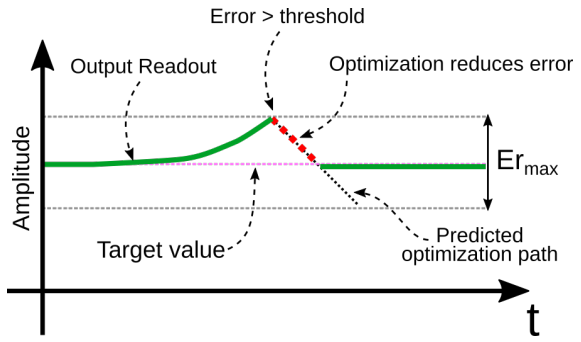

Figure 5.23: Illustration of the optimization function. Once the accumulated error at the reference output reaches the maximum error threshold the optimization algorithm is triggered and performs a power sweep in on of the phase shifters of the MZI to restore the power level at the reference output.

the reference output deviates from average. Ideally the reference output should not contain ripples, therefore all the signal should be clustered at the center of the distribution curve, but we can see that for larger values of $\delta\phi_{opt}$ we have a higher ripple level, and as the size of $\delta\phi_{opt}$ decreases the measured ripple in reference signal decreases as well. Each histogram was obtained by analysing the ripple of an amplitude measurement containing 500 points.

The MZI together with the differential-mode and common-mode driving algorithms constitute the building blocks of the programmable circuits that we are going to discuss in the next chapter. As the functionalities of the programmable circuit emerges from the number of elements in the circuit, it is important to have these building-blocks elements encapsulated and reusable. In our large-scale programmable circuit we no longer address the MZI as a stand-alone component. Instead we recognize the sub-system formed by the photonics component (MZI) the logic (algorithms) and the electronics (for driving and control) as one building block for the system.

5.3.2 $2 \times 2 \times 2$ MZIs control loop

In Chapter 2 we introduced an extension of the MZI, the $2 \times 2 \times 2$ tunable coupler, as an alternative to implement high extinction ratio tunable couplers with imperfect components. One characteristics of this tunable coupler is that it uses two phase shifters (one for each stage of the MZI) in its operation. Because of that the coupling of the device responds to a two-variable function, as shown in Fig. 5.26. That means that, to optimize the function of a $2 \times 2 \times 2$ MZI (to operate in cross or bar state, or in any ratio in between) it is necessary to find the best combination of power in Ps_1 and Ps_2 that results in a minimum (or maximum) in the transmission

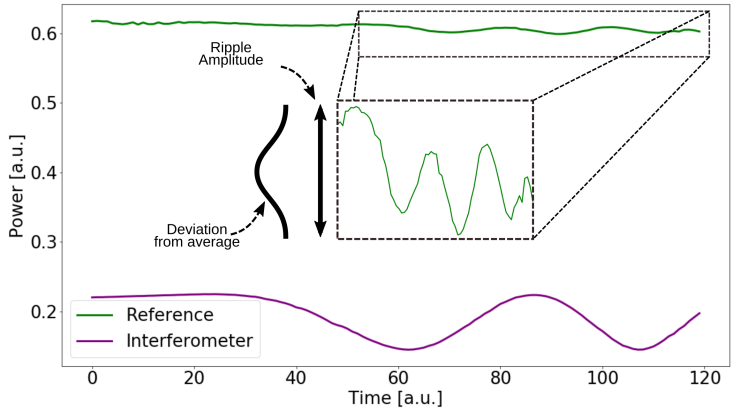

Figure 5.24: A poorly calibrated common-mode driving algorithm causes ripples at the output of the reference signal. To determine the correct parameters for the algorithm we used the amplitude of the ripple and its deviation from average as quality parameters.

function. As we can notice from the measured transmission shown in Fig. 5.26, the MZI has multiple points of maxima and minima, but as the transfer function of the MZI is periodic in both Ps_1 and Ps_2 axis, we assume, in a first approximation, that all local maxima and minima have the same transmission value, therefore we use the optimization algorithm to find the maximum and minimum that requires the smallest values of Ps_1 and Ps_2.

To operate the $2 \times 2 \times 2$ tunable coupler we use a *Gradient Descent Algorithm* [18] as an optimization algorithm to find the points of minima and maxima transmission of the MZI. The gradient descent is an iterative algorithm that operates by solving the target function in multiple incremental step, until it converges to a point where the gradient of the function is zero. For a two-dimension function $f(x, y)$, each iteration of the algorithm is given by:

$$f(x_n, y_n) = f(x_{n-1} + step_x,\ y_{n-1} + step_y) \tag{5.13}$$

Where $step_x$ and $step_y$ are the incremental values applied to the current status of the input variables x and y of the function to be optimized.

The value of the $step$ variables are proportional to the gradient of the function at its current point. If the current point is far from a minimum or a maximum, the value of the gradient will be high, which will result in a long incremental step in the next iteration. If applied to a point that is close to the minimum of the function, the gradient will be small, which leads to a small step size. If the gradient is zero, the step size is also zero, meaning that the algorithm reached its target. The algorithm

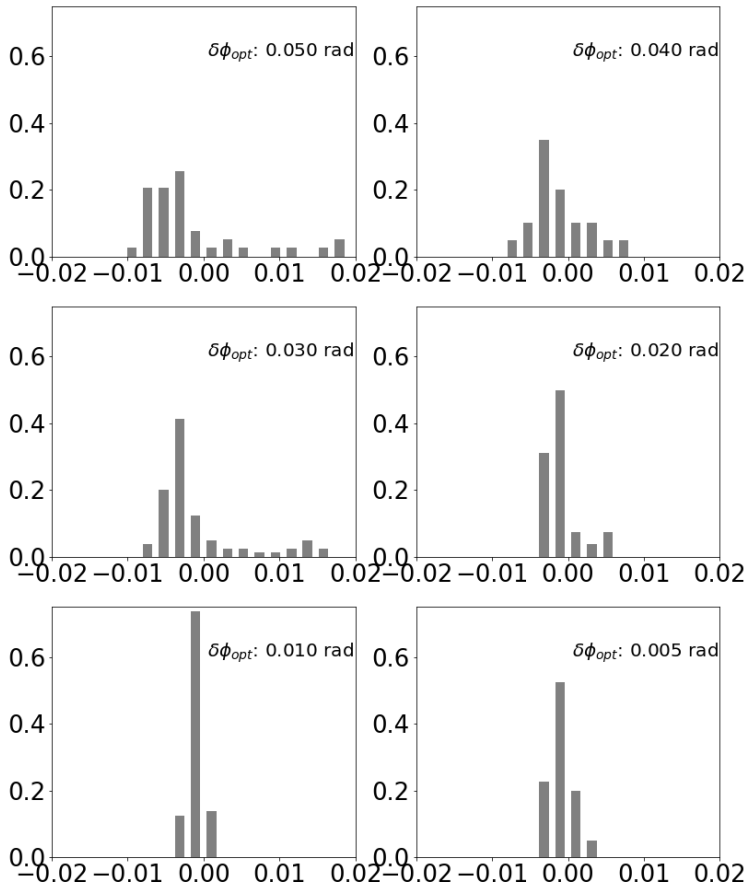

Figure 5.25: Deviation from average at the reference output of the MZI operating in common-mode driving for different values of $\delta\phi_{opt}$.

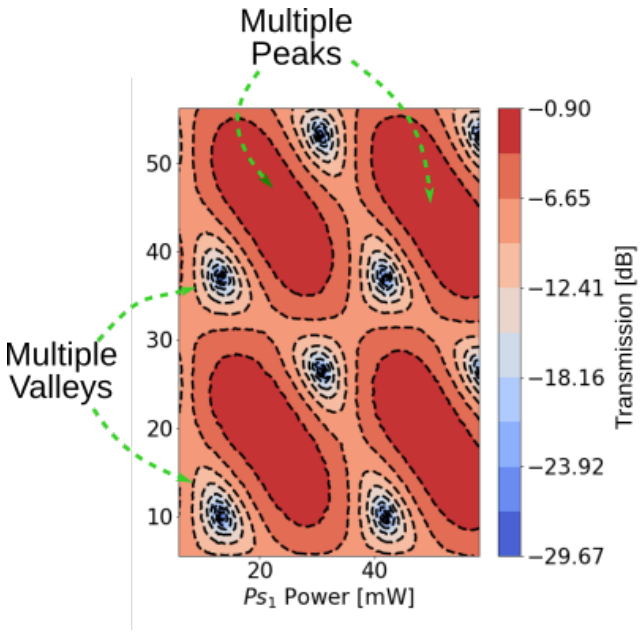

Figure 5.26: Transmission of a $2 \times 2 \times 2$ MZI in function of the power applied at the phase shifters Ps_1 and Ps_2.

can be easily modified to converge into a point of maximum instead by modifying the calculation of the gradient function.

The optimization algorithm flow is illustrated in Fig. 5.27. We start the algorithm by defining the variable L_{max}, that indicates the size of the maximum step possible to be performed at each iteration of the algorithm, and the variables Δx and Δy, that are used to calculate the gradient of the function we are optimizing. The value of the gradient function is given by:

$$\nabla_x = \frac{f(x + \Delta x, y) - f(x - \Delta x, y)}{2 \cdot \Delta x} \tag{5.14}$$

and

$$\nabla_y = \frac{f(x, y + \Delta y) - f(x, y - \Delta y)}{2 \cdot \Delta y} \tag{5.15}$$

Once the gradient of the function is calculated, we update the values of x and y by calculating the next iteration of the optimizing function. The new values are given by:

$$x_n = x_{n-1} + L_{max} \cdot \nabla_x \tag{5.16}$$

and

$$y_n = y_{n-1} + L_{max} \cdot \nabla_y \tag{5.17}$$

The optimizing algorithm repeats the operation steps until the difference between the calculated values at subsequent steps are below the defined precision limit ($|f(x_n, y_n) - f(x_{n-1}, y_{n-1})| < precision$) or until the iteration performs a maximum stipulated number of steps. The later stop condition is used to interrupt non-converging optimization.

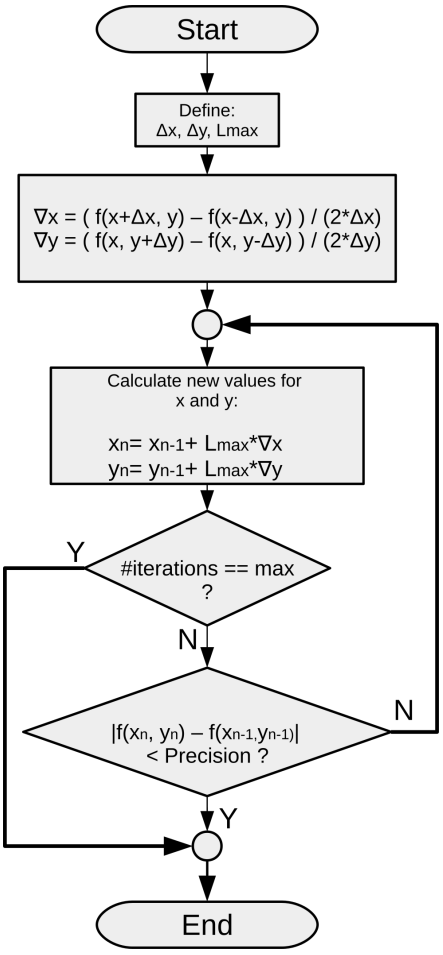

Figure 5.27: Flux diagram of the gradient descend algorithm.

5.3.2.1 Experimental validation of the $2 \times 2 \times 2$ MZI optimization algorithm

We used the described optimization algorithm to operate a $2 \times 2 \times 2$ tunable coupler implemented with power taps at the ports of the component, as illustrated in Fig. 5.28. The optical taps are connected to on-chip photodetectors, that are used to monitor the power at the ports of the MZI. The readout of the photodetectors gives us the relative power level at the output of the device, which is used to implement a feedback loop and to control the tunable coupler.

We can express the function $f(x, y)$ to be optimized by the gradient descent algorithm as the power measured by the power tap in function of the electrical power applied at the phase shifters:

$$f(x, y) = P_{tap} = f(Ps_1, Ps_2) \tag{5.18}$$

Notice that we don't need to obtain the absolute power value at the output of the tunable coupler to use the optimization algorithm here, as the step size and the direction of the optimization algorithm are calculated based on the relative power change induced by each iteration step, as expressed in Eq. 5.14 and Eq. 5.15.

The algorithm uses three main parameters to govern its operation: L_{max}, which is the maximum increment applied at the input variables x and y of the function to be optimized at each iteration. In our implementation of this algorithm this increment refers to the power applied to the phase shifters, and is expressed in mW. The second variable used in the algorithm is the Δx and Δy, which are used to calculate the gradient of the function. Both values also correspond to the power applied at the phase shifters, and their values are expressed in mW.

Fig. 5.29 shows the optimization algorithm being applied to the tunable coupler optimize its transmission to a bar state. In this example value of the deltas used in the gradient function are $\Delta x = \Delta y = 0.5\ mW$, while the value used for the maximum step size is: $L_{max} = 5\ mW$. This allows the algorithm to perform the optimization of the device in thirty steps and achieve an extinction ratio $ER > 20\ dB$. The measurement was performed for a $2 \times 2 \times 2$ tunable coupler operating at wavelength $\lambda = 1.616\ \mu m$, in the same conditions described in Section 3.3.2.2.

The path illustrated in Fig. 5.29(top) shows the path followed by the optimization algorithm during its operation. From Fig. 5.29(center) it is possible to notice that the initial steps of the optimization algorithm ($step < 5$) have a much higher impact than the remaining steps. That's due to the weighting of the step size with the value of the gradient of the function. As we gets close to the target the gradient decreases, leading to a smaller step size.

The algorithm can be used to identify the points of maximum and minimum and, later, use these values to directly drive the $2 \times 2 \times 2$ tunable coupler without iterations. Fig. 5.29(bottom) shows the transmission of the device when following a straight path (illustrated in Fig. 5.29(top)) connecting the points of minimum and

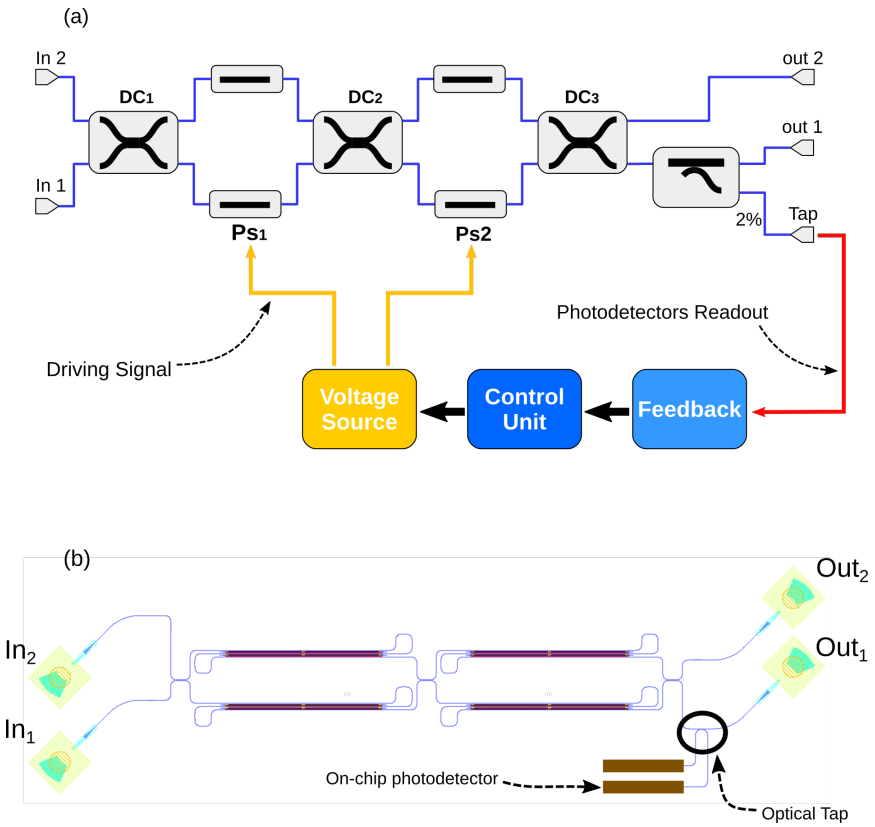

Figure 5.28: (a) Schematic of the $2 \times 2 \times 2$ tunable coupler with the feedback control loop. (b) GDSII layout of the designed component, with power tap at its ports and integrated photodetectors.

maximum obtained from the optimization algorithm. This allows the operation of the device without a feedback loop, which increases the operation speed.

5.4 Summary

In this chapter we discussed how we implement optical power monitoring in integrated photonics circuits, and how we can use the implemented power tap to implement a phase difference monitor. We discussed the use of photodetectors to implement on-chip power monitoring and compared it to the use of off-chip monitoring, with focus on camera monitoring, that can be used for prototyping and development, as it doesn't need the use of full-platform fabrications due its lack of active components.

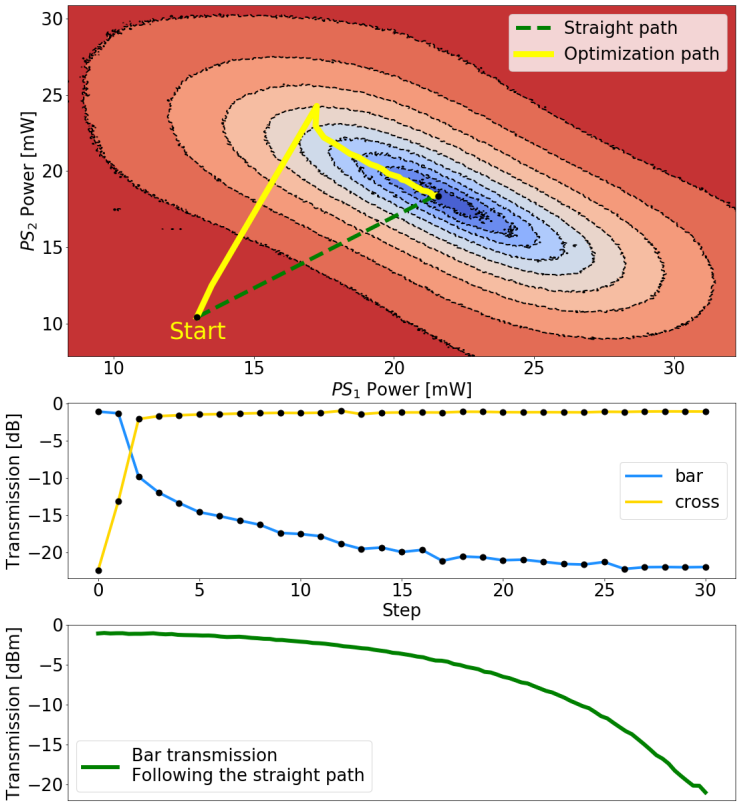

Figure 5.29: (top) Path followed by the gradient descend algorithm used to optimize the transmission of the $2 \times 2 \times 2$ MZI. (center) Progress of the bar and cross transmission along the evolution of the optimization algorithm. (bottom) Transmission of the device following a straight path connecting the points of minimum and maximum.

The second half of this chapter focused on discussing control algorithms used to operate photonics components. The control algorithms are implemented under a feedback loop that uses the power taps to monitor the optical power in strategic parts of the circuit while driving the phase shifters using the driving techniques introduced in Chapter 4. We demonstrate the use of feedback loops to, among other operations, perform a common-mode driving scheme in a 2×2 MZI and to optimize the $2 \times 2 \times 2$ tunable coupler.

The control algorithms discussed in this chapter fall in the category of *local optimization algorithms*, as they focus on controlling one local component from the circuit. In the next chapter we will discuss how we used such local control algorithms to implement programmable silicon photonics circuits, that operates under a broader *global optimization algorithm*.

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6

Demonstrations of programmable PICs

Over the past chapters we discussed the implementation of several building blocks, subcircuits, and techniques with the main focus of implementing programmable photonics circuit in the Silicon Photonics platform. In this chapter we present the implementation of two programmable circuits using such building blocks and we discuss how to apply the techniques developed in this work to implement scalable programmable circuits.

Current state-of-the-art implementation of programmable linear circuits can be separated in two categories: feed-forward and feed-back optical meshes. A feed-forward circuit can be represented by a generic *T-matrix* linear circuit (Fig. 6.1(a)), where the optical signal propagates in only one direction in the circuit. Feedback circuits, on the other hand, allow the implementation of optical feedback loops and delay lines, and can be described as a generic *S-matrix* circuit, as illustrated in Fig. 6.1. This chapter discuss both approaches for programmable circuits implementation.

Figure 6.1: (a) Feed-forward networks can be described by a T-matrix representation, as the optical signal propagates in a single direction, without the possibility of implementing feedback loops. (b) Optical meshes that can implement feedback loops can be described using a S-matrix representation.

This chapter is divided in two main parts. First we introduce the implementation of a feed-forward optical network implemented with MZI-based tunable couplers, based in the topology proposed by Reck [1] and Miller [2, 3]. The circuit is used to demonstrate multiple functions via reprogramming the states of its internal elements. Being the first implementation of such circuit topology in silicon photonics, this implementation was used as an exploratory platform, and was essential to identify the necessity of adopting dedicated actuation and control techniques to scale up the size of the circuit.

The second part of this chapter is dedicated to the implementation of a large-scale mesh-based programmable optical circuit [4, 5]. This circuit is implemented using most of the techniques explored in this thesis, such as digital driving and matrix addressing, to allow the control of a large number of phase shifters ($>$ 300) with fewer voltage sources, and more compact and efficient phase shifters. This section of the chapter is dedicated to discuss the circuit topology and design choices. The designed circuit has been fabricated and is currently in the process of packaging and initial characterization tests.

6.1 Feed-forward optical networks

A great number of optical operations, such as coupling structures, frequency filtering, optical delays, switch networks, and quantum optics operations can be implemented using linear operations [6–10]. In the past years, multiple concepts of programmable photonics circuits based on linear operators have been proposed [11–15]. This approach has been demonstrated in multiple platforms and for different applications, such as quantum optics and machine learning [9, 11].

A generic and reconfigurable optical linear device is a device that implement any linear operation between its inputs and outputs by changing its internal configurations. This approach introduces a versatile and flexible linear optical component that can be configured to perform different complex optical applications. Such a device can be reusable, and scalable if its internal connectivity is reprogrammable. This programmable universal linear circuit makes use of the fact that linear optical components can be completely described as a device that converts one set of orthogonal input modes to a matching set of orthogonal output modes [16]. Therefore, we can explore the structure of programmable mode converter circuits [3] to implement linear operations on the signals at the input of the device.

One important aspect of a programmable circuit is that it should be easily programmable to perform the desired functions [17]. It is possible to avoid the calculation of each individual element of the programmable circuit by using a self-configuring calibration mechanism to train the circuit [2, 3]. This configuration step involves the use of feedback loops that operates on individual elements of the

circuit. In this section we are going to discuss the implementation of a 4×4-port linear operator based on a feed-forward MZI mesh and the procedures used to program the device.

6.1.1 Discrete optics theoretical device

To illustrate the conceptual programmable linear circuit we start from a minimum unit cell that can perform the linear operation between two optical signals [3]. This 2×2 unit cell, illustrated in Fig. 6.2(a), is composed by a tunable phase shifter, a mirror with variable reflectivity and a pseudo-transparent[1] photodetector. By controlling the reflectivity of the mirror and the value of the phase shifter it is possible to control the interference between the signals from inputs A and B and, therefore, guide the light to either output C or D (or a linear combination between the two). The transmission of the device for two arbitrary signals at the inputs A and B is given by:

$$T_{AB\to D} = A \cdot \sqrt{r} \cdot e^{j\Delta\phi} + B \cdot \sqrt{t} \cdot e^{j\pi/2} \tag{6.1}$$

and

$$T_{AB\to C} = A \cdot \sqrt{t} \cdot e^{j\Delta\phi} \cdot e^{j\pi/2} + B \cdot \sqrt{r} \tag{6.2}$$

Where r is the reflectivity of the variable mirror, $t = 1 - r$ is the transmission of the variable mirror, and $\Delta\phi$ is the phase shift applied by the phase shifter at input A. The input signals A and B are complex values, such as output signals C and D.

Fig. 6.2(b) illustrates the process of optimizing the device to guide all the light from its inputs to one specific output. The device is illuminated with two arbitrary optical signals A and B, with arbitrary amplitude and phase (Fig. 6.2(b1)). Initially the phase shifter and the variable mirror have random values, which causes the light to go arbitrarily to both outputs C and D.

To guide all the light from inputs A and B to one output D we apply a two-step optimization that aims to minimize the power at output C, where the pseudo-transparent detector is localized. The first optimization step we apply is the *phase* optimization, where we adjust the phase shift $\Delta\phi$ to set the two incident signals at output C to be in antiphase, minimizing the power level at the detector.

The second optimization step is the *balance* optimization, which aims to equalize the amplitude of the two wave fronts at the output C of the device, where the

[1] The pseudo-transparent photodetector, as a theoretical concept, allows power monitoring without introducing loss in the system. We implemented our pseudo-transparent detectors using optical power taps, as discussed in Chapter 5

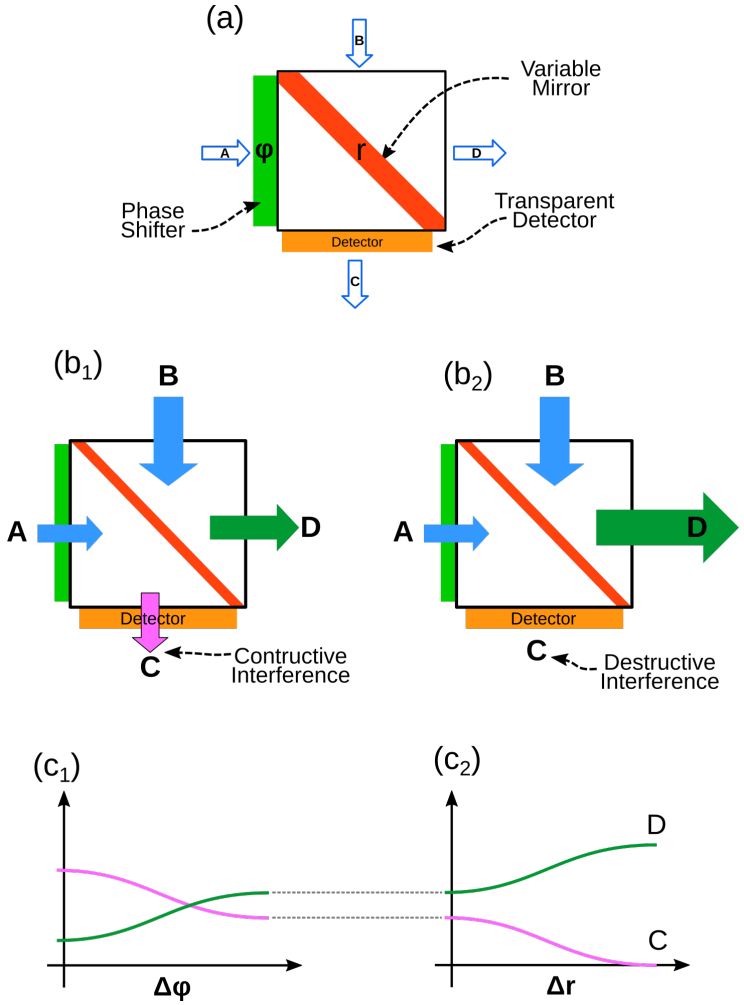

Figure 6.2: (a) Schematic of the unit cell implemented as a theoretical discrete optical device. (b) Optimization of the unit cell to guide the light at inputs A and B to output D. (c) Power evolution at outputs C and D during the phase optimization $\Delta\phi$ and the reflectivity optimization Δr

detector is localized. As the incident signals at output C are in antiphase, equalizing their amplitudes at this port of the device places the two wavefronts in destructive interference, resulting in no transmission to output C. Due to the reciprocity of the device, the contribution signals at output D are in constructive interference, which maximize the power at this output.

Using this approach we can operate the device by just minimizing the power read at the detector at output C. The same process can be used to guide the light to output C instead. To do that we have to modify the algorithm to maximize the power at the detector during the optimization steps instead.

6.1.2 Linear operator from multiple unit cells

To implement a linear combination between multiple inputs signals we can connect an arbitrary number of unit cells as illustrated in Fig. 6.3(a). By optimizing each individual cell in the circuit we can guide all the contributing inputs to the output of the circuit.

One characteristic of this topology is that, after being optimized for an initial input set, any second input signal that is orthogonal to the first one will see this stage as a transparent device [3]. Because of that we can connect multiple stages together (Fig. 6.3(b)) and map any different combinations of input signals to different outputs of the device.

6.1.3 Realization of a 4×4 Operator[2]

We implemented the described concept as a 4×4-port linear operator in an silicon photonics integrated circuit. The unit cell is implemented using a symmetric MZI operating as a tunable coupler, as illustrated in Fig. 6.4. Operating the MZI in differential-mode driving changes the coupling ratio of the device, which can be mapped onto the variable reflectivity of the mirror of our unit cell. To implement the tunable phase shifter at the input A of the unit cell we can operate the MZI in common-mode driving scheme. Therefore, we can perform both the phase and balance optimization steps described earlier by performing a common-mode and differential-mode driving of our MZI.

The pseudo-transparent detector is implemented using a power tap attached to one of the outputs of the device. Fig. 6.4(b) shows the schematic of the equivalent implementation of the unit cell and Fig. 6.5 shows a microscope image of the fabricated device before processing it to add phase shifters.

We implemented the MZIs using imec's passive Silicon-on-insulator platform using 2×2 MMIs as splitters and combiners and $450\ nm$ wide silicon waveg-

[2]Part of this work was done in collaboration with Laurent Van Acker, in the context of his thesis project.

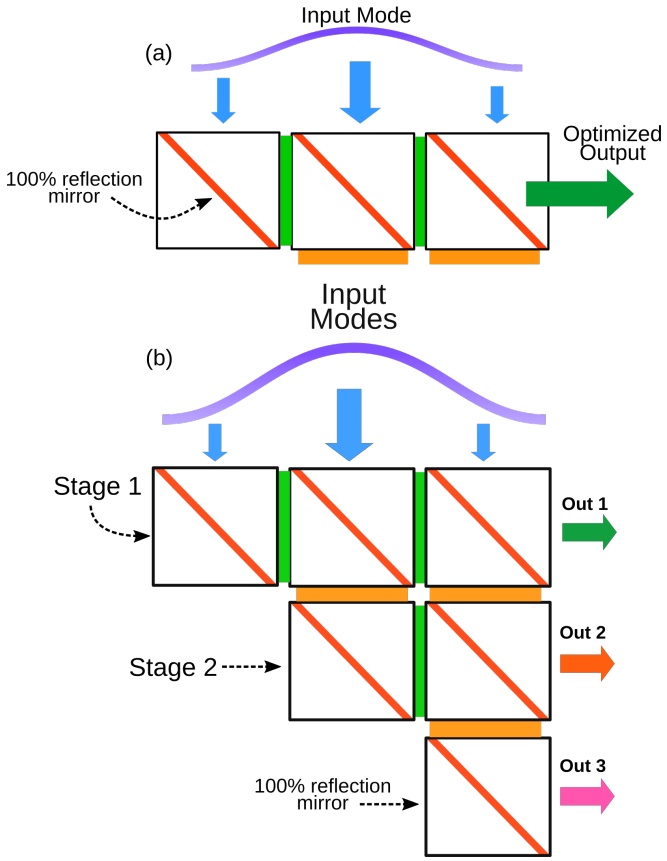

Figure 6.3: (a) Multiple unit cells can be connected in series. By optimizing the device we can guide all the incident light to a common output of the circuit. (b) Multiple stages can be connected together to implement a mode converter.

uides as arms [18]. The choice of MMIs as splitters/combiners (over directional couplers) is due to its broadband characteristics [19, 20].

The phase shifters are added on the fabricated chip by postprocessing titanium line heaters on the arms of the MZI, following the methodology discussed earlier in Chapter 2. We implement phase shifters in both arms of the device, which allow it to be operated in differential-mode and common-mode.

The 4×4-port linear circuit was implemented in a three-stage topology, as illustrated in Fig. 6.6(a). Power monitors are placed between the stages to act as the pseudo-transparent photodetectors and allow the monitoring of the power flowing from a stage to the next one. The power monitors are implemented using optical power taps connected to grating couplers, following the methodology discussed in

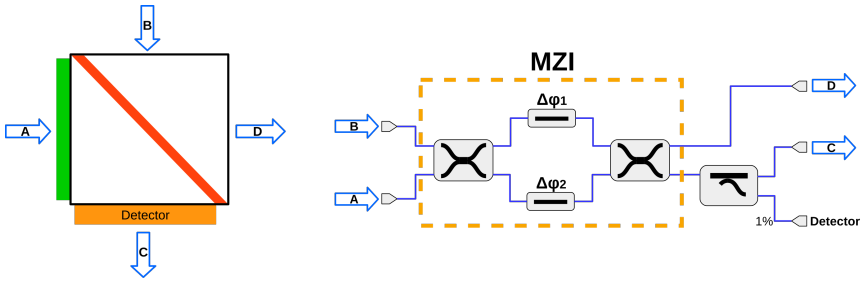

Figure 6.4: The unit cell can be implemented as a MZI. The differential-mode actuation of the MZI control the reflectivity of the mirror, while the common-mode operates the phase shifter function.

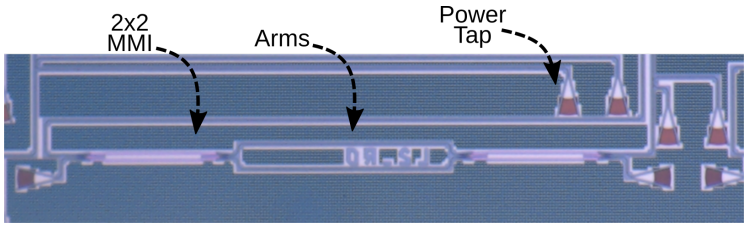

Figure 6.5: Microscope picture of the fabricated 2×2 *MZI.*

Chapter 5. We also introduce power monitors at the output of the device, which allows us to monitor the states of the detectors and of the output of the circuit at the same time using a camera monitoring approach. Optical IO is done via optical fibers vertically-coupled to grating couplers connected at the inputs and outputs of the circuit. Fig. 6.6(b) shows a microscope picture of the fabricated device.

6.1.4 Circuit operation

To operate the circuit we use a two-level control hierarchy, splitting the control of the unit cells from the overall control of the circuit. We call each of these levels *local optimization* and *global optimization* algorithms.

The global optimization algorithm is in charge of defining the operations to be performed by the circuit and defining what should be the state of each unit cell in all the stages of the circuit to perform such operation. Once the global optimization algorithm defines what should be the state of each unit cell it delegates the control of the unit cells to the local optimization algorithms.

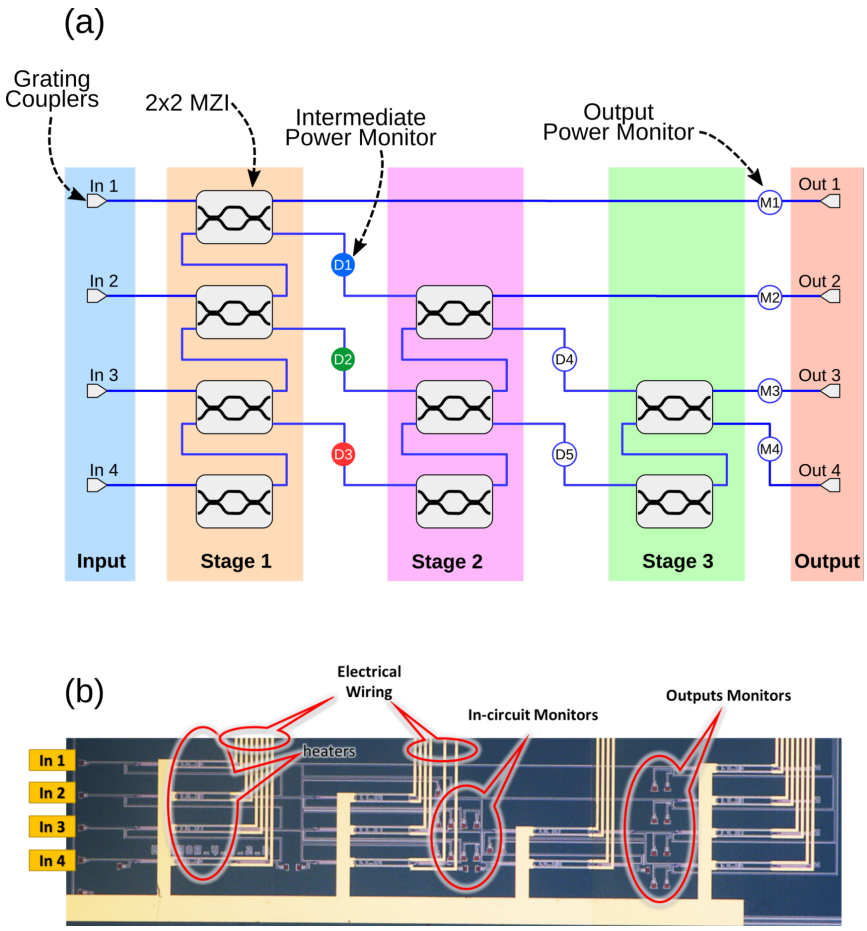

Figure 6.6: (a) Schematic of the 4×4-port universal linear circuit implmented with MZIs. The circuit is implemented in three stages, with tap-based detectors between the stages. (b) Microscope picture of the fabricated 4×4-port universal linear circuit.

6.1.4.1 Local optimization algorithm

The role of the local optimization algorithm is to control one individual unit cell to perform a specific task, which can be either maximizing or minimizing the power at the detector associated to this unit cell. This is done by performing both the phase and balance optimization discussed earlier, while using the associated detectors to implement the feedback loop and stabilize the circuit. Each unit cell has its own dedicated instance of a local optimization algorithm that operates independently from the rest of the circuit. The phase and balance optimization of the unit cells are performed by the common-mode and the differential-mode driving of the

MZIs.

Fig. 6.7 shows the local optimization algorithm realizing a balance optimization at one unit cell of the circuit (composed by MZI_3 and D_3) to minimize the power at the detector D_3. The inset plot shows the measured power at the detectors D_1, D_2, and D_3 during the optimization process. We notice that as the power in D_3 decreases, the power at both D_2 and D_1 increases. This happens because as the balance optimization is realized, the local optimization algorithm drives its associated MZI in differential mode, changing the coupling ratio of the MZI. This causes the optical power to either go forward to the next stage (which increases the power read at D_3), or to continue in the same stage (decreasing D_3 and increasing both D_2 and D_1). As the local optimization algorithm in this example is configured to minimize the power at D_3, the algorithm will return to the point of minimum value at D_3 after the initial scan.

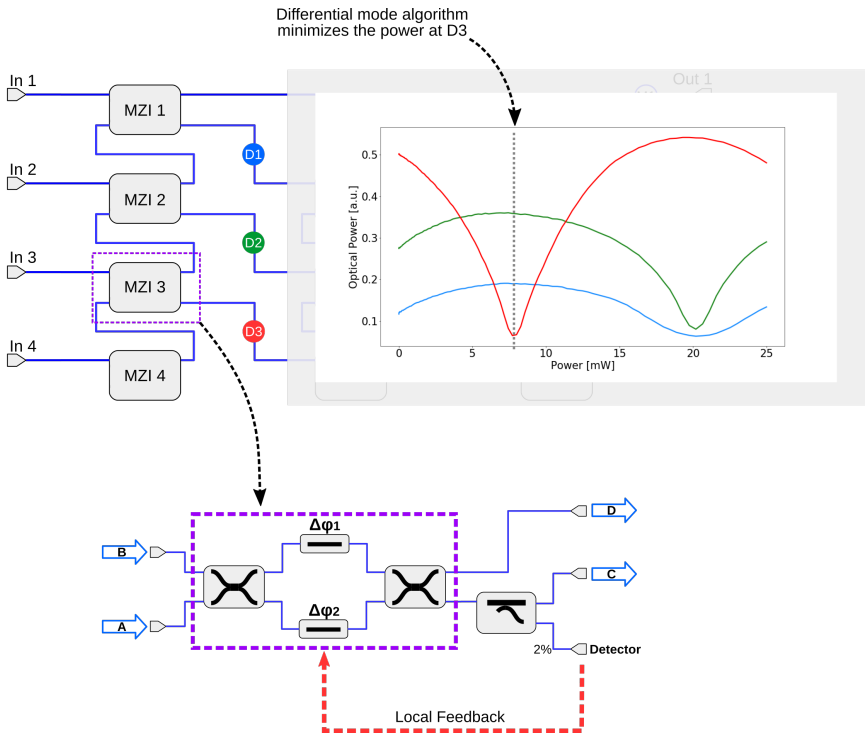

Figure 6.7: Measured power at detectors D_1, D_2, and D_3 during the differential driving of MZI_3.

A second optimization process realized by the local optimization algorithm is the balance optimization, where it adjust the phase shift $\Delta\phi$ at the input of the unit cell to change the interference between the two contributing input signals. This is

done by the local optimization algorithm by performing a common-mode driving at the associated MZI, which than acts as a phase shifter. That means that for performing a balance optimization in a unit cell we need a detector to be used as a target for the optimization process, but we also need an auxiliary detector to use as reference and stabilize the common-mode driving algorithm, as discussed earlier in Chapter 5.3.1.1.

Fig. 6.8 shows how we use two detectors for the common-mode optimization process. In this example the local optimization algorithm operates MZI_3 in common-mode to act as a phase shifter and change the optical phase at one of the input signals of MZI_2 in the balance optimization step. To do so, the local optimization algorithm drives MZI_3 in common-mode, using the detector D_3 as a reference point to guarantee the stabilization of MZI_3 during the common-mode driving, as discussed in Chapter 5.3.1.1. We see in the plot in Fig. 6.8(a) that the power at D_3 remains stable during the optimization process, as the common-mode driving operation changes only the outcome phase of MZI_3, without changing its coupling ratio. We can also see the power at D_2 changing as the optimization process happens. This is due to the change in the phase of the optical signal at the input of MZI_2 due to the common-mode operation. This is how the local feedback loop operates the phase optimization in the circuit.

The balance and phase optimization of the unit cells are the fundamental optimization steps that are performed indirectly by the global optimization with the aide of the local optimization algorithms. This strategy of splitting the operation of the circuit in two levels leads to a simplification in the control process, and facilitates the debugging and troubleshooting of the circuit. It also opens the possibility for distributed control and parallelization of the operation of the circuit, which can be useful for large scale implementations of programmable PICs.

In the coming sections we discuss how we use the optimization algorithms to perform specific functions using the implemented device. To demonstrate the 4×4-port linear circuit we implemented two distinct functions using the same device: an arbitrary cross-bar optical switch and an adaptive beam coupler. Each application uses a distinct algorithm for training the circuit and implementing its function. Both applications use the local optimization algorithms to perform the balance optimization of the unit cells of the circuit, while the beam coupling application uses also the phase optimization process.

6.1.5 Cross-bar switch

The first operation that we demonstrate using the 4×4 linear operator is a cross-bar switch matrix that guides the light from the four inputs to any permutation of the four outputs. As this operation can be implemented by toggling the MZIs in the circuit between bar and cross-states, the circuit can be configured using only

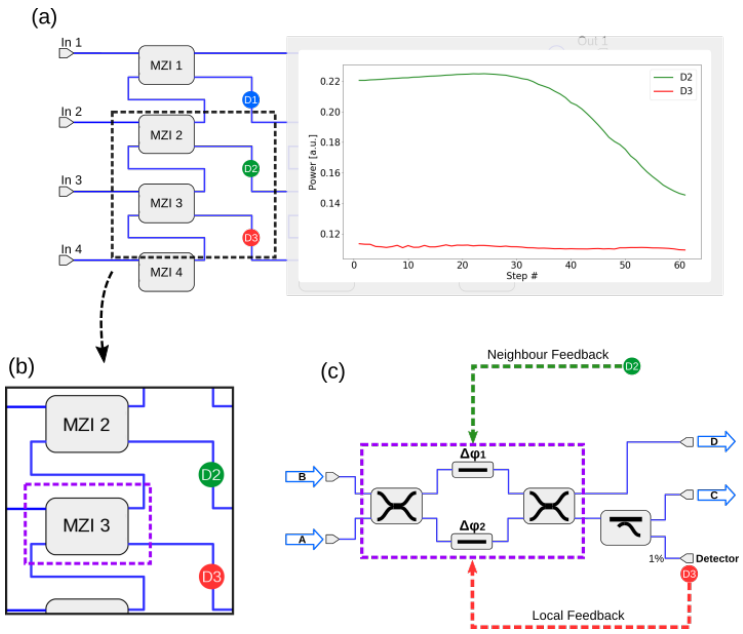

Figure 6.8: (a) Schematic of the 4×4-port universal linear circuit. (b) Zoom-in at MZI_2 and MZI_3, together with detectors D_2 and D_3. (c) Schematic of the closed feedback loop signals used to operate MZI_3. Operating MZI_3 in common-mode causes a phase shift at the signal input of MZI_2, which changes the value at its output associated to D_2.

the balance optimization step in the unit cells.

We start the configuration of the circuit by placing it in a state that we call *full-cross*, illustrated in Fig. 6.9(a). In this state the circuit will connect the inputs and outputs of the circuit as follow: $In_1 \rightarrow Out_4$, $In_2 \rightarrow Out_3$, $In_3 \rightarrow Out_2$, and $In_4 \rightarrow Out_1$. This configuration was selected to be performed initially because it can be fully automated by the global optimization algorithm. Once the circuit is configured in this state we can easily modify its connections by changing the states of the unit cells of the circuit. Fig. 6.9(b) shows a second connection state configured later to demonstrate the reconfigurability of the circuit.

6.1.5.1 Full-cross training

The training of the circuit to operate in the full-cross state is done in three phases. First we train the first stage of the circuit (Fig. 6.10(a)) to route the light path $In_4 \rightarrow Out_1$. This is done by injecting light at input In_4 of the circuit while the local optimization algorithms of the unit cells of the first stage proceed to minimize the optical power at the detectors D_1, D_2, and D_3. Fig. 6.10(b) shows the measured power at the detectors during the training process of the *Stage 1* of

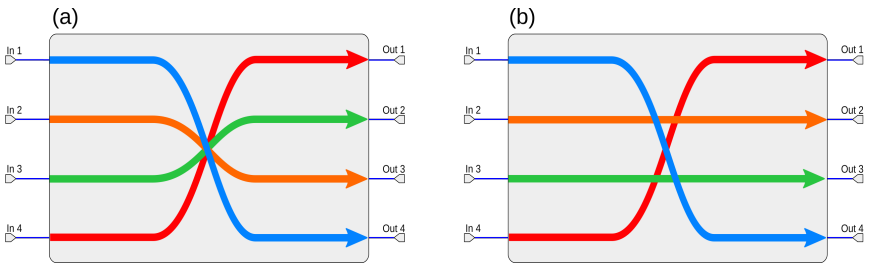

Figure 6.9: (a) Full-cross configuration. This state can be configured automatically by the global optimization algorithm. (b) Alternative configuration. This state is achieved by modifying the configuration of the circuit after the initial full-cross state.

the circuit. The algorithm progressively minimizes the power at the detectors D_3, D_2, and D_1, guiding all the light to the output Out_1 of the circuit. Fig 6.13(a_1) shows the optical path created in the circuit after the optimization process.

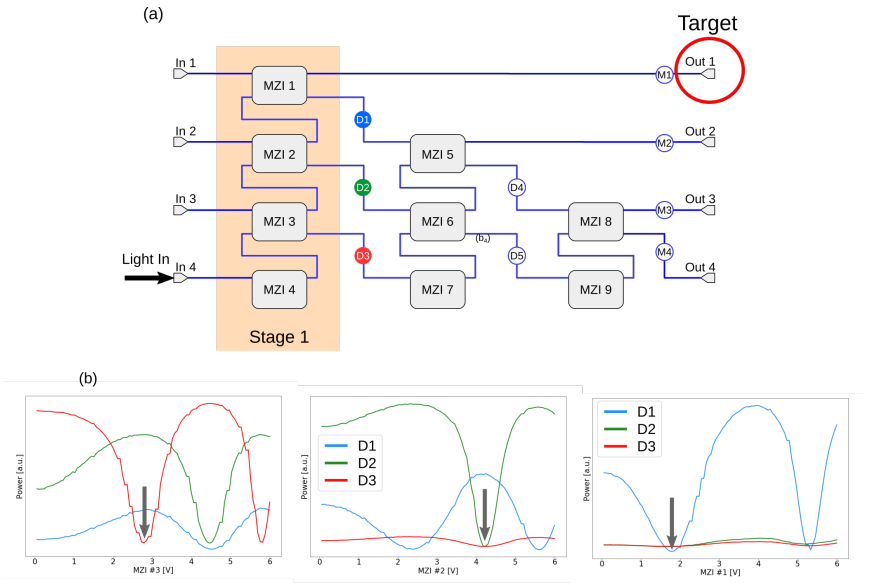

Figure 6.10: (a) Optimization of Stage 1. (b) The power at each photodetector D_3, D_2, and D_1 during the optimization process. The algorithm minimizes the power at each step of the optimization process.

Fig. 6.13(a_2) shows the transmission of the device for an input signal at port In_1. We can notice from the transmission recorded at outputs Out_1, Out_2, Out_3, and Out_4 that we have high transmission at only one of the outputs of the circuit, while the remaining outputs shows negligible power level. The measurement of

the output power was done using a camera imaging approach, and the power was measured using optical taps at the output waveguides of the circuit.

Once the first stage of the circuit is properly optimized we repeat the process with Stage 2 (Fig 6.11), where we inject light at input In_3 and the local optimization algorithms operates on MZI_6 and MZI_5 to reduce the power at detectors D_4 and D_5, creating the optical path illustrated in Fig. 6.13(b_1).

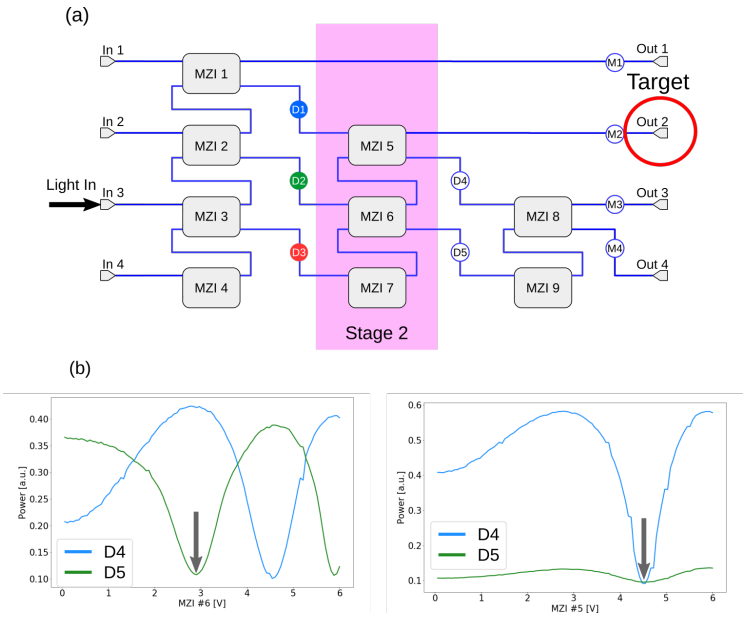

Figure 6.11: Optimization of Stage 2.

Fig. 6.13(b_2) shows the transmission of the device from input In_3 to outputs Out_1, Out_2, Out_3, and Out_4. The measurement shows a high transmission to output Out_2 while the remaining outputs have lower transmission levels.

We finally proceed to the optimization of the last stage of the circuit (Fig 6.12), which creates the optical paths $In_2 \rightarrow Out_3$ and $In_1 \rightarrow Out_4$.

Fig. 6.13 shows the transmission of the device for light input at each of the four inputs of the device. We can notice that for each input, all the light is transmitted to only one output of the circuit. At this point the optimization of the circuit is finished, and the device is configured to operate as a cross-bar switch in the full-cross state.

From this full-cross configuration state we can change the state of the device to a different configuration by changing the states of the unit cells in the circuit without requiring a new full circuit training. After configuring the device to operate in this configuration, we modified the circuit to perform a different connection

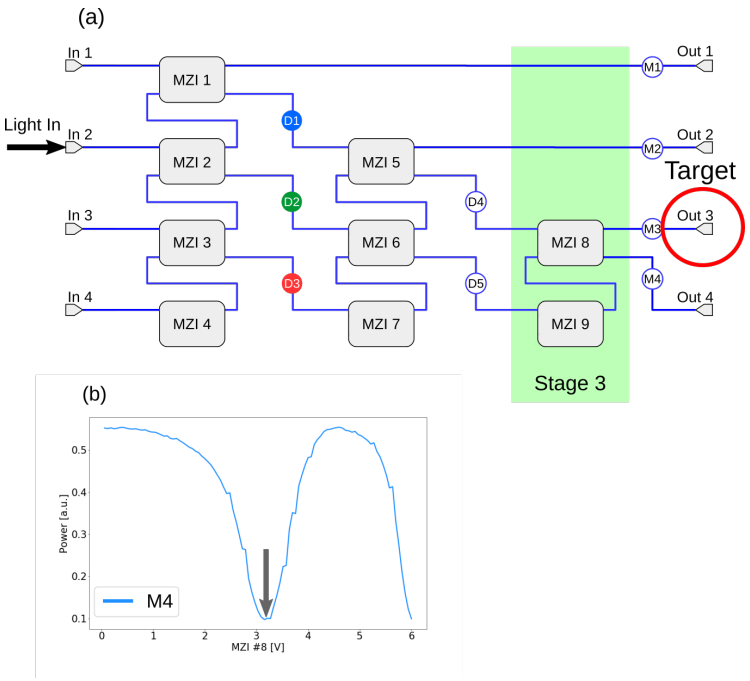

Figure 6.12: Optimization of Stage 3.

between inputs and outputs, as illustrated in Fig 6.9(b). This was done by changing the state of MZI_6, which inverted the outputs Out_2 and Out_3. The transmission of the device under this new configuration can be seen in Fig. 6.14.

The cross-bar switch shows that we can use the linear operator as a flexible interconnect. The circuit can be configured to a full-cross state by performing an automatic optimization process, and any other combination of inputs and outputs can be obtained by changing the states of specific components in the circuit.

6.1.6 Adaptive beam coupler

To demonstrate that the circuit can operate in a self-adaptive fashion we reprogrammed it to perform a beam coupling function. In this experiment we inject light in the circuit via its four input ports at the same time and the circuit automatically adjusts its configuration to maximize the power at the output of the circuit.

We inject light in the circuit using flood illumination, as illustrated in Fig. 6.15. This process assures that the power at each input of the circuit has an arbitrary value, and as the optical path in the free space propagation can be different for each input of the circuit (e.g., Fig. 6.15(b) $E_2D_3 < E_2D_4$), the phase of the optical signal at each input of the device is not necessarily equal for all inputs.

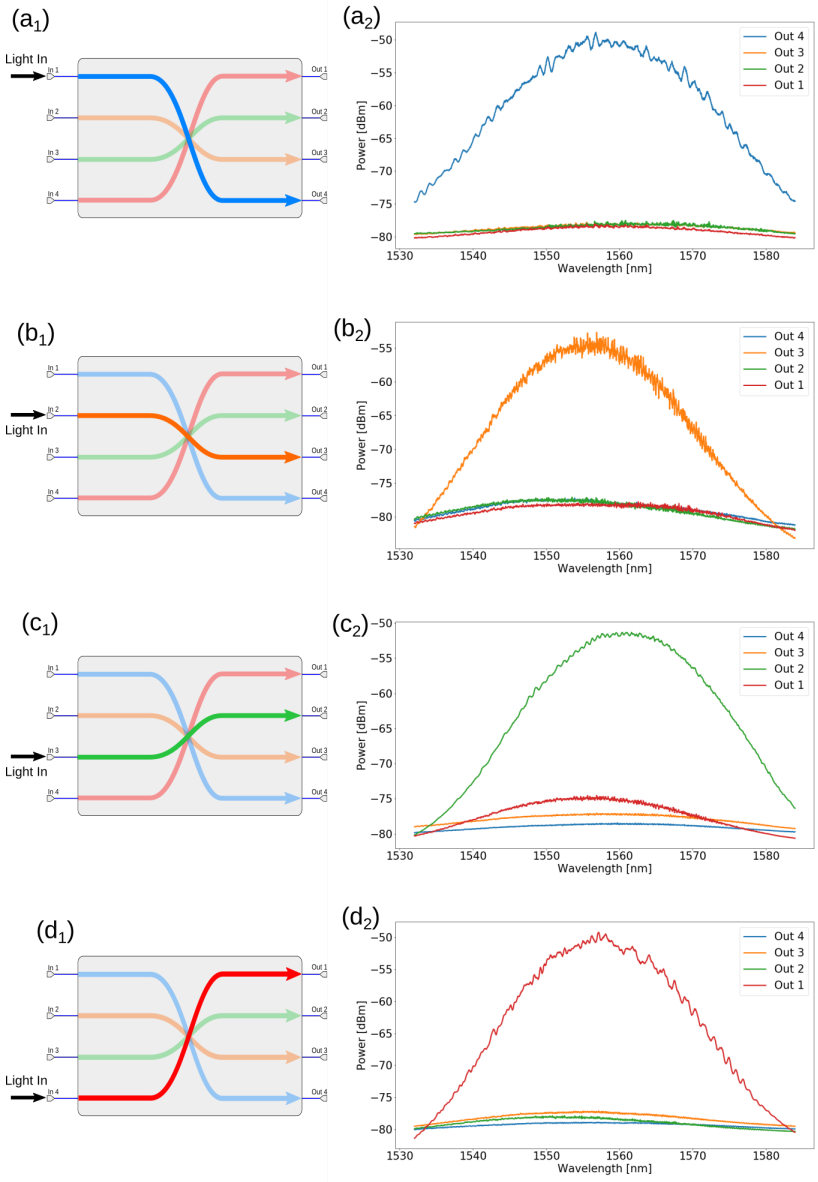

Figure 6.13: Transmission of the device for light input at each of the four inputs.

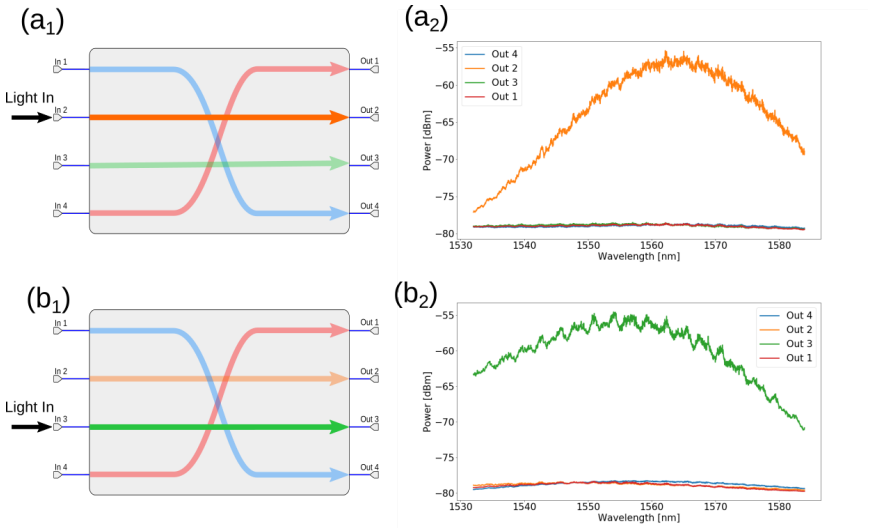

Figure 6.14: Transmission of the device after reconfiguration.

This causes the four input signals in the circuit to have arbitrary power and phase values.

The goal of the circuit operating the beam coupler function is to route all the incoming light with arbitrary power and phase to output Out_1. This is done by adjusting the unit cells in the first stage of the circuit to minimize the power at the detectors D_1, D_2, and D_3 (therefore maximizing the power at Out_1). For this operation the local optimization algorithms perform both phase and balance optimization processes at the unit cells of Stage 1, as we have multiple inputs being excited simultaneously.

To illuminate the input of the circuit we used a laser with fixed wavelength $\lambda = 1.55\ \mu m$ and $13dBm$ of power. The optimization of the MZIs was done automatically by the local optimization algorithm and the readout of the monitors was done using an IR camera. A second optical fiber was vertically coupled to a grating coupler monitor M_1 at the output of the circuit to perform real-time measurement of the power at the output.

6.1.6.1 Self adapting optimization

The self-adapting optimization algorithm is illustrated in the flow diagram in Fig. 6.16(b). The algorithm actuates in series, optimizing the balance and phase of one unit cell of the device at a time. This produces a constant increment at the power level at the output of the circuit as the optimization algorithm evolves.

Initially the algorithm performs a balance optimization in MZI_4 to maximize

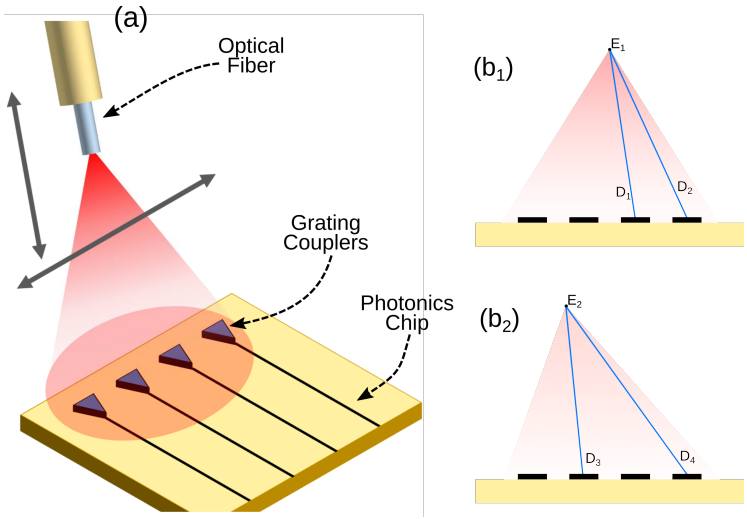

Figure 6.15: (a) Illustration of the flood illumination set-up. (b) The position of the optical fiber over the grating coupler inputs determine the relative phase between the input signals.

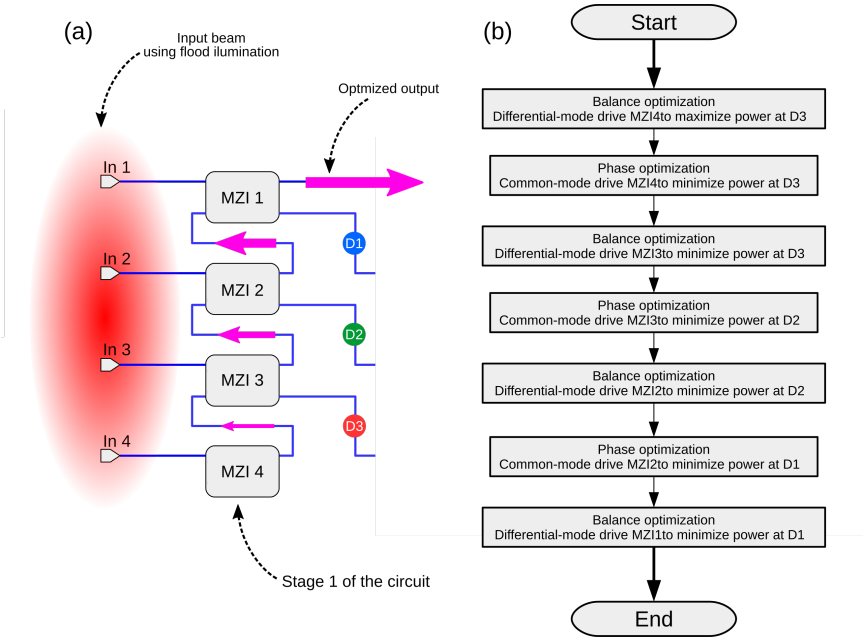

Figure 6.16: (a) Schematic of the first stage of the linear operator device with in the beam-coupling configuration. (b) Diagram flow of the algorithm used to optimize the circuit to guide all the light to the output of the beam coupler device.

the power at D_3. As MZI_4 only has one input being excited, this optimization step is only necessary to guarantee that the MZI is in the correct (bar) state. The next step in the algorithm is the phase optimization of MZI_4. In this step the local optimization algorithm drives MZI_4 in common mode (therefore operating as a pure phase shifter) to change the phase of its contributing optical signal going to MZI_3. The local optimization algorithm performs the balance optimization to minimize the power at D_3. Following, a balance optimization is realized at MZI_3 to reduce further the power in D_3. At this point we should have negligible power at D_3, meaning that all the contributions from inputs In_4 and In_3 are being guided to MZI_2 in the first stage, regardless their phase and power values. The process continues for the remaining MZIs in the stage, until we have all unit cells optimized to guide the light to Out_1.

Fig. 6.17(b) shows the balance optimization steps of each unit cell of the device. We can see in Fig. 6.17(b_1) that the optimization algorithm maximizes the power at D_3 while the remaining steps focus on minimizing the power at D_3, D_2, and D_1. This eventually guides all the incident light to the output of the circuit. Once the circuit is optimized for an incident light beam, the optimization circuit keeps operating to maintain the beam coupler in case of changes in input signal. That makes the circuit self-adapting to any change in the input signal.

The plot in Fig.6.18 shows the evolution of the total power at the output of the circuit (Out_1) after each optimization step (each step being either the balance optimization or the phase optimization of one MZI) for two distinct incident optical beams, each with the optical fiber positioned at a different position along the grating couplers of the circuit. Notice that the power increase during a phase optimization steps are substantially smaller than the contribution due the balance optimization. The reason for that is the flood illumination process, as the spacing of the input grating couplers is constant and the arm lengths are equal for all the input waveguides, resulting in a fairly small phase difference between the inputs.

6.1.6.2 Stabilization algorithm

Once the main optimization process is concluded, the global optimization algorithms enters a stabilization state, which aims to keep the circuit optimized to guide the light to Out_1. This is done by constantly performing local optimizations on the unit cells of the circuit to minimize the power level at D_1, D_2, and D_3.

Fig. 6.19 shows the relative output power at the output of the circuit over a span of one hour with and without the use of the feedback stabilization algorithm. To enforce a change in the conditions of the device over the one-hour measurement we realized the experiment with the optical chip mounted on a temperature controlled plate, and programmed a steady increase of $10\ K$ in the temperature of the device during the course of the measurement.

It is possible to notice a penalty of over $-4\ dB$ in the measured optical power

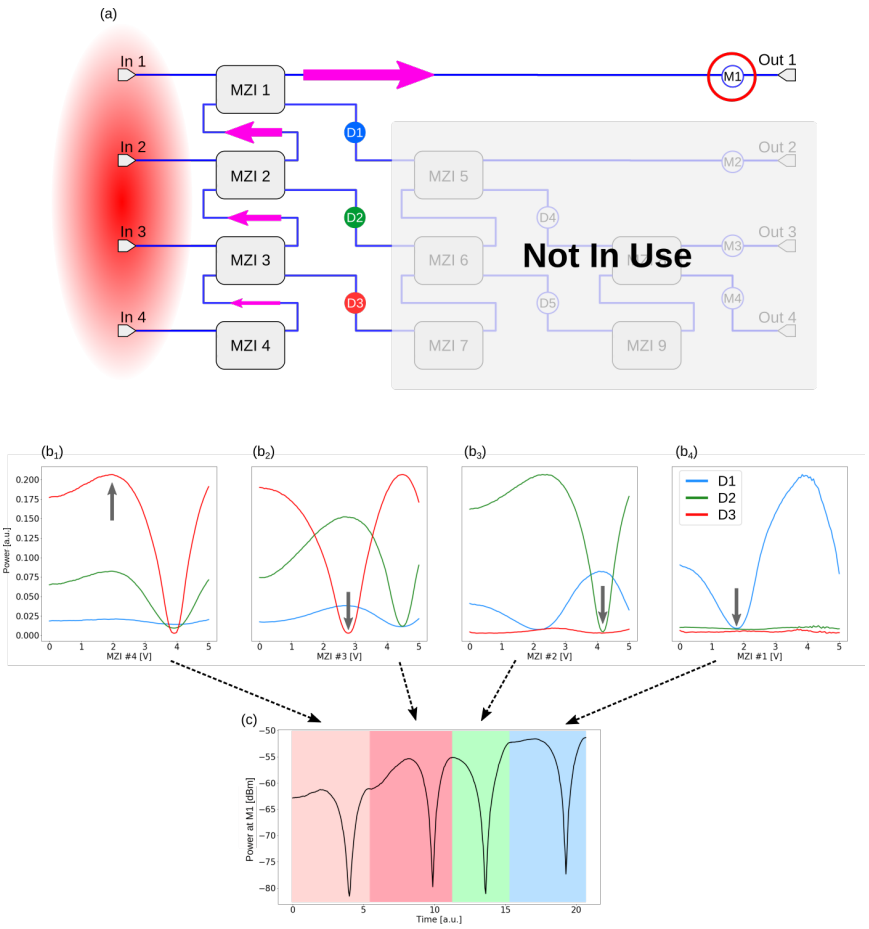

Figure 6.17: (a) Schematic of the 4 × 4-port universal linear circuit during the beam-coupling operation. (b) Evolution of the adaptive algorithm actuating in the circuit.

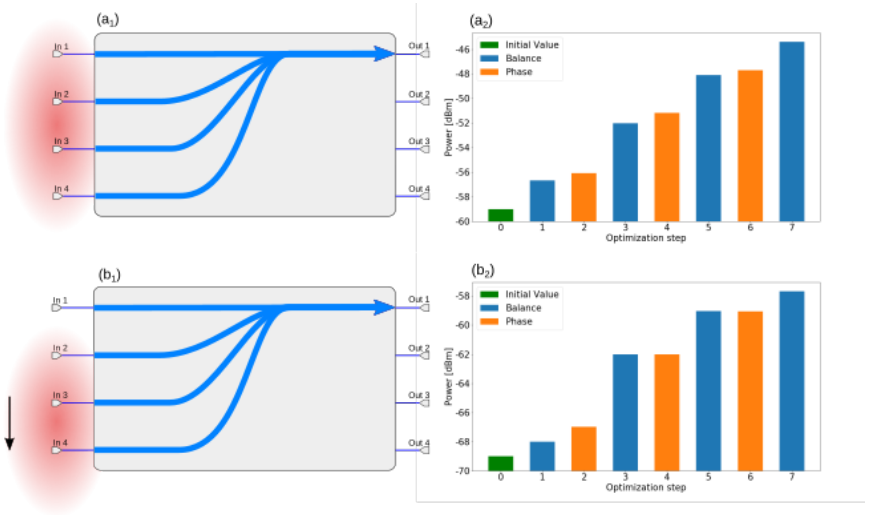

Figure 6.18: Power evolution at the output of the circuit for a centered beam and an off-set beam.

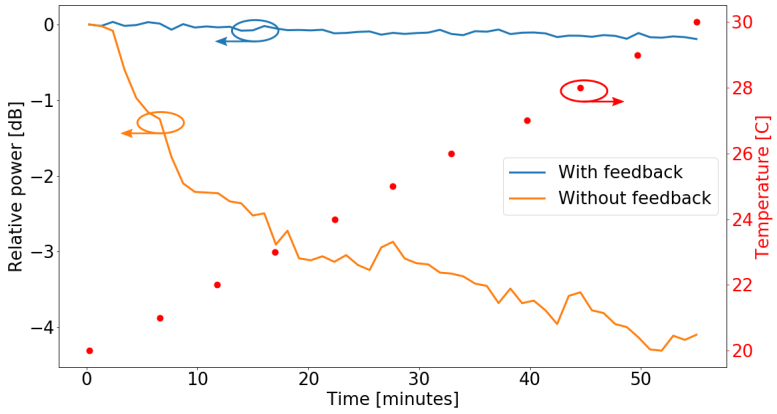

Figure 6.19: Power evolution at the output of the circuit for a fixed input beam over a span of one hour with and without the stabilization feedback loops. To enforce a change in the operating conditions during the experiment we applied a change in the temperature of the device along the experiment.

at the output of the device operating without the stabilization algorithm. This can be attributed to multiple factors, such as the drifting of the positioning of the optical fiber relative to the grating power due to the temperature change of the chip, change in the effective index of the silicon components due to the temperature changes (which leads to phase changes across the device), etc. The same experiment performed with the stabilization algorithm operating shows a much more stable power level at the output of the device over time. This is due to the operation of the feedback loops in the circuit, that constantly optimize the elements of the circuit to minimize the power at the detectors D_1, D_2, and D_3, resulting in a constant power level at Out_1. This result shows that the closed feedback loops used to optimize the programmable device are also an efficient way to increase the stability of the operating device.

6.1.7 Future work and perspectives

We have demonstrated a working implementation of a 4×4-port universal linear circuit realizing two distinct operations: a 4×4-port matrix switch and a self-adapting beam coupler. That was achieved by changing the algorithm that controls the circuit. The circuit work with self adaptive algorithms and use individual local feedback loops to enforce the adaptation of the circuit. We believe that reconfigurable and adaptive multi-port optical linear circuits can be used as building blocks to implement complex but flexible optical circuits.

The complexity of the functions that can be implemented by the programmable linear operator emerges from the number of elements in the circuit. To implement large-scale programmable linear circuits it is necessary to make use of techniques that allow the implementation of scalable optical circuits. We should not rely on having hundreds of power sources to drive a PIC with hundreds of tunable components. Because of that reason we started investigating the possibility of multiplexing the access to the phase shifters in the circuit with techniques such as digital driving and matrix addressing, discussed in earlier chapters.

6.2 Mesh-based networks

Although flexible, the linear optical processors introduced in the first section of this chapter have their drawbacks, in particular the limitation that light always propagates forward in the circuit, which prevents the implementation of optical feedback. An alternative to this topology are the optical meshes [4, 5], where tunable couplers are arranged in a mesh topology, as illustrated in Fig. 6.20. In this topology the light can be guided in any desired path, including splitting, creating feedback loops, etc. This gives a larger number of choices to create different optical circuits by rearranging the combinations of the elements of the circuit.

Fig. 6.20(b) illustrate one possible light path in an optical mesh that results in the implementation of a Mach-Zehnder interferometer, while in Fig. 6.20(c) shows the same circuit implementing a ring resonator. The path of the light is determined by programming the tunable couplers in the mesh and can be reprogrammed at users will.

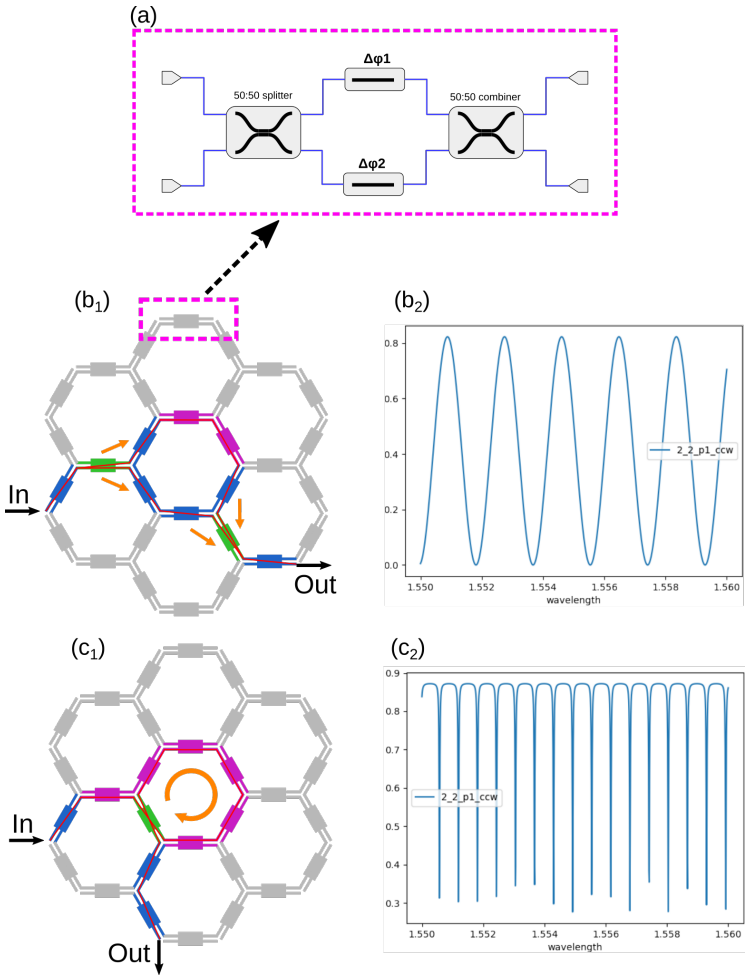

Figure 6.20: Simulated example of a 7-cells optical mesh. (a) Each element of the mesh circuit is formed by a tunable coupler. (b) The circuit configured to operate as a ring resonator. (c) The same circuit, but configured to operate as an MZI filter.

There has been quite some work done on configurable optical meshes recently [21, 22], including demonstrations of the operating concept and extensions and scalability analyses [23]. In this section we discuss the design and imple-

mentation of a large-scale optical mesh, constructed using 49 hexagonal cells in a 7×7 arrangement. The circuit contains over 150 tunable couplers and over 300 phase shifters, as well as high speed modulators and photodetectors. The circuit is designed to be operated using a time-multiplexed matrix-driving approach, which reduces the number of contact pads and power sources necessary for its operation.

6.2.1 Large-scale mesh design and fabrication

We designed our optical mesh using a hexagonal unit cell. The reason for adopting a lattice hexagonal mesh design over square or triangular lattices is due to the larger tunable elements density, the larger number of possible internal connections, and better incremental spectral resolution [24] when synthesizing functions using the mesh circuit.

The schematic of the mesh cell used in this design is shown in fig. 6.21(a). The mesh is constructed using six MZI-based tunable coupler with phase shifter in both arms, allowing them to be driven in both differential and common-mode schemes. That allows us to use any MZI in the circuit as a tunable coupler or a phase shifter (or a combination of both functions).

Fig. 6.21(c) shows the GDSII layout of the tunable coupler used in the design. The MZI is fabricated using the directional couplers discussed in Chapter 3 as splitter/combiners, and we use paperclip-shaped phase shifters in the arms of the MZI. The heaters used in the phase shifter are diode-loaded heaters, and each phase shifter has a bank of eight heaters connected in parallel. Such construction reduces the total resistance of the heater bank, which increases the power output for a given driving voltage.

The calculated resistance of the phase shifter is $R = 400\ \Omega$ for the bank of eight heaters in parallel, which yields $40\ mW$ of power when driven with a PWM signal of $7\ V$ amplitude and duty cycle $D.C. = 33\%$. Assuming a phase efficiency of $20\ mW/\pi$ (see Chapter 2), this phase shifter can perform a 2π phase shift even when used in a three-fold time-multiplexed arrangement (such as a driving matrix with 3 elements per driving channel).

The paperclip design of the phase shifter not only contributes to the efficiency of the phase shifter, as we concentrate the heated element in a smaller volume, but also reduces the footprint of the device, allowing the increase of the size of the total circuit. Constructing the phase shifter in a compact fashion and having a large number of heating elements also contributes to the increase of the thermal mass of the phase shifter, which increases its time constant [25]. This makes the phase shifter to have a slower switching speed, which facilitates the implementation of time-multiplexed driving schemes, as discussed in Chapter 4.

Fig. 6.21(b) shows the GDSII layout of the hexagonal unit cell. When compared to the schematic presented in Fig. 6.21(a) we can notice that the actual imple-

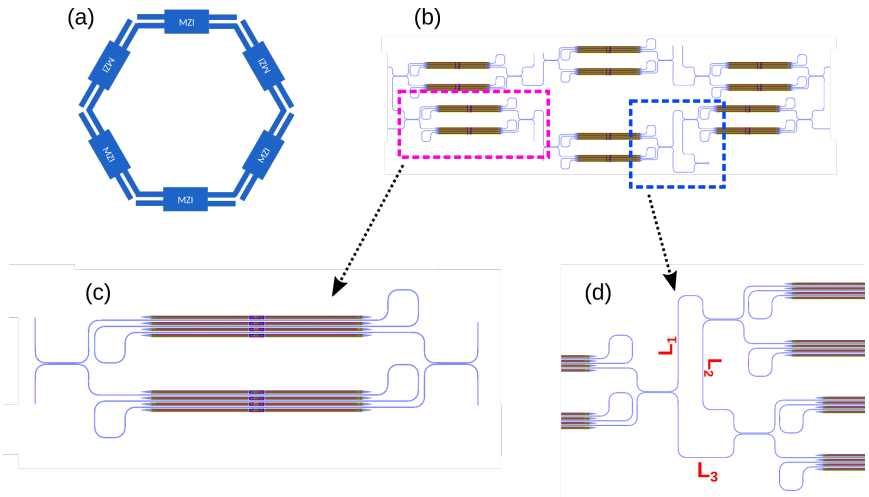

Figure 6.21: (a) Schematic of a single hexagonal mesh. (b) GDSII layout of a hexagonal cell that compose the circuit. Notice that the cell is flattened on the vertical axis to reduce the footprint of the circuit. (c) GDSII layout of the MZI used in the implementation of the mesh circuit. (d) Detail of the connection between three MZIs in a vertex of the optical mesh. To implement a balanced circuit we have to guarantee that the three waveguides have the same length $L_1 = L_2 = L_3$.

mentation design has an asymmetric shape, flattened in the vertical direction. This is done to further reduce the footprint of the device, avoiding large empty areas at the center of the hexagonal cell. This also avoids the placement of components on a non-orthogonal axis (such as $60\,\mathrm{deg}$ or $30\,\mathrm{deg}$), which could compromise the performance of the device [26].

The flattening of the unitary hexagonal cell does not affect the behavior of the device, as long as we don't change its connection properties. One important aspect that has to be preserved when flattening hexagonal cell is the optical length of the connections between the MZIs in the circuit. Fig 6.21(c) shows the waveguide connections between three MZIs at any vertex of the mesh circuit. In a non-flattened design (such as in Fig. 6.21(a)) the three waveguide connections automatically have the same length. The same is not true for the flattened design. Because of that we have to calculate the relative position of the MZIs to ensure that the three connecting waveguides have the same optical length. Fig. 6.21(c) shows the GDSII layout of the resulting connections after optimizing the waveguide length in such way that $L_1 = L_2 = L_3$. Notice that the three waveguides also have the same number of bends (2 per connection). This is important to balance the loss in the optical paths, as waveguide bends have distinct losses values [27] and effective indexes.

Fig. 6.22 shows the GDSII layout of the full circuit. The circuit consists of a

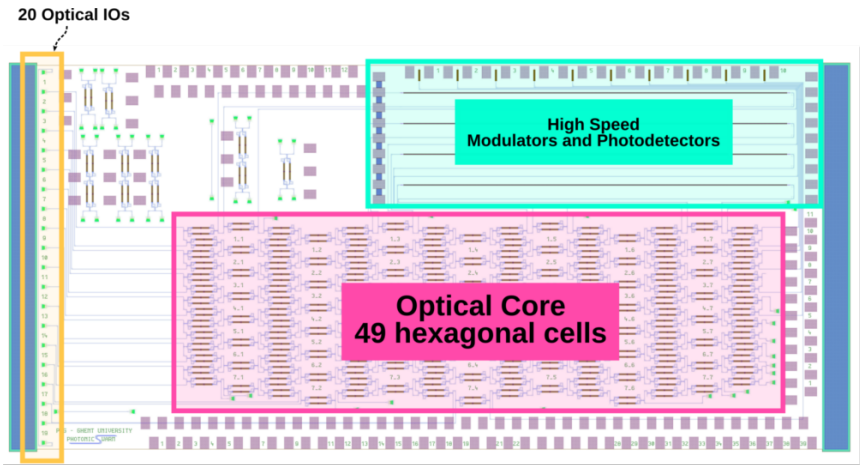

Figure 6.22: GDSII layout of the full chip. The optical core of the circuit is formed by 49 *hexagonal cells in a* 7×7 *arrangement. The circuit is also equipped with high speed modulators and photodetectors.*

7×7 hexagonal optical mesh with 20 grating couplers for optical IO placed in a fiber-array arrangement. The electrical IO is done via three arrays of aluminum contact bondpads, placed at the edges of the chip for wirebonding. The circuit also contains four high-speed modulators and ten high speed germanium photodetectors. The high-speed elements are standard building blocks from imec PDK, and are placed are connected to the optical core to extend the functionality of the circuit. Fig. 6.23 shows the summary of the designed circuit.

The circuit was designed using the $200\ mm$ silicon-on-insulator iSiPP50G full platform from imec. The platform allowed the integration of high speed germanium photodiodes and high speed modulators for implementation of RF-compatible circuits. The total size of the chip is $5.0\ mm \times 2.5\ mm$. Fig. 6.24 shows a microscope image of the fabricated device.

6.2.2 Multiplexed driving scheme

Due to the large number of tunable components in the circuit (over 300 phase shifters) it was clear from the beginning of the design that we should make use of multiplexed driving schemes to operate such large circuit. We designed the circuit to be operated using a matrix-driving approach, and divided the circuit in multiple tiers (Fig. 6.25), each having its own driving matrix and characteristics. Each tier is again divided in two identical blocks to facilitate the electrical routing of the circuit.

$Tier\ 1$ contains the first seven mesh cells that are connected directly to the op-

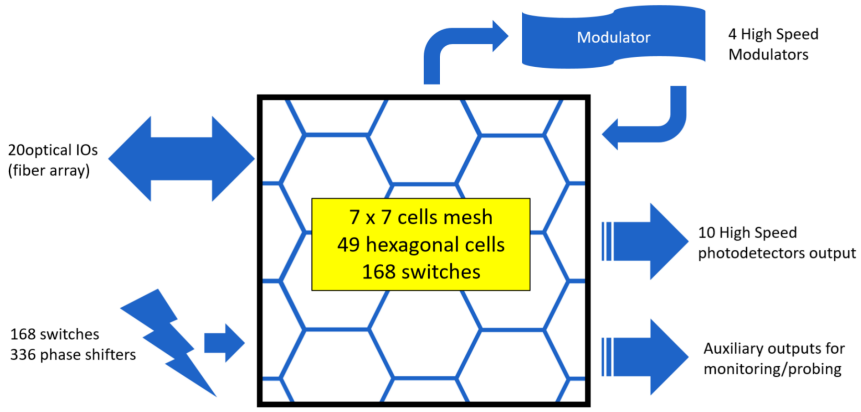

Figure 6.23: Summary of the specifications of the designed chip.

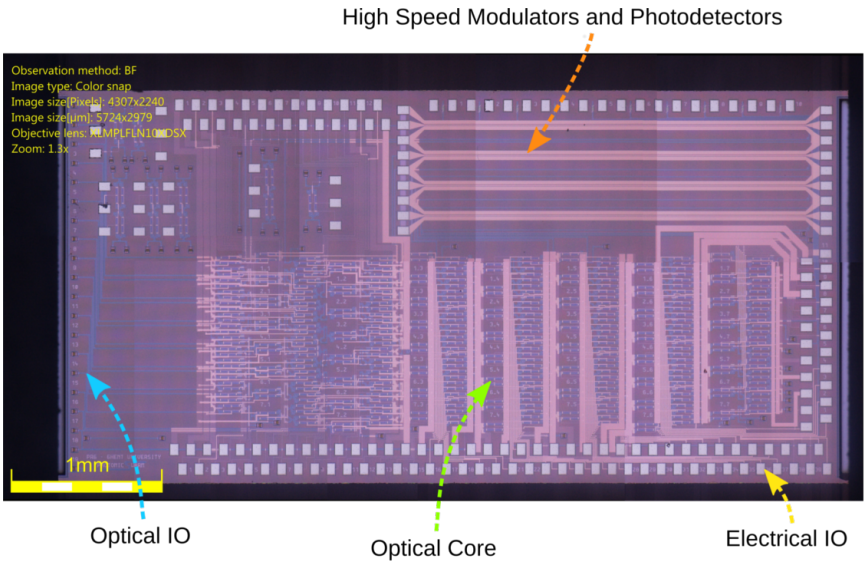

Figure 6.24: Microscope image of the fabricated device.

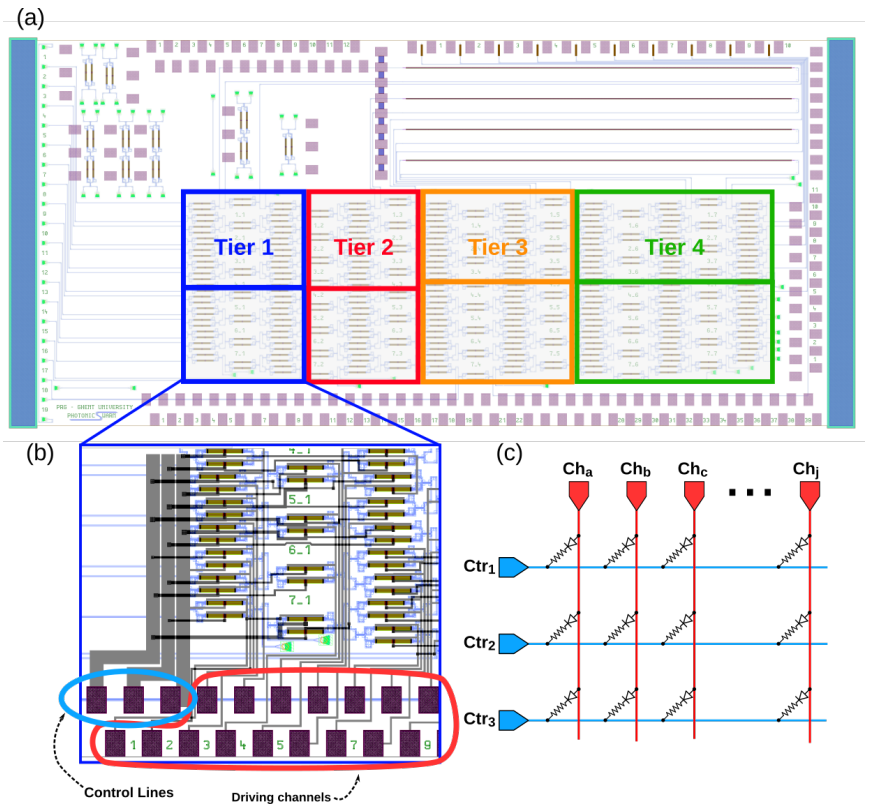

Figure 6.25: (a) The optical core is divided in multiple blocks to facilitate the electrical actuation of the circuit. (b) Each tier contains two matrix-addressed electrical circuit that allow the time-multiplexed driving of the phase shifters in the circuit. (c) Schematic of the electrical connection of the phase shifters in the matrix arrangement.

tical IOs of the circuit. Because of that the matrix topology used on $Tier1$ follows a conservative approach regarding the number of channels and control lines used to operate the matrix. Fig. 6.25(b) shows the metal routing used in the bottom half of Tier 1, while Fig. 6.25(b) shows the schematic of the connections of the phase shifters in this matrix. The matrix is designed in a 3×10 topology, meaning that we have three driving channels per control line in the matrix addressing circuit, resulting a total number of 30 phase shifters in the matrix.

$Tier$ 2 repeats the driving strategy of the first tier of having three control lines, but each driving matrix is in a 3×15 arrangement. This allows to drive more channels with the same number of control lines, but also increases the current flow in each control line.

$Tier$ 3 contains parts of the third and fourth column of hexagonal cells, and

Tier #	Matrix Topology	Max. D.C.	Notes:
1	3×10	33%	• Conservative (three fold) multiplexing • Low current at control line
2	3×15	33%	• Conservative multiplexing • Higher current at control line
3	4×10	25%	• Aggressive (four fold) multiplexing
4	4×10	25%	• Aggressive multiplexing • Some MZIs cannot be driven in common-mode

Table 6.1: Summary of the parameters of driving matrix topology schemes used in the mesh circuit.

uses a 4×10 matrix topology for routing the phase shifters. This scheme shares four heaters per driving channel, which means that each heater can be accessed by only 25% of the time at most (as opposed to 33% for the 3×10 topology used in $Tier$ 1). That reduces the maximum power output possible by each phase shifter, and can impact the operation of the circuit, as now the phase shifter can no longer be used to induce a 2π phase shift. Although that doesn't affect the use of the MZIs as a tunable coupler (as a π phase shift is enough to operate a MZI as a tunable coupler), it reduces the maximum phase shift that each MZI can yield when driven in common-mode, to operate as a pure phase shifter.

$Tier$ 4 controls the last part of the circuit, and also uses a 4×10 driving scheme, but not all MZIs in this part of the circuit can be driven in common-mode, as for each cell, three MZIs have both of its phase shifters connected to the circuit, while the remaining three have only one of the phase shifters connected to the circuit, therefore can operate only in differential mode (Fig. 6.26). That was necessary to further reduce the number of contact pads in the circuit. Table. 6.1 shows a summary of the driving scheme used by the four tiers of the circuit.

The use of a matrix-based multiplexed approach allowed a substantial reduction in the number of contact pads used to operate the circuit. The 336 phase shifters in the circuit were divided among the eight driving matrices (two per tier), which resulted in a total of 125 contact bondpads needed to drive the circuit.

6.2.3 Minimum optical length increment

One important metric from a mesh circuit is the *Basic Unit Length* (BUL) of the device [21]. The BUL is the total optical length of one edge of the hexagonal cell, and it includes the optical length of the tunable coupler plus the waveguides connecting two adjacent tunable couplers. This value is specially relevant for length-

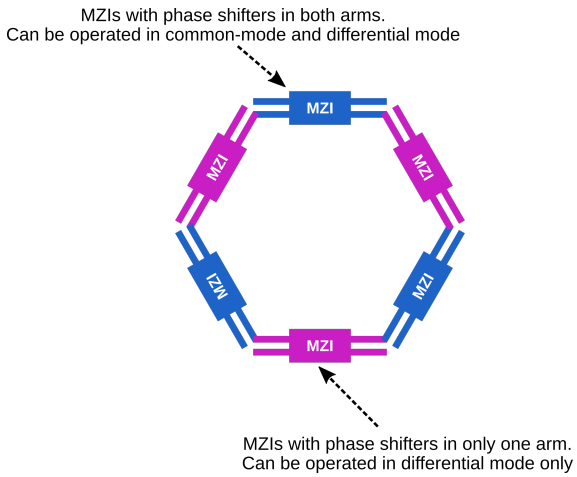

Figure 6.26: Not all MZIs in the hexagonal cells from $Tier\ 4$ can be driven in common-mode. This is done to reduce the amount of phase shifters in the circuit.

sensitive applications, such as optical cavities and interferometers, as the BUL determines what is the minimum incremental optical length resolution that can be implemented in the circuit. The mesh circuit designed during this work has a BUL of $520\ \mu m$.

We can use this value to calculate the maximum *Free Spectral Range* (FSR) that can be produced by a filter synthesized using the mesh circuit. The FSR of a MZI filter can be expressed by:

$$\Delta\lambda_{FSR} = \frac{\lambda^2}{n_g \cdot \Delta L} \tag{6.3}$$

The minimum incremental length that can be implemented in the circuit is $\Delta L = 2 \cdot BUL$ [28]. For a group index $n_g = 4.26$ and $\Delta L = 1.04\ mm$, we obtain:

$$\Delta\lambda_{FSR} = \frac{(1.55 \times 10^{-6})^2}{4.26 \cdot 1.04 \times 10^{-3}} = 0.54\ nm \tag{6.4}$$

We can verify such result by simulating an MZI filter using the designed mesh circuit. Fig. 6.27 shows the schematic of three implementations of a MZI filter using the mesh circuit. Each filter has a ΔL expressed in function of the BUL of the circuit. The filters are routed in the mesh circuit by configuring the tunable coupler in cross-state, bar-state or operating as a $50/50$ splitter.

The simulation is realized using the S-matrix circuit simulator CAPHE [29], and for sake of efficiency we simulated a circuit of reduced dimensions. Fig. 6.28 shows the normalized spectrum of the three implementations of the MZI filters

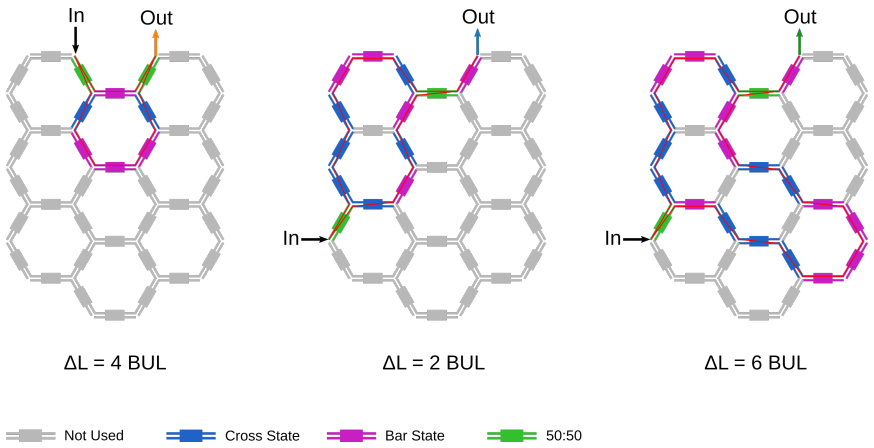

Figure 6.27: Three different implementations of a MZI filter using the mesh circuit.

illustrated in Fig. 6.27. We notice that the filter implemented using the smallest length increment ($\Delta L = 2 \cdot BUL$) has a FSR value equivalent to the calculated in Eq. 6.2.3. That represents the upper limit in terms of FSR for a filter implemented using this circuit.

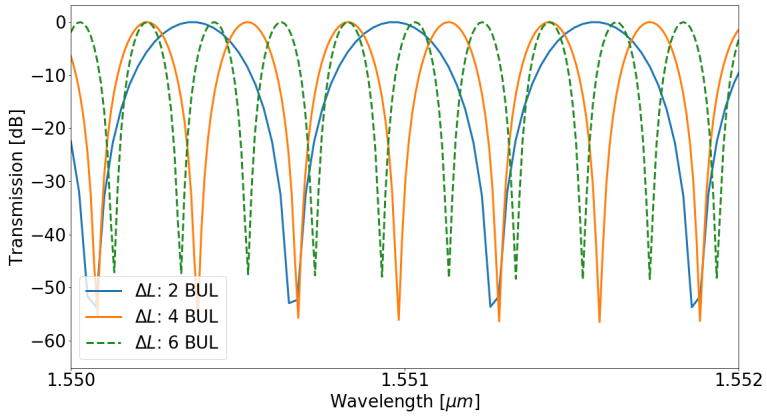

Figure 6.28: Simulation results for the MZIs filters synthesized in the mesh circuit.

6.2.4 Perspectives and Future Work

The designed circuit is currently in its initial characterisation phase, where the building blocks are being tested. Due to the size and complexity of the electrical

connections, the packaging of the circuit is being processed in collaboration with external partners to provide a stable and testable device.

Among the applications that we foresee being demonstrated using the implemented optical mesh circuit we can include:

- Configurable optical switches.
- Programmable filters.
- Programmable arbitrary multicast networks.
- Beamforming devices.
- Optical transceivers (with the use of the modulators and photodetectors included in the circuit).

We expect that the programmable mesh circuit can be and advance in our capability in both programmable photonics circuits, but also on the design and operation of large scale PICs, as we believe that proper control of large scale circuits is fundamental for the implementation of complex applications using programmable PICs.

6.3 Summary

In this chapter we discussed the implementation and demonstration of a 4×4-port linear circuit based on a feed-forward mesh topology. We demonstrated the circuit operating as a cross-bar switch matrix as well as a adaptive beam coupler. We concluded by showing how the local feedback loops can be used to stabilize the circuit over time. Beside the practical demonstrations, this initial design was important to highlight the necessity of more sophisticated driving schemes to allow the scaling of programmable photonics circuit.

The second half of this chapter was dedicated to the implementation of a large scale mesh-based programmable photonics circuit. In this design we used most of the techniques developed in this work, such as diode-based heaters and multiplexed driving schemes. We expect that this circuit can be used to expand the applications of programmable optical circuits. For that it is crucial that we establish a solid foundation on controlling of large scale PICs.

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7 Conclusion and Perspectives

7.1 Conclusions

We started this work at the beginning of the popularization of the field of programmable photonics. Even though some basic concepts were proposed decades ago, it was only with recent advances in the field of photonics (and in special in silicon photonics) that the implementation of complex programmable photonics circuits became feasible. Our first approach to programmable PICs was the implementation of the 4×4-port universal linear circuit [1], heavily influenced by the work of David Miller [2]. With this work we managed to do the first demonstration of a fully reconfigurable linear operator in silicon photonics. To demonstrate its capabilities we demonstrated multiple functions using the same optical chip, including a cross-bar optical switch and a self-adjusting beam coupler.

Our first demonstration of a programmable photonics circuit not only showed the capability of such topology of optical circuits, but it was also important to show us the limitations of our current library of components, building blocks and techniques to implement large scale programmable photonics circuits. It was clear after the first demonstrations that our capability on controlling programmable PICs was not fit for scaling up to devices with hundreds or even thousands of elements.

We started addressing these issues with the development of a customized library of photonics components with large scale programmable circuits applications in mind. In this process we developed phase shifters and optical couplers (both passive directional couplers and also tunable power couplers) with charac-

teristics that would fit in the implementation of large programmable circuits. This included the diode-heaters, used for time-multiplexed access using duobinary signals and matrix-addressing, and the paperclip-shaped phase shifter, to improve the power efficiency of the thermo-optic phase shifter. We also developed a two-stage MZI-based tunable coupler, the $2\times2\times2$ tunable coupler, to implement high extinction ratio tunable couplers with imperfect optical components, such as directional couplers with a split ratio as unbalanced as $25/75$.

With the increase in size of programmable PICs, a larger number of active components are used to control the circuit. To power photonics circuits with hundreds of active components we cannot assume that we will have hundreds of electric power sources at our disposal. For that reason we invested in developing techniques for time-multiplexing the access to the phase shifters in the circuit. We did it by implementing a digital-driving technique that uses a PWM signal for driving thermo-optical based phase shifters. This is possible to the very high thermal constant of the device (in the order of $\tau \approx 100\ \mu s$).

With the increase in complexity of the building blocks used to implement programmable photonics circuits, a more elaborated control scheme was needed to operate the components in the circuit. We implemented dedicated control schemes using a closed feedback loop to monitor the behavior of the photonics components in the circuit and adapt the driving signal used for tuning the circuit. Among the dedicated control algorithms implemented during this work we discussed the common-mode and differential mode actuation of tunable couplers and the optimization of the $2 \times 2 \times 2$ tunable coupler using the gradient descent method. To manage the optical programmable PIC as a whole we introduced the concept of a global optimization algorithm, that control the overall functions of the optical chip. After integrating the PIC with electronics and software control, the programmable circuit is no longer one single complex optical circuit alone, but a system that combines photonics (in the form of a PIC), electronics (for the drivers and the controllers), and software (for both controlling the individual elements of the system and as an interface to the final user).

The implementation of a large-scale 7×7-cells optical mesh during the final part of this work makes use of multiple techniques and building blocks developed over the four years of this Ph.D.. The implementation of a PIC with such large number of tunable phase shifters (> 300) is only possible if we multiplex the use of the contact pads in the circuit to reduce the final footprint of the device and to reduce the total number of power sources needed to drive the circuit. Also, the use of PWM driving source simplifies the electronics involved in the system, as PWM requires one single fixed-voltage power source instead of multiple tunable power sources. On the control side, the use of local optimization loops with closed feedback loops from the system allows an individual control of each independent element of the circuit. The use of paperclip-based phase shifters and diode-heaters

were essential to the implementation of the circuit.

7.2 Perspectives and Future Work

Programmable circuits is a paradigm that can be explored to implementation of multiple applications in silicon photonics. Both topologies discussed in this work can be used to extend and add flexibility to PICs applications.

Although we have made progress on multiplexing access driving, a validation in a very-large scale circuit is still needed to consolidate the technique. This can be achieved with the development of more power-efficient phase shifters, associated with heaters with even higher thermo-optical constant, which would allow time-multiplexing a larger number of phase shifters in a same channel in a matrix-topology. Other addressing topologies, such as *charlieplexing* [3] could be explored.

Programmable PICs can be extended to add flexibility in specialized optical circuits. The integration of programmable circuits with dedicated building blocks such as high-speed modulators and photodetectors to implement programmable optical transceivers is an example of venues that can be explored.

Scaling up is always a necessity when it comes to increasing the number of functions that can be performed by a programmable PIC. To increase the number of elements in the optical circuit we need to increase the availability of electronics for powering and control of the programmable circuit. Better packaging solutions and electronics integration, such as flip-chipping the electronics IC onto the optical chip, are possibilities that should be explored. Also, large optical circuits have to deal with high optical losses. Integrating power source and amplifiers could be a way to avoid such problem.

One area of this work that still has to be explored is the human-machine interface and possible synthesis of optical functions from human-friendly specifications. This opens space for implementation of a language specifications to define the optical functions on programmable PICs, automatized tools to translate such definitions into electrical signals to operate the optical chip, etc.

We expect that the work presented here helps moving forward the development of programmable PICs in silicon photonics, and we believe that programmable PICs will be part of the future of Silicon Photonics.

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A
Design Error

Due an error during the design of the directional coupler used for the $2 \times 2 \times 2$ tunable coupler (Chapter 3) the device was fabricated with directional coupler with incorrect dimensions. In this appendix we discuss the error in the design process and the approach we used to obtain meaningful results from the experiment.

A.1 Parametric cells

The process of designing an integrated photonics circuit requires dedicated techniques for data and information management. As a circuit is a complex structure, with multiple components and sub-components, we adopt an hierarchical structure to layout the circuit.

The most basic element in this structure is a *parametric cell* (PCell). A PCell is a data structure that contains information about one specific component in the circuit. As a component has multiple domains, the PCell is sub-divided in multiple *views*, each containing its own set of parameters. The example in Fig. A.1 shows how the data structure of a directional coupler can be expressed in this hierarchy. At the top level, the PCell contain its global set of parameters, such as the name of the PCell. Parameters that are at the PCell level can be accessed by all views in the hierarchy. Each view in a PCell can define its own set of parameters, and a parameter from one view is not automatically visible to a different view. The PCells are implemented in the IPKISS framework, in the form of Python code.

If we want to change a parameter that belongs to one specific view, we have

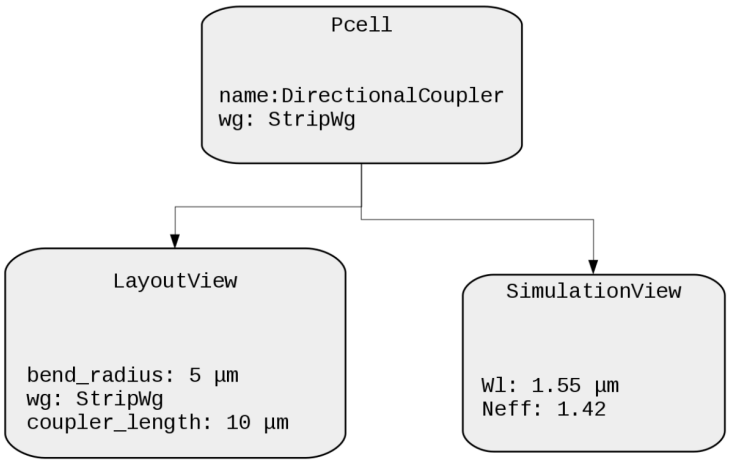

Figure A.1: The design of a photonics component is organized hierarchically. One parametric cell contains multiple views, each with its own parameters.

to specify the view and the parameter we are modifying. Fig A.2 shows how we change the coupling length parameter of a directional coupler PCell. As the parameter belongs to the layout view of the component, we have to specify not only the parameter, but also the appropriated view which its belong.

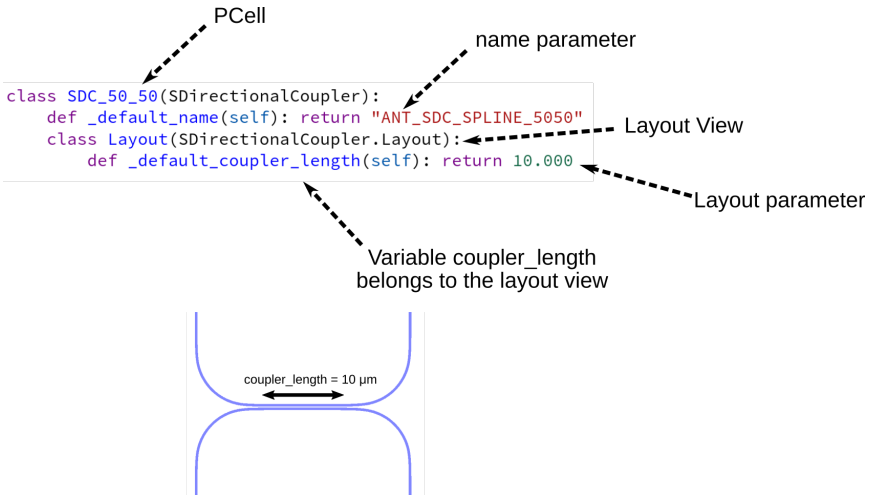

Figure A.2: To modify the value of the parameter of a view, we define its value inside their respective view.

A.1.1 Design error source

Due to a modification in the component library during the development of the design, the value for the parameter that defines the coupler length was misplaced. The parameter, that was supposed to be set in the layout view, was defined directly in the PCell of the component (Fig. A.3). As the PCell doesn't have a parameter named *coupler_length*, the line was ignored by the design tool and was never executed. As a result the directional coupler component was generated with a incorrect value for the coupler length.

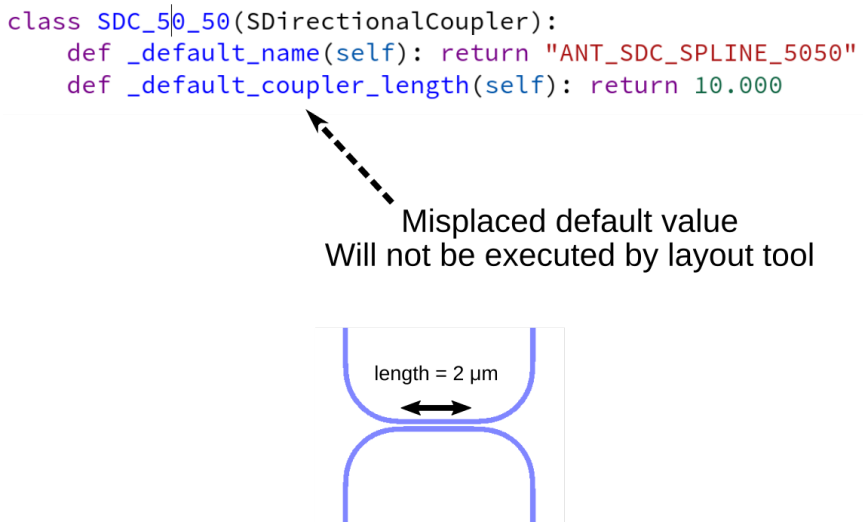

Figure A.3: As the PCell doesn't have a parameter named coupler_length, this line of code will not be executed. The layout view will use the system default value for this parameter instead.

This error in the definition of the component parameter caused all the directional couplers in the circuit to be fabricated with a coupler length value different from the value obtained during the design of the component. This resulted in a directional coupler with coupling length much smaller than required by design.

A.2 DC Wavelength dependency

Although the fabricated device showed a coupling coefficient too low for proper operation ($\kappa = 0.20$ at wavelength $\lambda = 1.55\ \mu m$), we could explore the wavelength dependency of the directional coupler to operate the device at a longer wavelengths.

Fig. A.4 shows the simulated coupling coefficient of the fabricated device for

longer wavelengths. As we can see, the simulation shows a coupling coefficient $\kappa > 0.25$ for a wavelength $\lambda = 1.616\ \mu m$. As the $2 \times 2 \times 2$ tunable coupler requires a device with coupling coefficient $0.25 < \kappa < 0.75$ to work properly (see Chapter 3, Fig. 3.20), we can still operate the circuit as long as we do it at wavelength $\lambda = 1.616\ \mu m$.

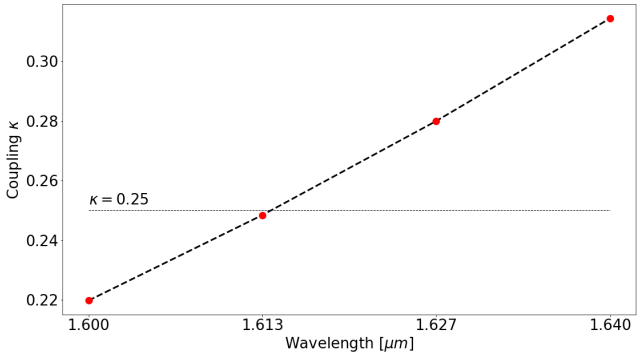

Figure A.4: Coupling coefficient of the device in function of wavelength. Even tough the directional coupler is not long enough to provide a $25/75$ coupling ratio for $\lambda = 1.55\ \mu m$, if we operate the device at a longer wavelength we can reach a higher coupling ratio.

Fig. A.5 shows the FDTD simulation of the fabricated directional coupler for wavelengths $\lambda = 1.55\ \mu m$ and $\lambda = 1.616\ \mu m$.

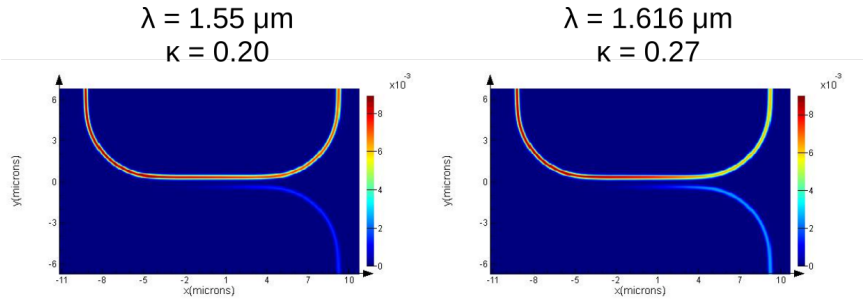

Figure A.5: FDTD simulation of the fabricated device shows a coupling coefficient $\kappa = 0.27$ for wavelength $\kappa = 1.616\ \mu m$.

A.3 Final thoughts

An error in the definition of the component library resulted in a circuit fabricated with incorrect dimensions, even tough the device was properly designed. A number of actions were adopted to avoid this problem in the future:

- Adoption of standardized library: We adopted the use of a standard library of components, open for all members of the research group. This possibilities reusability and better control of components, avoiding code duplication.
- Peer reviewing modifications in the standard library: Peer-reviewing all modifications in components from the standard library has been adopted as a mandatory step when modifying the library.
- Peer reviewing the final circuit mask design: Before taping-out a design, a third-part member has to review the circuit, flagging possible design errors.

B

Phase Difference Monitor for Arbitrary Signal Amplitude

In Chapter 5 we introduced the *Phase Difference Monitor* (PDM) as a component that can be used to extract the relative phase difference for two optical signals of same wavelength and equal amplitude. Fig. B.1 shows the schematic of the PDM implemented in this work. The device uses power taps to tap-off a fraction of the light from the targeted waveguides and used a MMI as a interferometer, to infer the phase difference between the two signals.

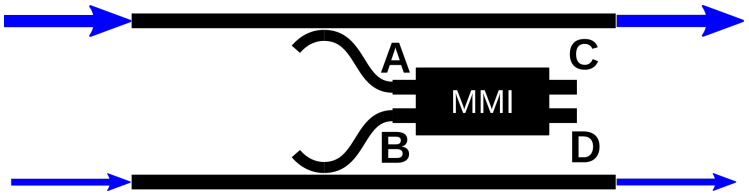

Figure B.1: Schematic of the interferometer of the phase monitoring device.

The transmission to outputs C and D of the device can be expressed as:

$$T_C = \frac{\sqrt{2}}{2}(A + B \cdot e^{j \cdot \frac{\pi}{2}}) \tag{B.1}$$

and

$$T_D = \frac{\sqrt{2}}{2}(A \cdot e^{j \cdot \frac{\pi}{2}} + B) \tag{B.2}$$

Where A, B, C, and D are complexes values. If the input values A and B are two monochromatic optical signals with the same wavelength, we can express A and B as:

$$A = a \cdot e^{j \cdot \phi_a} \tag{B.3}$$

and

$$B = b \cdot e^{j \cdot \phi_b} \tag{B.4}$$

Where a and b are the amplitude of the input signals and ϕ_a and ϕ_b their respective phases. We than can express the output T_C as:

$$T_C = \frac{\sqrt{2}}{2}(a \cdot e^{\phi_a} + b \cdot e^{j(\phi_b + \pi/2)}) \tag{B.5}$$

We can define the input A as our reference signal (making $a = 1$) and treat B relative to A. Fig. B.2 shows the output T_C in function of the phase difference $\Delta\phi = \phi_a - \phi_b$ for different relative values of b. The plot shows that it is still possible to extract the relative phase between tho signals of different amplitude using the PDM device, even if the inputs have distinct amplitude levels, with the condition that the power ratio between the signals is know.

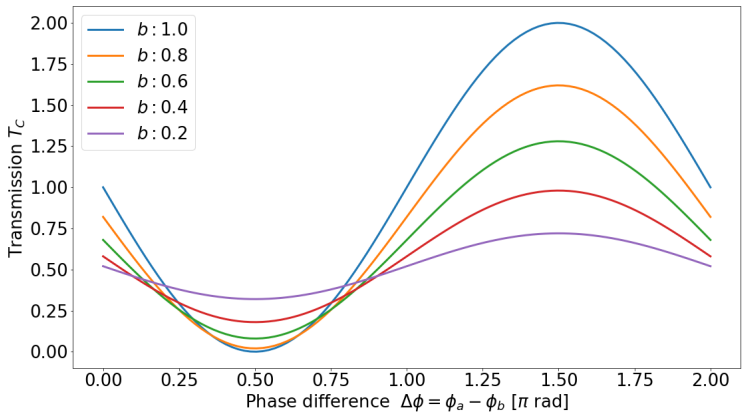

Figure B.2: Transmission T_C of the PDM device shown in Fig. B.1 in function of the phase difference $\Delta\phi$ between the two input signals A and B.